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***Abstract*—Power supplies for high-temperature superconducting (HTS) magnets placed inside of the magnet's cryostat to improve the system-level energy efficiency are four-quadrant (4Q) step-down dc-dc converters operating from an input dc voltage of about 1 V and conventionally employ paralleled full-bridge (FB) phase modules. Leveraging the limited but sufficient reverse blocking capability of GaN transistors, we propose a new three-switch T-Type (3S-TT) phase module topology, which reduces conversion losses by a factor of 2 while requiring 25% fewer transistors compared to conventional FB phase modules, i.e., enables more efficient and/or more compact power supplies with fewer phases.**

***Keywords*—GaN, HTS magnet, multi-phase, full-bridge, T-Type.**

I. INTRODUCTION

Future particle accelerators such as the Future Circular Collider (FCC) [1] at CERN should feature circumferences of 80…100 km, i.e., much more than today's Large Hadron Collider (LHC), to facilitate fundamental physics experiments with ever higher particle energies. Significant energy savings—[2] estimates a power demand reduction from 79 MW to 12 MW—could be achieved if the thousands of high-current electromagnets needed for guiding and shaping the particle beam were realized with high-temperature superconducting (HTS) magnets operating at around 40…60 K instead of with normal-conducting or low-temperature superconducting coils.

However, if the HTS magnets (e.g., $L_{\mathrm{load}} = 500\,\mathrm{mH}$ and parasitic $R_{\mathrm{load}} \approx 1\,\mu\Omega$) in their cryostats are supplied from external power supply units (PSUs) operating at typical ambient temperatures of $T_{\mathrm{amb}} \approx 25\,°\mathrm{C}$ (298 K) [3], unavoidable heat leak-in occurs via the thick current leads needed for high magnet currents [4], increasing the required cooling power/energy [5]–[7]. Cryogenic PSUs *inside* of the cryostat [5], [8]–[11] could

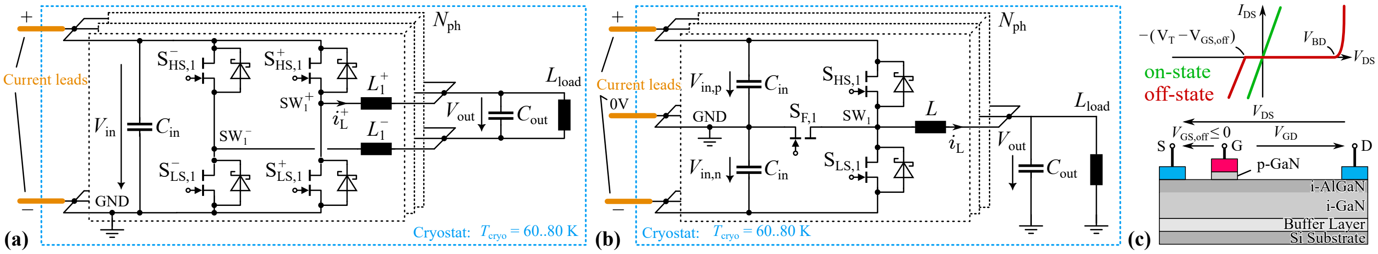

Fig. 1. Multi-phase HTS magnet 4Q PSUs based on **(a)** full-bridge (FB) phase modules (coupled inductors possibly needed to suppress circulating currents not shown) and **(b)** the proposed three-switch T-Type (3S-TT) bridge-leg topology. The midpoint switch $S_{\mathrm{F},1}$ is realized using a single standard GaN transistor, whose (limited) reverse blocking capability of up to $V_{\mathrm{DS}} \geq -(V_{\mathrm{T}} - V_{\mathrm{GS,off}})$ indicated in **(c)** suffices for the low dc voltage $V_{\mathrm{in,n}} < 2\,\mathrm{V}$. Note the Schottky diodes in parallel to the other GaN transistors to minimize the deadtime conduction losses.

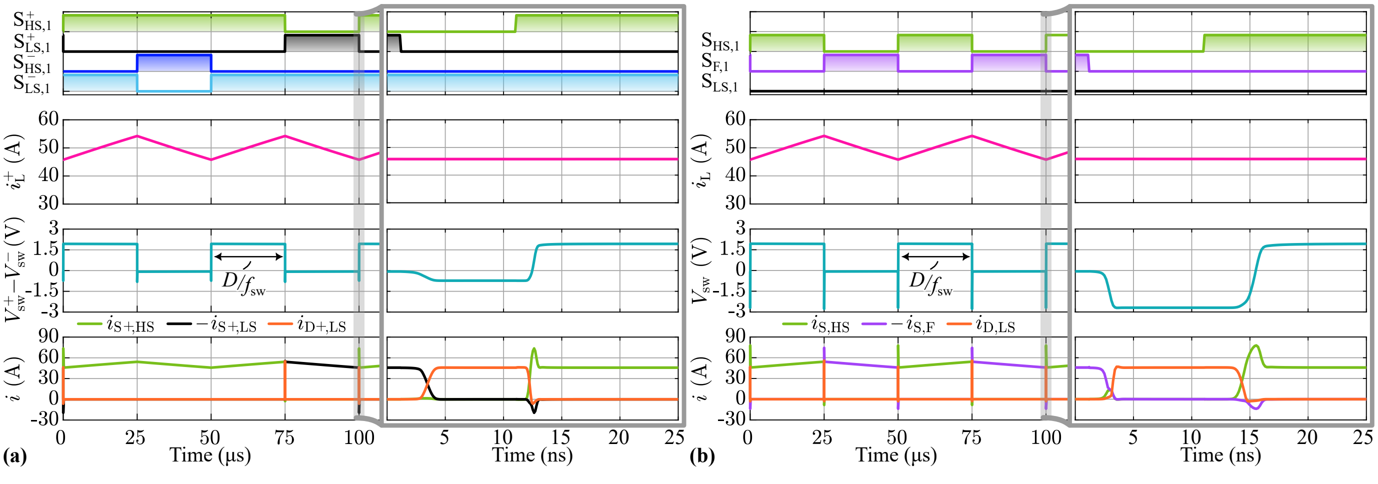

Fig. 2. Exemplary simulated (LTspice) key waveforms of a single phase module with a duty cycle of $D = 50\%$, effective switching frequency of 20 kHz at the output, and one EPC2302 GaN HEMT per switch position. **(a)** FB phase module with $V_{\mathrm{in}} = 2\,\mathrm{V}$, $L^+_1 = L^-_1 = 1.5\,\mu\mathrm{H}$, and $f_{\mathrm{sw}} = 10\,\mathrm{kHz}$ (per switch), and **(b)** proposed 3S-TT phase module with $V_{\mathrm{in,p}} = 2\,\mathrm{V}$, $V_{\mathrm{in,n}} = 2\,\mathrm{V}$, $L = 2L^+_1 = 3\,\mu\mathrm{H}$, and $f_{\mathrm{sw}} = 20\,\mathrm{kHz}$; the zoomed view indicates that the commutation from $S_{\mathrm{HS},1}$ to the midpoint switch $S_{\mathrm{F},1}$ involves the anti-parallel diode of the low-side switch $S_{\mathrm{LS},1}$, as the switch node is at $-V_{\mathrm{in,n}}$ during the interlock delay time.

thus potentially realize further energy savings. For example, a 250 A cryogenic multi-phase step-down dc-dc converter based on $N_{\mathrm{ph}} \approx 5 \ldots 10$ full-bridge (FB) phase modules (see **Fig. 1a**, **Fig. 2a**) with four parallel EPC2302 GaN HEMTs per switch position and operating with an (effective) switching frequency of 20 kHz (due to control bandwidth requirements [12]) could achieve overall losses inside of the cryostat (including leak-in losses) of around 5 W, i.e., a fourfold reduction compared to the losses if an external power supply was used [4], [5]. Still, the major share of the FB-based PSU losses are semiconductor conduction losses. Therefore, this paper proposes a new phase module topology that ultimately could enable an at least twofold further reduction of the system losses.

II. Proposed LV Three-Switch T-Type (3S-TT) Topology

Fig. 1b shows the proposed three-switch T-Type (3S-TT) bridge leg, whose switch node SW_1 can be tied to the positive, middle or negative rail, i.e., $V_{\mathrm{in,p}} = V_{\mathrm{in,n}} = V_{\mathrm{in}}$ results in the same bipolar and/or three-level output voltage capability as the FB. Unlike conventional TT bridge-legs [13], [14], the midpoint switch $\mathrm{S}_{\mathrm{F},1}$ is realized with a standard GaN transistor instead of with either an anti-series connection of two such transistors or a monolithic bidirectional switch [15]–[17]. A single standard GaN transistor suffices due to the very low dc voltages of typically $V_{\mathrm{in,p}} \leq 2\,\mathrm{V}$ and/or $V_{\mathrm{in,n}} \leq 2\,\mathrm{V}$: as indicated in **Fig. 1c**, the essential (functional) symmetry of a GaN HEMT can support a negative drain-source voltage $V_{\mathrm{DS}} < 0$ as long as the gate-drain voltage $V_{\mathrm{GD}} < V_{\mathrm{T}}$ where V_{T} is the threshold voltage, or, in other words, as long as $V_{\mathrm{DS}} > -(V_{\mathrm{T}} - V_{\mathrm{GS}})$. Thus, a negative gate-source voltage V_{GS} can be employed to increase the reverse blocking capability to some extent.[1],[2] Advantageously, only *one* switch is located in the load current path (i.e., in series with the load) at any given time instead of two switches in case of the FB. Therefore, considering the same number of transistors for each position, the proposed 3S-TT reduces the conduction losses by at least a factor of two.[3]

Fig. 2 further shows key waveforms of the FB and the proposed 3S-TT phase module (i.e., $N_{\mathrm{ph}} = 1$ is considered in the following), where identical output voltages and hence identical requirements and stresses for the (total) series inductor and the output filter capacitor result (note that the device switching frequency of the 3S-TT is twice that of the FB, however). Note further that in the 3S-TT, the commutation from $\mathrm{S}_{\mathrm{HS},1}$ to the midpoint switch $\mathrm{S}_{\mathrm{F},1}$ involves the anti-parallel diode of the low-side switch, as can be seen in the zoomed waveforms; i.e., there are no soft commutations, which is acceptable due to the low switched voltages and dominating conduction losses.

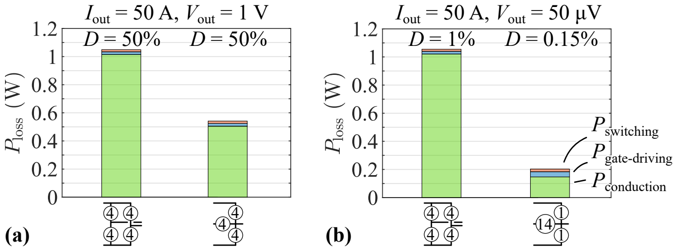

Fig. 3. Calculated switching-stage losses for an FB and a 3S-TT phase module with equal effective switching frequencies of 20 kHz ($f_{\mathrm{sw,FB}} = 10\,\mathrm{kHz}$ and $f_{\mathrm{sw,3S-TT}} = 20\,\mathrm{kHz}$) and thus equal output voltage quality. **(a)** Operating point from **Fig. 2** using four parallel EPC2302 GaN transistors per position. The twofold reduction of conduction losses (which is independent of D) is clearly visible. **(b)** Typical HTS magnet PSU operating point (very small D), where the 3S-TT features the same total of 16 transistors as the FB, but with optimized allocation to switch positions (in case of the 3S-TT, see text).

Fig. 3 illustrates the reduction of the switching stage losses of the 3S-TT compared to the FB phase module for equal DM output voltage quality and hence equal conditions for the inductors and output filter. Considering the operating point from **Fig. 2** and four parallel EPC2302 transistors per position for the FB phase module, **Fig. 3a** confirms the dominance of conduction losses and hence about a factor of 2 lower losses for the 3S-TT compared to the FB phase module, even though only 12 instead of 16 transistors are used.

Optimizing the performance of the 3S-TT phase module for a specific operating point, i.e., very low and positive output voltages in case of an HTS magnet supply in steady-state, $\mathrm{S}_{\mathrm{F},1}$ should feature much more chip area than the other two positions, which **Fig. 3b** illustrates for the case of equal total number of 16 transistors. Note that also the FB transistor allocation could be changed (not shown) to favor, e.g., the low-side freewheeling path by placing 7 parallel transistors for positions $\mathrm{S}^{-}_{\mathrm{LS},1}$ and $\mathrm{S}^{+}_{\mathrm{LS},1}$, respectively (the FB modulation must be modified such that only this freewheeling path is used). Then, for the same total of 16 transistors, the 3S-TT conduction losses are still only $(1/14)/(2/7) = 1/4$ that of the FB. In general, the asymmetric transistor allocation leads to increased losses for higher output voltages, which are required during ramp-up/down of the magnet current [5]. Thus, a trade-off between low steady-state losses and maximum ramp rates exists, depending on the specific application.

III. Conclusion

The proposed 3S-TT topology has the potential to reduce the losses of cryogenic four-quadrant step-down multi-phase GaN converters by a factor of $2 \ldots 4$ and/or to reduce the number of employed transistors or phase modules, enabling more compact realizations. Further research will address the system-level optimization, including ramp-up/down, leak-in losses, etc., and the experimental verification.

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[1] Specifically, $V_{\mathrm{GS,off}} = -1\,\mathrm{V}$ is used for the considered EPC2302 transistors with $V_{\mathrm{T}} \approx 2\,\mathrm{V}$ [18], [19]. Note also the omission of an anti-parallel Schottky diode for $\mathrm{S}_{\mathrm{F},1}$, which would compromise the reverse blocking capability.

[2] Note that the orientation of $\mathrm{S}_{\mathrm{F},1}$ is selected such that bootstrap gate drive power supplies can be employed, resulting in an asymmetric blocking capability with $V_{\mathrm{in,p}} >> V_{\mathrm{in,n}}$. To implement magnet quench protection, $V_{\mathrm{in,n}} >> V_{\mathrm{in,p}}$ is required to quickly ramp down the magnet current [5]: $\mathrm{S}_{\mathrm{F},1}$ could be flipped but an isolated gate drive interface would be needed.

[3] Even though a PSU based on 3S-TT phase modules requires three instead of two current leads, the overall much lower losses allow thinner cross sections and hence a clear system-level benefit results.

REFERENCES

[1] CERN, "Future circular collider study: Exploring concepts and technologies for the next generation of powerful particle colliders," accessed 2024-05-14. [Online]. Available: https://fcc.web.cern.ch/

[2] J. Kosse, M. Koratzinos, and B. Auchmann, "Reliability engineering of cryocooler-based HTS magnets for FCC-ee," *IEEE Trans. Appl. Supercond.*, vol. 34, no. 5, Aug. 2024.

[3] E. Coulinge, S. Pittet, and D. Dujic, "Design optimization of two-quadrant high-current low-voltage power supply," *IEEE Trans. Power Electron.*, vol. 35, no. 11, pp. 11 602–11 611, Nov. 2020.

[4] R. McFee, "Optimum input leads for cryogenic apparatus," *Rev. Sci. Instrum.*, vol. 30, no. 2, pp. 98–102, Feb. 1959.

[5] D. Cao, D. Zhang, J. W. Kolar, and J. Huber, "Conceptualization of a cryogenic 250-A power supply for high-temperature-superconducting (HTS) magnets of future particle accelerators," in *Proc. 11th Int. Conf. Power Electron (ICPE/ECCE Asia)*, Jeju, Korea, May 2023, pp. 688–696.

[6] A. Ballarino, "Current leads, links and buses," pp. 547–558, 2014, comments: 12 pages, contribution to the CAS-CERN Accelerator School: Superconductivity for Accelerators, Erice, Italy, 24 April - 4 May 2013, edited by R. Bailey. [Online]. Available: https://cds.cern.ch/record/1974072

[7] V. Parma, "Cryostat design," in *CAS-CERN Accelerator School: Superconductivity for Accelerators*, Erice, Italy, Apr. 2014, pp. 353–399. [Online]. Available: http://cds.cern.ch/record/1974062

[8] Y. Kondo, S. Fukano, A. Ninomiya, and T. Ishigohka, "Cryogenic low-voltage/high-current DC power source using multi-parallel-connected MOSFETs," *IEEE Trans. Appl. Supercond.*, vol. 19, no. 3, pp. 2337–2340, Jun. 2009.

[9] A. Elwakeel, N. McNeill, R. Peña-Alzola, M. Zhang, and W. Yuan, "Cryogenic DC/DC converter for superconducting magnet application," *IEEE Trans. Appl. Supercond.*, vol. 32, no. 6, Sep. 2022.

[10] H. Kawashima, T. Ito, and S. Sugimoto, "Power supply for superconducting magnets," Poster presented at the *Appl. Supercond. Conf. (ACS)*, Honolulu, HI, USA, Oct. 2022.

[11] J. K. Nøland, R. Mellerud, and C. Hartmann, "Next-generation cryo-electric hydrogen-powered aviation: A disruptive superconducting propulsion system cooled by onboard cryogenic fuels," *IEEE Ind. Electron. Mag.*, vol. 16, no. 4, pp. 6–15, Dec. 2022.

[12] Y. Zhang, X. Zhang, R. Zane, and D. Maksimovic, "Wide-bandwidth digital multi-phase controller," in *Proc. 37th IEEE Power Electron. Specialists Conf. (PESC)*, Jeju, Korea, Jun. 2006.

[13] J. Holtz, "Selbstgeführter Wechselrichter (in German)," German Patent 2 339 034C2, Jan., 1983.

[14] M. Schweizer and J. W. Kolar, "Design and implementation of a highly efficient three-level T-Type converter for low-voltage applications," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 899–907, Feb. 2013.

[15] T. Morita, M. Yanagihara, H. Ishida, Y. Uemoto, and M. Inoue, "Bidirectional switch and method for driving the same," US Patent US7 595 680B2, Sep., 2009.

[16] T. Morita, M. Yanagihara, H. Ishida, M. Hikita, K. Kaibara, H. Matsuo, Y. Uemoto, T. Ueda, T. Tanaka, and D. Ueda, "650 V 3.1 mΩcm^2 GaN-based monolithic bidirectional switch using normally-off gate injection transistor," in *Proc. IEEE Int. Electron. Dev. Meet. (IEDM)*, Washington, DC, USA, Dec. 2007, pp. 865–868.

[17] F. Vollmaier, N. Nain, J. Huber, J. W. Kolar, K. K. Leong, and B. Pandya, "Performance evaluation of future T-Type PFC rectifier and inverter systems with monolithic bidirectional 600V GaN switches," in *Proc. IEEE Energy Conv. Congr. Expo. (ECCE)*, Vancouver, Canada, Oct. 2021, pp. 5297–5304.

[18] Efficient Power Conversion Corporation, "EPC2302 datasheet." [Online]. Available: https://epc-co.com/epc/Portals/0/epc/documents/datasheets/EPC2302_datasheet.pdf

[19] A. Lidow, M. Rooij, J. Strydom, D. Reusch, and J. Glaser, *GaN transistors for efficient power conversion*, 3rd ed. Hoboken, NJ, USA: Wiley, Sep. 2019.