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***Abstract*—In recent years, driven by worldwide growing environmental awareness the research in power electronics was focusing on the development of highly efficient but mostly bulky converter systems e.g. for interfacing renewable energy to the grid. The GOOGLE Little Box Challenge was impulse to give the power density again more attention by motivating engineers worldwide to design a single-phase solar inverter system at the cutting edge of what is technically possible. In this paper a comparative evaluation of inverter concepts considered by a team of ETH Zurich, FH-IZM and Fraza company for the GOOGLE Little Box Challenge is given. Based on the lessons learned from the participation in the competition, for the considered inverter concepts the achievable efficiency, power density and the optimal modulation scheme are identified with a multi-objective $\eta\rho$-Pareto optimization. This provides a sound basis for the redesign of the existing system pushing the forefront of power density even further.**

I. Introduction

With the original objective to promote new technologies, the application of new materials, new integration concepts, advanced component designs and converter topologies, in September 2014 GOOGLE and IEEE launched the "Little Box Challenge" (LBC) a worldwide competition to build the world smallest 2kW single-phase solar-inverter in order to push the forefront of power density in today's converter systems further [1]. The most important inverter specifications of the LBC are given in **Table I**.

The Power Electronic Systems Laboratory (PES) at the ETH Zurich, in collaboration with the Fraunhofer Institut for Reliability and Microintegration (FH-IZM) and the Fraza company, has been selected as one of the 18 finalists, who presented their technical approaches on 21 Oct. 2015 and handed over the prototype to the National Renewable Energy Laboratory (NREL), Golden (Co), USA, for final testing. The winner of the grand prize of the $ 1 Million, whose inverter also passed the 100 hours testing, has been announced in Feb. 2016. The winning team achieved a power density of $8.72\,\mathrm{kW/dm^3}$ ($142.9\,\mathrm{W/in^3}$) which is - not surprisingly - only slightly higher than the power density of the converter system presented in this paper $8.18\,\mathrm{kW/dm^3}$ ($134\,\mathrm{W/in^3}$), since both teams were following the same technical approach.

Looking back without any exerting time pressure, the question has to be asked whether with the pragmatic and direct solution-oriented decision-making of the team of ETH the right concept was followed and how the optimal system would look like in a second attempt. This question should be answered in this paper. As a starting point of this analysis, in Section II the selected inverter concept is described in detail and the performance of the realized hardware prototype is evaluated by means of the achieved efficiency which is accompanied with a loss and volume distribution at full load. Based on the lessons learned, possible improvements are illustrated and discussed in Section III. Afterwards, in Section IV an alternative inverter topology is identified, which became possible due to late revisions of the LBC specifications. Accordingly, a turnaround to this inverter concept was not any more possible three weeks before a technical report had to be submitted. After a detailed analysis of the functionality of this topology, in Section V both inverter topologies are compared regarding achievable efficiency (η) and power density (ρ) based on a $\eta\rho$-Pareto optimization where also the optimal modulation scheme, PWM or Zero Voltage Switching (ZVS) Triangluar Current Mode(TCM) modulation, is identified. The paper is completed with a discussion of the optimization results, which provides a sound basis for the redesign of the existing system.

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TABLE I: Most important specifications given in the GOOGLE Little Box Challenge (LBC).

Parameter	*Requirement*
Input voltage source	$450\,\mathrm{V_{DC}}$ with $10\,\Omega$
Output voltage and frequency	$240\,\mathrm{V_{rms}}$ / $60\,\mathrm{Hz}$
Maximum output power	$2\,\mathrm{kVA}$ (Power factor $\pm 0.7 \ldots 1$)
Required power density	$> 3\,\mathrm{kW/dm^3}$ ($> 50\,\mathrm{W/in^3}$)
Minimum CEC weighted efficiency	$> 95\,\%$
Minimum lifetime	$> 100\,\mathrm{h}$
Max. ambient and case temperature	$30\,^\circ\mathrm{C}$ / $60\,^\circ\mathrm{C}$
Max. DC-side input current and voltage ripple	$20\,\%$ and $3\,\%$
Max. ground current	initially $5\,\mathrm{mA}$, changed to $50\,\mathrm{mA}$
Electromagnetic compliance	CISPR11 Class B

II. Realized Inverter System

In the first design phase the most suitable solar-inverter topology fulfilling all given specifications had to be identified (cf. **Table I**, [1]). Due to the initially specified low-frequency ground current of only $5\,\mathrm{mA}$, while considering the large earth capacitance of the DC power supply ($\approx 120-250\,\mathrm{nF}$) that emulated the PV-panels, for the inverter stage a full-bridge topology with two output phases was selected, where each output phase consisted of two interleaved bridge legs in buck-configuration (cf. **Fig. 1**). For the generation of the AC output voltage v_o the two phase voltages were actively controlled to values directly symmetric around half of the DC-link voltage $v_\mathrm{i}/2$, i.e. two sinusoidal voltages with only half the output voltage amplitude; thus only a DC but ideally no low-frequency Common-Mode (CM) output voltage component occured and no low-frequency ground currents were generated.

The promising properties of WBG semiconductor devices, such as improved switching performance with lower switching losses and lower on-state resistance per chip area compared to Si devices, are allowing for the achievement of higher power densities and higher

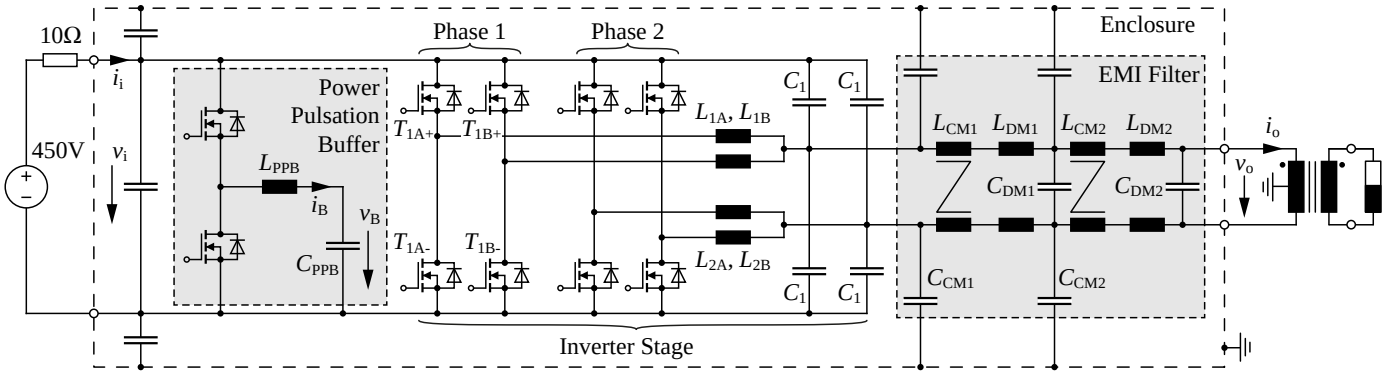


Fig. 1: Topology of the realized inverter consisting of two output phases, each of which is formed by two interleaved bridge legs in buck-configuration and a subsequent EMI output filter realized with two Common and Differential Mode (CM/DM) filter stages. The system DC-side energy storage is realized with an active Power Pulsation Buffer (PPB) [16].

efficiencies [2]–[5]. Therefore, new normally-off gallium nitride gate injection transistors (CoolGaN, Samples from Infineon, [6]) were used for the implementation of the four bridge legs, which were driven by a novel high-performance gate driver [7], [8]. In addition, each of the four bridge legs was operated with a TCM modulation scheme [9], [10] controlled with an FPGA, that enabled zero voltage switching and resonant switching transitions in all operating points.

In general, with the TCM modulation scheme a higher efficiency and power density are expected as compared to PWM, since the ZVS results in lower switching losses and accordingly the cooling effort/volume can be reduced. This also allows to select a rather high (variable) switching frequency in the range of 200 kHz-1 MHz resulting in a small volume of passive components, e.g. of the output inductors L_{1A}-L_{2B} (cf. **Fig. 1**). Furthermore, the high switching frequency in combination with the interleaving of the two bridge legs per output phase decreases the current ripple at the output capacitors C_1 and doubles the effective switching frequency, thus a higher cut-off frequency of the output filter can be selected, promoting an EMI filter of low volume.

In order to achieve a high attenuation while still keeping the filter components small, for the given circuit structure and selected frequency range a two-stage EMI output filter topology is employed as shown in **Fig. 1**. As can be noticed, although with the full-bridge topology ideally no low-frequency CM-voltage is generated at the inverter output, the CM-inductors L_{CM1} and L_{CM2} as well as the CM-capacitors C_{CM1} and C_{CM2} are still needed to filter the remaining switching frequency CM-components. Unfortunately, CM-inductors are one of the largest components in the EMI filter. However, in the given filter configuration the output capacitors C_1 not only help to attenuate the Differential Mode (DM) noise but also the CM-noise, which means that if C_1 is increased, the needed CM-inductance can be decreased. Furthermore, since C_1 is either connected to the positive or negative DC-rail and thus no ground currents are generated, C_1 can be designed in the µF-range which is much larger than the CM-capacitor values of C_{CM1} and C_{CM2} which are more in the tens of nF-range. The only limiting factor for the capacitance of C_1, and also for the other DM-capacitors C_{DM1} and C_{DM2}, is the additional reactive power drawn from the DC-side that causes larger currents and higher losses in the whole system. For the built prototype each C_1 is realized with four parallel and C_{DM1} and C_{DM2} with three parallel 2.2 µF 450 V X6S ceramic capacitors (C5750X6S2W225M250KA from EPCOS/TDK), since ceramic capacitors feature a much higher capacitance per unit volume than the conventionally used film capacitors. Considering the voltage- and temperature-dependent capacitance of the selected components, the effective capacitance drops to approximately 650 nF per piece which results in an additional reactive output filter power of around 200 Var. The CM-inductors L_{CM1} and L_{CM2} are built with toroidal cores from Vacuumschmelze which are based on the core material VITROPERM 500F that offers a high permeability and high saturation flux density (core type: T60006-L2012-W498, winding: 11 turns, 1 mm-Ø). Even if the leakage inductance of the CM-inductor contributes to the DM-inductance, separate DM-inductors L_{DM1} and L_{DM2} have to be added. For all DM-inductors the commercially available 10 µH-inductors from Coilcraft (XAL1010-103MED) are used.

As already mentioned, due to the rather high switching frequency the inductance value and/or the volume of the output inductor can be strongly reduced. However, a high switching frequency also demands for suitable core materials and sophisticated inductor design in order to keep the high frequency core and winding losses to a minimum. Addressing these challenges, the four output inductors are realized based on a novel type of multiple air gap multiple parallel foil winding inductor [12]–[15]. Since the multiple small air gaps are evenly distributed over the full length of the inner limb, the H-field in the winding window shows a quasi 1D field distribution running in parallel to the inner limb. Consequently, a foil winding enabling a high filling factor can be use, due to the fact that the H-field is also aligned with the foil winding and thus no eddy currents are induced in the copper. In order to counteract the skin effect at these high frequencies, the foil winding is realized with four parallel 20 µm thin copper foils which are mutually isolated with a 7 µm thin layer of Kapton. Furthermore, a sophisticated winding arrangement is used, which forces the current to flow evenly distributed in all four parallel copper layer, thus counteracting the proximity effect [12], [13]. The four output inductors of the built prototype are realized based on this approach, where N59 from EPCOS is used as high frequency core material. The inner limb of each output inductor has 24 air gaps surrounded by the four parallel copper foils with totally 16 turns, which gives an inductance value of 10 µH.

Due to the initially tight input current and voltage ripple criteria (cf. **Table I**, [1]), a conventional DC-link energy buffer realized with electrolytic capacitors would comprise the largest part of the overall inverter volume in order to eliminate the current and voltage ripple at twice the line frequency, i.e. at 120 Hz. Meeting the initial specifications, a capacitance value of at least 1.9 mF would be needed,

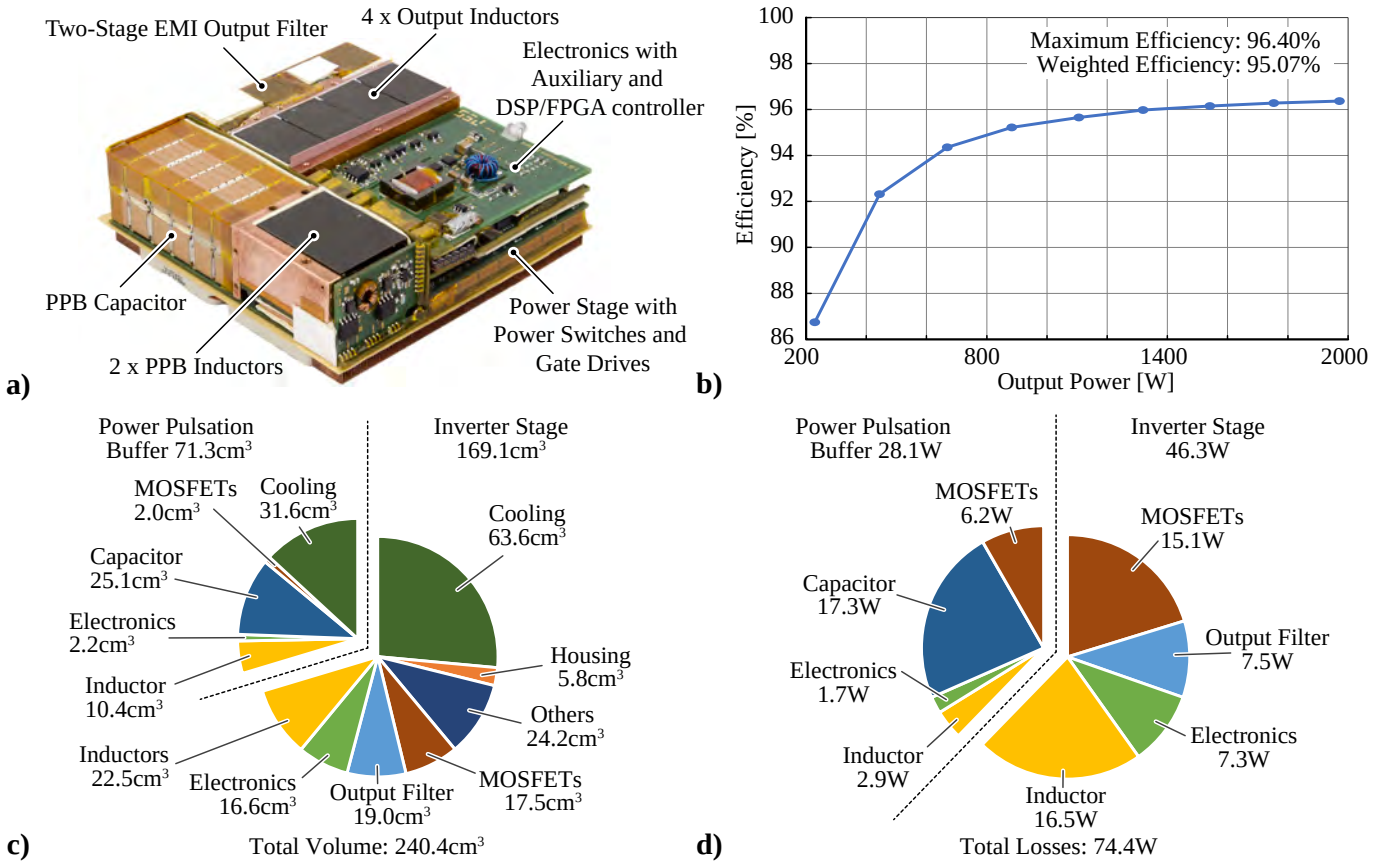
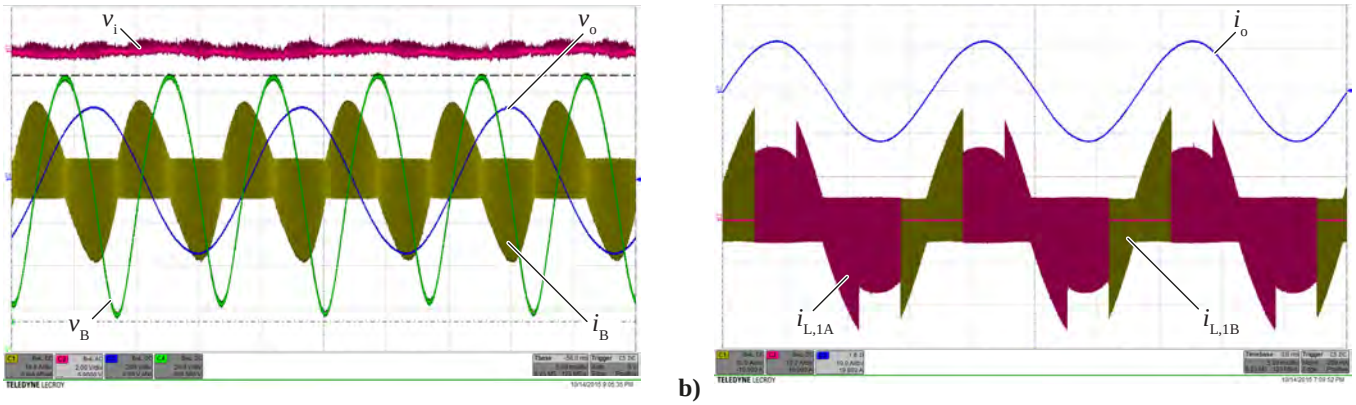


Fig. 2: a) Photograph of the realized hardware (without housing and top-side heat sink) presented by a team of ETH Zurich (PES), FH-IZM, and Fraza company, at the finals of the GOOGLE Little Box Challenge ($3\,\mathrm{cm}$ x $8.8\,\mathrm{cm}$ x $8.9\,\mathrm{cm}$), **b)** measured efficiency dependency on the output power, **c)** corresponding volume distribution and **d)** loss distribution.

which in case of e.g. four high density electrolytic bulk capacitors ($493\,\mu\mathrm{F}$, $450\,\mathrm{V}$, B43991-X0009-A223 from EPCOS/TDK) would result in a boxed volume of $126\,\mathrm{cm}^3$. The reason is that the energy fluctuations of the bulk capacitor due to the low admissible voltage ripple are only marginal compared to the total stored energy, i.e. the capacitor basically remains fully charged and its energy storage capacity is hardly utilized. Therefore, the DC-link capacitors are substituted by an active buck-type power pulsation buffer (PPB) [16] (cf. **Fig. 1**) including the proposed control scheme in [18]. The PPB largely compensates the AC component of the sinusoidally varying load power by storing/releasing the energy in/from the capacitor C_{PPB} which, in contrast to electrolytic capacitors, is charged and discharged to a significant extent (cf. **Fig. 3 a)**). Accordingly, for C_{PPB} a much smaller capacitance value is required which allows to reduce the total volume of the DC link energy storage even though additional semiconductors, an inductor L_{PPB} and auxiliary circuits are needed. In order to meet the high RMS-current requirement and energy storage capacity at minimum volume, a novel ceramic capacitor technology (CeraLink from EPCOS/TDK) is used for C_{PPB} and C_{DC} [16], [17], where C_{DC} ($10\,\mu\mathrm{F}$) is only needed to filter the high switching frequency ripple. The semiconductors, the type of inductor L_{PPB} ($20\,\mu\mathrm{H}$; i.e. 2 inductors of $10\,\mu\mathrm{H}$ connected in series) and the modulation scheme (TCM) are identical to the inverter stage.

With TCM operation, a further important circuit part is the Zero Crossing Detection (ZCD) circuit, which detects the zero crossing of the TCM inductor current and thus enables a proper control of the inductor current and the interleaving of the bridge-legs. Different concepts such as current measurement with a shunt, current transformer, hall element, Giant Magneto-Resistive (GMR) sensors, measurement of the MOSFET's on-state resistance $R_{\mathrm{ds,on}}$, and a saturable inductor have been analyzed for the realization of the ZCD circuit. For the sake of brevity a detailed discussion of these concepts has to be omitted here, but it can be stated that, as presented in [11], with the saturable inductor the best performance is achieved, which features isolation, low complexity, and a high Signal-to-Noise Ratio (SNR) and proper operation up to high frequencies ($2-3\,\mathrm{MHz}$). In order to saturate the core already at low currents (close to the current zero crossings), a core material with a high permeability and a core shape without air gap should be selected. Furthermore, the core volume should be as small as possible to keep the core losses to a minimum. Therefore, a small toroidal core (no air gap) with an outer diameter of $4\,\mathrm{mm}$ (R4 x 2.4 x 1.6, B64290P0036X830 from EPCOS) is used. The selected core material is N30 which features a low saturation flux density and high permeability over a wide frequency range. The number of turns of the secondary (measurement) winding is set to $N_{\mathrm{s}} = 10$. Depending on the current slope ($\mathrm{d}i/\mathrm{d}t$), with this number of turns the induced voltage reaches values from $20\,\mathrm{V}$ up to $160\,\mathrm{V}$, which make the ZCD circuit robust against electric disturbances, however, with the variable induced voltage also the time delay of the detection of the current crossings slightly changes. The induced voltage is tracked with a fast comparator (TLV3501, $4.5\,\mathrm{ns}$ propagation delay) in order to keep the signal delay short. The digital output signal of the comparator is then digitally filtered and used for the TCM state



a) **b)**

Fig. 3: a) DC input voltage v_i (2 V/div, AC-coupled), generated AC voltage v_o (200 V/div), PPB capacitor voltage v_B (20 V/div), and TCM current i_B in the PPB inductor (10 A/div), **b)** output current i_o (10 A/div) and corresponding TCM currents $i_{\mathrm{L,1A}}$, $i_{\mathrm{L,1B}}$ (10 A/div) in the interleaved half-bridges of one output phase, whereas in the vicinity of the current zero-crossings only a single bridge-leg is operated alternatingly (4D-interleaving [25]).

machine implemented in the FPGA (200 MHz clock) resulting in an overall propagation delay of around 20 ns.

In **Fig. 2** a picture of the built hardware prototype with an overall volume of 240.4 cm^3 (inverter stage: 144.9 cm^3, PPB: 95.5 cm^3) and the achieved performance are shown. With the total losses of 74.4 W (inverter stage: 46.3 W, PPB: 28.1 W) at full output power a maximum efficiency of 96.4 % is obtained. At low load power the efficiency strongly drops, thus the CEC weighted efficiency of 95.07 % is only slightly above the required 95 %. The reasons for this are discussed in the following section, but with the given volume and loss distribution at full output power, the lossy components can already be determined. As can be noticed, the passive components such as the inductors and the PPB-capacitor, which together generate 36.7 W of losses, mainly contribute to the overall converter losses (49 %). In addition to their total volume of 58 cm^3 (24 %), the passive components also strongly affect the needed heat sink volume of 95.2 cm^3 (39.6 %), which can be calculated based on the achieved overall Cooling System Performance Index (CSPI, [19]) of 25 $\mathrm{W}/(\mathrm{K}\cdot\mathrm{dm}^3)$ and the maximum heat sink temperature difference of 30 °C.

III. Measures for Performance Improvements

Based on the above given description of the system presented in the finals of the GOOGLE LBC, measures for further performance improvements are discussed in the following.

A. Capacitor Technology of PPB

The capacitor of the PPB, which generates 61.5 % of the PPB losses and 23.2 % of the overall converter losses, has been realized with 120 x 2 µF 500 V CeraLink capacitors from EPCOS/TDK (size: 8.5 mm x 9.2 mm x 2.6 mm). Beneficially, these ceramic capacitors can be operated with much larger current ripples than electrolytic capacitors and in addition feature a high capacitance density (≈ 10 $\mu\mathrm{F}/\mathrm{cm}^3$) which in contrast to other ceramics even increases with voltage and/or temperature and reaches its maximum at around 375 V and 80 °C [17]. Furthermore, the capacitors are available in compact 20 µF or even custom-made blocks making the system assembly much easier and ensuring higher reliability. Thus, it was obvious to utilize these capacitor, however, it turned out that these capacitors are well suited for high-frequency DC applications but generate high losses in low-frequency AC applications like in the PPB or the inverter output filter. As shown in [17], with the X6S 2.2 µF 450 V ceramic capacitor (C5750X6S2W225M250KA also from EPCOS/TDK) the capacitor losses can be strongly reduced to around 2.1 W, while the capacitor volume only slightly increases by ≈ 2 cm^3 but the corresponding heat sink volume reduces by ≈ 20 cm^3! Consequently, the X6S capacitors are the most suitable alternative to the CeraLink capacitors and will be used for the $\eta\rho$-Pareto optimization performed later in this paper. For the sake of completeness, it should be noted that these capacitors are only available as single 2.2 µF chip capacitors (for the given PPB specifications the effective capacitance reduces to 700 nF). Thus, a large number of chip capacitors has to be soldered on a PCB which on the one hand increases the volume and on the other hand reduces the system reliability.

B. Core Losses in Multiple Air Gap Inductor

Besides the PPB capacitor also the multiple air gap inductors showed higher losses than expected, which finally could be localized in the core material. It turned out that the cutting of the ferrite, which is needed to insert the multiple air gaps, introduces mechanical stresses in the surface and significantly increases the core losses as described in [20]–[22]. This was also proven by comparing the core losses measured with a bulk and a sliced ferrite sample at the same flux density and frequency. These additional losses can slightly be reduced by polishing or etching, but at the moment cannot be quantitatively describe and are subject of research. Therefore, the subsequent Pareto optimization only considers conventional inductor designs using different commercially available core types and a litz wire winding.

C. Soft-Switching Losses and Minimum Charging Current

In order to calculate the switching losses of the built inverter prototype, the soft-switching losses of the employed GaN GIT switches (CoolGaN, Samples from Infineon) were calorimetrically measured for different peak currents; as presented in [7], for the selected switching frequency range the soft-switching turn-off losses are not any more negligible. Possible causes for these losses are the high internal gate resistance, which inhibits a fast turn-off of the GIT channel thus overlapping of the GIT's drain-source-voltage and the current in the GIT channel occurs, or the nonideality of the GIT's output capacitance, which generates losses during the dead time

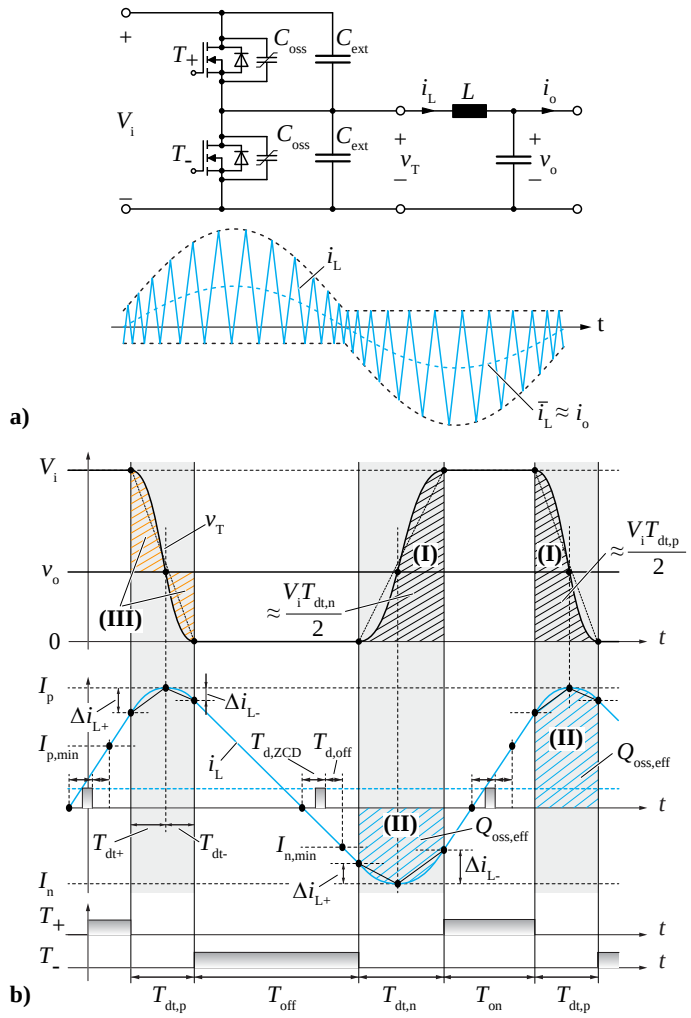


Fig. 4: Detailed explanation of challenges with defining the switching instances of the TCM modulation considering time delays of the ZCD and the gate drives ($T_{\mathrm{d,ZCD}}$, $T_{\mathrm{d,off}}$), **a)** bridge-leg with external capacitors C_{ext} placed in parallel to the MOSFETs in order to reduce the switching losses [7], **b)** detailed analysis of one TCM switching cycle.

interval when the output capacitance is charged and discharged [23], [24]. The answer to this question is also subject of current research. Nevertheless, as shown in [7], by adding an external capacitance (up to $C_{\mathrm{ext}} = 600\,\mathrm{pF}$) in parallel to the high and low-side GITs (charge equivalent paracitic output capacitance $C_{\mathrm{oss,Qeq}} = 114\,\mathrm{pF}$), which strongly increases the effective output capacitance $C_{\mathrm{oss,eff}} = C_{\mathrm{oss,Qeq}} + C_{\mathrm{ext}}$, allows to reduce the turn-off losses by around 30 % (cf. **Fig. 4 a)**). However, due to the higher effective output capacitance $C_{\mathrm{oss,eff}}$, now for the soft-switching transient a higher amount of charge $Q_{\mathrm{oss,eff}}$ is needed to charge/discharge the GIT output capacitances $C_{\mathrm{oss,eff}}$ [10] (cf. **(II)** in **Fig. 4 b)**). This means that with the same charging current the positive and negative dead time intervals $T_{\mathrm{dt,p}}$ and $T_{\mathrm{dt,n}}$ have to be increased and are consuming an appreciable part of a switching cycle at high switching frequencies (cf. **Fig. 4 b)**); e.g. charging the effective output capacitances of the high and low-side switches of $2{\cdot}C_{\mathrm{oss,eff}} = 2{\cdot}(114\,\mathrm{pF}{+}600\,\mathrm{pF})$ with an already large charging current of 5 A from 0 V to 400 V and vice versa, results in a dead time of $T_{\mathrm{dt}} \approx 125\,\mathrm{ns}$, which for both switching transitions is 25 % of a 1 MHz switching cycle. Furthermore, during the dead time intervals $T_{\mathrm{dt,p}}$ and $T_{\mathrm{dt,n}}$ additional voltage-time areas are applied to the TCM inductor L (cf. **(I)** in **Fig. 4 b)**), which by assuming in a first approximation a linear increase/decrease of v_{T} can be easily calculated as $V_{\mathrm{i}}T_{\mathrm{dt,x}}/2$. Consequently, this means that even if the on-time T_{on} of the power transistor is reduced to zero, during the dead time intervals a certain minimum voltage v_{T} is applied to the inductor. Similarly, if the off-time T_{off} is reduced to zero, during the dead times a certain voltage-time area is missing, thus increasing $T_{\mathrm{dt,p}}$ and $T_{\mathrm{dt,n}}$ results in a limitation of the output voltage range V_{o}, i.e. the minimum and maximum achievable output voltages of a bridge leg are more and more restricted around $V_{\mathrm{i}}/2$. Based on the specifications, however, the minimum output voltage range is defined to $V_{\mathrm{o}} = 30\,\mathrm{V}...370\,\mathrm{V}$ at $V_{\mathrm{i}} = 400\,\mathrm{V}$, which means that a certain minimum charging current I_{p} or I_{n} is needed to keep $T_{\mathrm{dt,p}}$ or $T_{\mathrm{dt,n}}$ below a maximum admissible value. Accordingly, the additional external capacitor C_{ext} increases the minimum charging and RMS currents, and thus leads to higher conduction losses in all components, which could finally again compensate the gained reduction in switching losses. Therefore, the optimal C_{ext} has to be found in a Pareto optimization in Section V.

D. Time Delays of ZCD Circuit and Gate Drives

Furthermore, the minimum charging current I_{p} or I_{n} is not only determined by C_{ext} but also by the propagation delay $T_{\mathrm{d,ZCD}}$ of the ZCD-circuit and the turn-off delay $T_{\mathrm{d,off}}$ introduced by the signal isolator and the gate driver. As one can imagine, due to $T_{\mathrm{d,ZCD}}$ and $T_{\mathrm{d,off}}$ the TCM controller cannot immediately react on the effective zero crossing event and hence defines the minimum on- or off-time only after the current zero crossing to $T_{\mathrm{on/off,min}} = T_{\mathrm{d,ZCD}} + T_{\mathrm{d,off}}$ (cf. **Fig. 4 b)**). Accordingly, during $T_{\mathrm{on/off,min}}$ the TCM current can already quickly increase depending on the applied voltages and selected inductance value, which defines the minimum switched current $I_{\mathrm{p,min}}$ or $I_{\mathrm{n,min}}$. In the built prototype, for example, the minimum on- or off-time is $T_{\mathrm{on/off,min}} = 20\,\mathrm{ns} + 30\,\mathrm{ns} = 50\,\mathrm{ns}$ which in combination with the highest voltage applied to the inductor of 395 V and an inductance of 10 µH results in an minimum switched current of $I_{\mathrm{p,min}} = -I_{\mathrm{n,min}} \approx 2\,\mathrm{A}$. However, during the dead times $T_{\mathrm{dt,p}}$ and $T_{\mathrm{dt,n}}$ the inductor current i_{L} further increases in a resonant manner, thus I_{p} and I_{n} can reach much larger values than $I_{\mathrm{p,min}}$ and $I_{\mathrm{n,min}}$. In **Fig. 4 b)** this is exemplarily illustrated for a positive inductor current i_L. As long as v_T is larger than v_o, a positive voltage-time area is applied to the inductor (cf. **(III)** in **Fig. 4 b)**), which results in an further increase of the inductor current by $\Delta i_{\mathrm{L+}}$. Again, assuming a linear voltage slope of v_{T}, the voltage-time area can easily be calculated as $1/2{\cdot}(V_{\mathrm{i}}{-}v_{\mathrm{o}}){\cdot}T_{\mathrm{dt+}}$, where $T_{\mathrm{dt+}} = T_{\mathrm{dt}}{\cdot}(V_{\mathrm{i}}{-}v_{\mathrm{o}})/V_{\mathrm{i}}$, thus leads to $\Delta i_{\mathrm{L+}} = 1/2 \cdot (V_{\mathrm{i}} - v_{\mathrm{o}})^2 \cdot T_{\mathrm{dt}}/(V_{\mathrm{i}} \cdot L)$. As can be noticed, compared to the on-state interval T_{on}, during the interval $T_{\mathrm{dt+}}$ only half the voltage-time area is applied to the inductor, which consequently results in an average current slope which is half the current slope during T_{on}. The resulting peak current is then $I_{\mathrm{p}} = I_{\mathrm{p,min}} + \Delta i_{\mathrm{L+}}$, which for the designed LBC prototype reaches values of $I_{\mathrm{p}} = -I_{\mathrm{n}} \approx 4 - 6\,\mathrm{A}$.

For sake of completeness, as soon as v_{T} falls below v_o, the inductor current starts to decrease, and in analogy to $\Delta i_{\mathrm{L+}}$, the change of the inductor current during $T_{\mathrm{dt-}}$ can again be calculated based on the voltage-time area $1/2 \cdot v_{\mathrm{o}} \cdot T_{\mathrm{dt-}}$, where $T_{\mathrm{dt-}} = T_{\mathrm{dt}} \cdot v_{\mathrm{o}}/v_{\mathrm{o}}$, to $\Delta i_{\mathrm{L-}} = 1/2 \cdot v_{\mathrm{o}}^2 \cdot T_{\mathrm{dt}}/(V_{\mathrm{i}} \cdot L)$ (cf. **(III)** in **Fig. 4 b)**). Furthermore, with the calculated values I_{p}, $\Delta i_{\mathrm{L+}}$, $\Delta i_{\mathrm{L-}}$, $T_{\mathrm{dt+}}$, and $T_{\mathrm{dt-}}$ the current-time area (cf. **(II)** in **Fig. 4 b)**) during the dead time can be approximately calculated, which actually equals the output charge

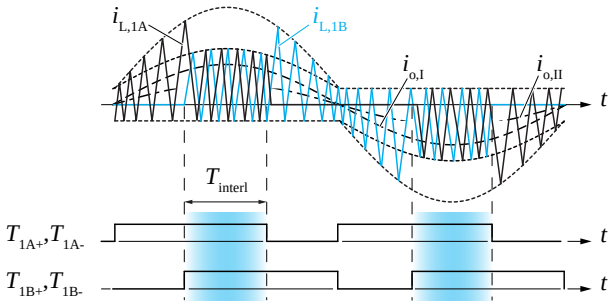


Fig. 5: Schematic current waveforms for the implemented 4D-Interleaving [25] in order to improve the converter efficiency, especially in the part load range. The duration T_{interl} of the time intervals in which both bridge-legs are interleaved, is adjusted depending on the actual output power.

$Q_{\mathrm{oss,eff}}$ of two transistors and external capacitors. If e.g. $Q_{\mathrm{oss,eff}}$ is known from measurements, one could also calculate in reverse direction in order to find all timings and current values, which is finally needed for a proper control of the TCM current.

E. 4D-Interleaving of Bridge Legs

Nevertheless, since certain values of $T_{\mathrm{d,ZCD}}$ and $T_{\mathrm{d,off}}$ are occurring in the prototype, all half-bridges are conducting a higher current than ideally expected, and it becomes clear that a permanent interleaving of two bridge-legs is no more attractive. Therefore, in order to (at least) slightly compensate the higher conduction losses and thus increase again the converter efficiency, the so-called 4D-Interleaving is implemented, which means that the individual half-bridges are only interleaved around the peak values of the output current (the TCM output current is then equally shared between the two bridge-legs) and in the vicinity of the current zero crossings only a single bridge-leg is operated alternatingly (the single bridge-leg has then to carry the total TCM output current) as schematically shown in **Fig. 5** [25]. The corresponding measured current waveforms are shown in **Fig. 3 b)**. At an output power of $1\,\mathrm{kW}$, for example, compared to continuous interleaving with the 4D-Interleaving in sections the losses can be reduced by $10\,\mathrm{W}$, which is an efficiency improvement of $1\,\%$ at this output power.

F. Conventional PWM Modulation with large Current Ripple

Alternatively, in order to reduce the influence of C_{ext} and $T_{\mathrm{on/off,min}}$ on $I_{\mathrm{p,min}}/I_{\mathrm{n,min}}$, a lower switching frequency could be selected. This is only possible by increasing the inductance value of the output inductor. The TCM peak current, however, is independent of the selected inductance and is always larger than twice the local average current within one switching interval. As a rule of thumb, assuming that the inductor volume scales proportionally with the stored magnetic energy $1/2LI_{\mathrm{p}}^2$, a reduction of the switching frequency would lead to a lower power density which in this case is not desired. In contrast to TCM, with conventional PWM modulation an increase of the inductance value would directly result in a decrease of the current ripple and the resulting peak current, which means that with PWM modulation the inductor volume doesn't dependent so strongly on the inductance value/switching frequency and therefore a compact design could also be feasible. Furthermore, based on the preceding considerations, with TCM the large current ripple and high RMS currents at high switching frequencies lead to much higher conduction losses reducing the advantage of soft-switching gained

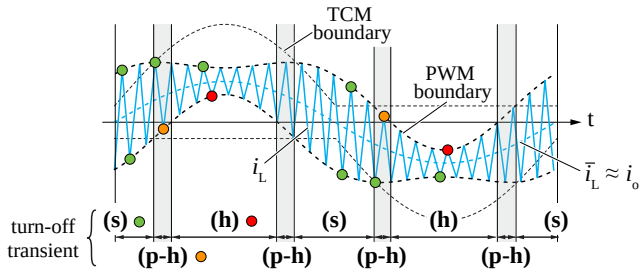


Fig. 6: Schematic inductor current waveform for PWM modulation if a rather small inductor value is selected. Due to the high current ripple, around the current zero crossings soft-switching **(s)** or at least partial hard-switching **(p-h)** can be achieved during turn-on. Hard-switching **(h)** only occurs if the lower current boundary gets positive. During turn-off always soft-switching is achieved.

by TCM modulation. Therefore, the question arises, whether with conventional PWM modulation the same or even a better performance can be achieved, although PWM suffers from turn-on switching losses. However, this major drawback of PWM is mitigated by the fact that with a relatively high current ripple also for PWM the turn-on switching losses can be strongly reduced (cf. **Fig. 6**). As can be noticed, due to the high current ripple, around the current zero crossings even with PWM soft-switching during turn-on and turn-off can be achieved as long as the switched current is sufficiently negative to fully charge/discharge the parasitic output capacitances of the half-bridge (cf. **(s)** in **Fig. 6**). If the switched current is still negative, but not large enough to provide $Q_{\mathrm{oss,eff}}$ during the dead times, partial hard switching occurs during turn-on (cf. **(p-h)** in **Fig. 6**). However, this still causes much lower turn-on switching losses than full hard-switching, since on the one hand C_{oss} is already charged to a certain voltage, which means that the anti-parallel diode of the switch which turned-off is already blocking (no reverse recovery) and on the other hand C_{oss} strongly decreases with voltage, thus the switching energy provided from the DC-link to further charge C_{oss} to V_i is smaller [26]. As soon as the lower current envelope gets positive, hard switching occurs during turn-on, while during turn-off always soft-switching is achieved. However, since the current ripple is high, the switched current is well below the average current $\bar{i}_{\mathrm{L}}$, thus lower turn-on losses occur. Consequently, since based on theses considerations TCM modulation has no longer immediate significant advantages over PWM modulation, in the Pareto optimization of section V both modulation schemes are considered and compared to each other.

IV. DC-|AC| Buck Converter & Unfolder

In the late stage of the competition, GOOGLE revised the maximum ground current from $5\,\mathrm{mA}$ to $50\,\mathrm{mA}$, thus immediately the suppression of a low-frequency CM-output voltage was no longer an issue and the high-frequency full-bridge topology was no longer the optimal choice to achieve highest power density. An alternative inverter topology based on a conventional buck converter and a subsequent low-frequency full-bridge unfolder, whose output is not free of low-frequency CM-voltage, was then identified as advantageous (cf. **Fig. 7**, [27]). However, a changing to this inverter topology was not any more possible until the LBC submission deadline, but, is now considered and evaluated in the Pareto optimization. The major advantage of this topology is that one half of the previously described inverter stage including output inductors and capacitors can be omitted, thus volume and losses can be saved and the

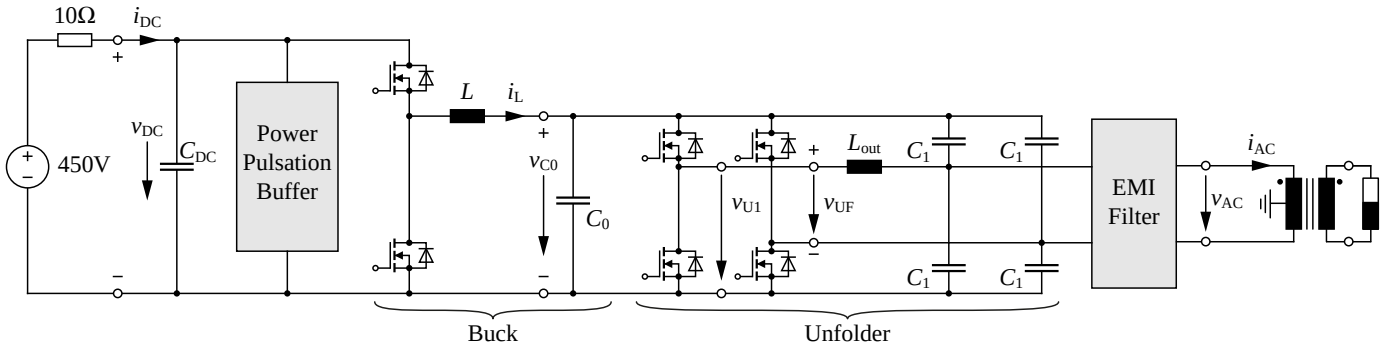


Fig. 7: Inverter topology based on a conventional buck converter and a subsequent low-frequency full-bridge unfolder.

system complexity can be reduced. The resulting buck stage, operated either with TCM or PWM, generates a rectified sinusoidal voltage $v_{C0} = |\hat{V}_o \cdot \sin(\omega t)|$ with respect to the negative DC-link bus, which is then unfolded to a sinusoidal output voltage v_{UF} by a subsequent low-frequency full-bridge (cf. **Fig. 7**). Considering a reversed power flow direction, one can noticed that this topology actually corresponds to the well-known conventional PFC Boost rectifier [28], where the input diode bridge is substituted by an active full-bridge. Since the full-bridge only generates conduction losses, MOSFETs with a low on-state resistance can be selected. Assuming that for the 60 Hz isolation transformer, connected to the output of the inverter (cf. **Fig. 7**), a center-tapped configuration is used (e.g. found in a North American households), a sinusoidal low-frequency CM-voltage with a peak voltage equal to half the output voltage amplitude is generated, i.e. $v_{CM} = \hat{V}_o/2 \cdot \sin(\omega t)$. Thus, for the revised specification a incredibly high total CM-capacitance of 1.1 µF would be allowed, which is much higher than the earth capacitance introduced by the DC power supply emulating the PV-panels.

If it is assumed that the buck stage is operated with TCM modulation, the previously mentioned problem arises that depending on the dead time duration $T_{dt,p}$ or $T_{dt,n}$ the output voltage cannot be controlled below a certain minimum output voltage $V_{C0,min}$, which means that a rectified sinusoidal voltage v_{C0} cannot be generated. This is actually also true for PWM if the interlocking delay would become a dominant part of the switching period. To overcome this problem, in [29] a new control scheme is proposed where the output voltage of the buck stage v_{C0} still follows the rectified output voltage reference $v_{C0,ref}$ until $v_{C0,ref}$ falls below $V_{C0,min}$. In the time interval where $v_{C0,ref} < V_{C0,min}$, the buck output voltage is kept constant at $V_{C0,min}$ and the unfolder is operated with high frequency PWM in such a way that v_{UF} follows the output reference $v_{C0,ref}$ (cf. **Fig. 8**). Typically, the time interval in which the full-bridge is operated with PWM is short compared to the mains period. In addition, the switched voltage is low (= $V_{C0,min}$), thus the switching losses of the full-bridge can be neglected. For the PWM modulation of the full-bridge different strategies can be followed. Either both bridges are switched at the same time with the same duty cycle but inverse polarity (cf. **Fig. 8 a)**) or only one bridge is operated with PWM and the other bridge leg clamps its switch node either to the positive or negative rail (cf. **Fig. 8 b)**). In **Fig. 9** the measured waveforms corresponding to the first modulation strategy at an output power of 1 kW are shown. The later modulation strategy generates only half the switching losses and since the voltage amplitude of the high frequency voltage v_{UF} is halved, this modulation strategy is also beneficial concerning emitted EMI noise. Nevertheless, since with the PWM modulation of the unfolder additional EMI noise is emitted, which mainly defines the needed output filter attenuation, interleaving of several buck stages or selecting a large capacitor C_0 is not reasonable. On the other hand, an additional output inductor at the output of the full-bridge is required, which, however, in case of a high switching frequency and a low $V_{C0,min}$ can be small. The rest of the EMI filter structure is equal to the one of the realized system (cf. **Fig. 1**).

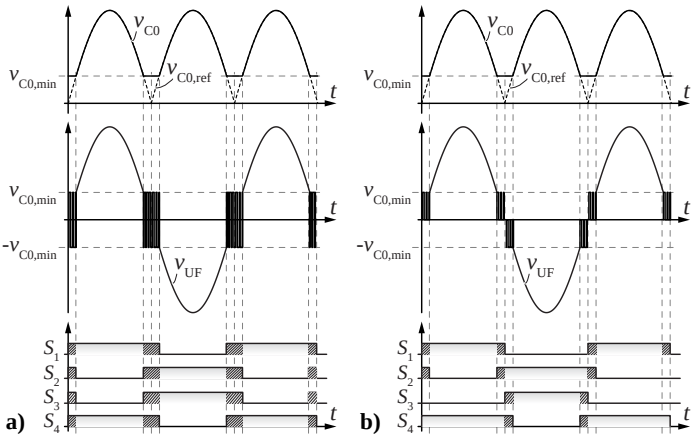


Fig. 8: Modulation strategies of the proposed control scheme where **a)** either both bridge legs are switched or **b)** only one bridge leg is operated with PWM and the other bridge leg is clamped.

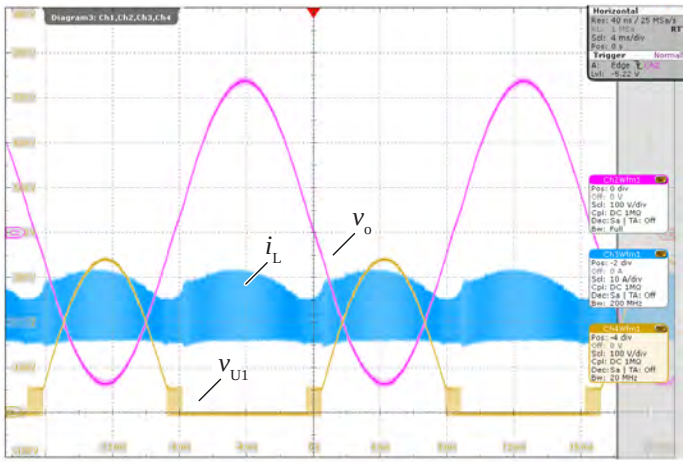


Fig. 9: Measured waveforms of the proposed modulation strategy for the DC-|AC| Buck Converter & Unfolder of Fig.7 at an output power of 1 kW. Inductor current i_L (10 A/div), bridge-leg voltage v_{U1} (100 V/div) and output voltage v_o (100 V/div).

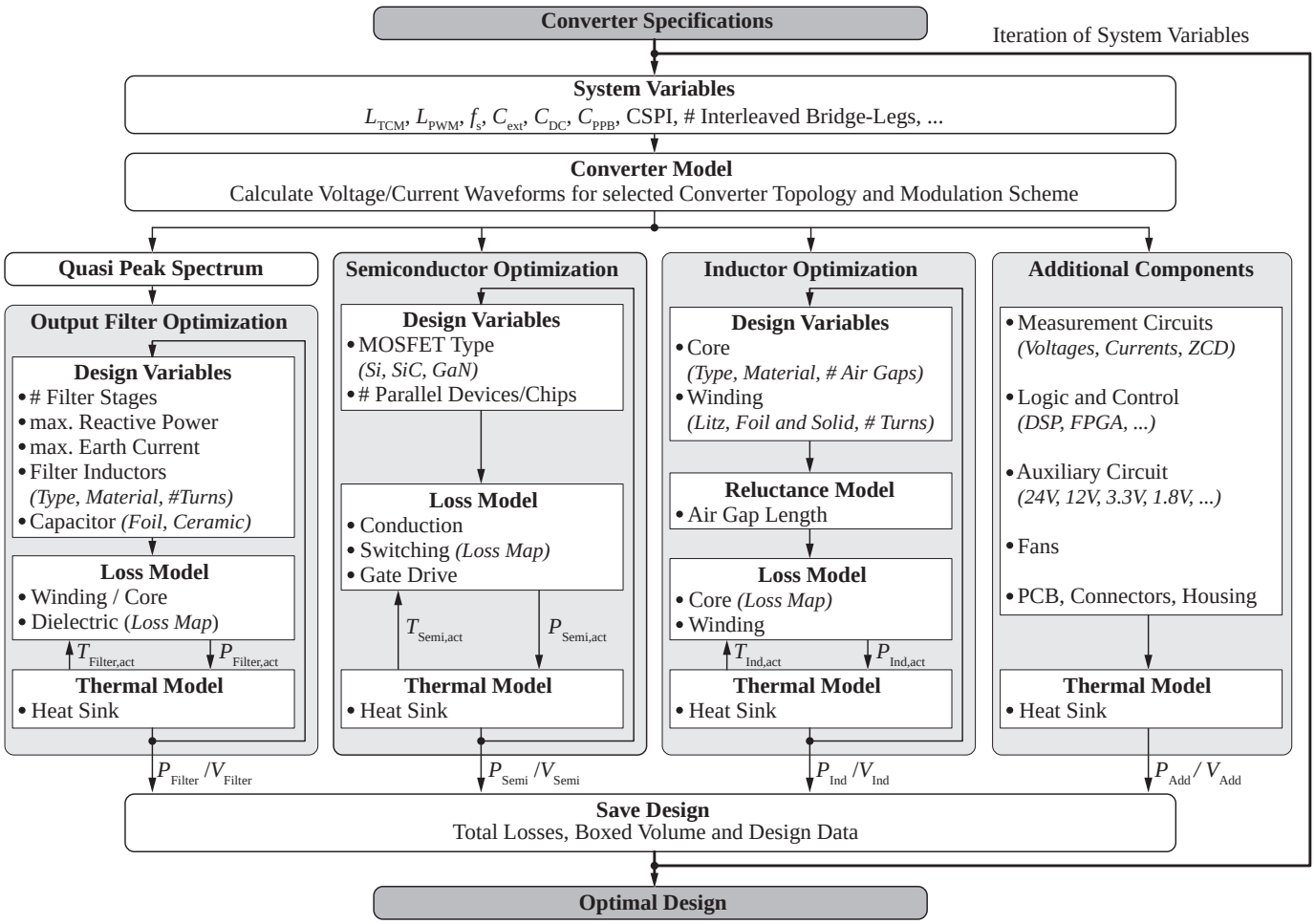


Fig. 10: Flow chart of the ηρ-Pareto optimization procedure.

Another advantage of the proposed operation mode is that there is always a certain minimum voltage v_{C0} available. This enables a proper control of the output current e.g. during transients such as load steps or for reactive loads (power factor of $\pm$0.7...1), where the output voltage and current are not in phase and during the voltage zero crossing the current has to be either increased or decreased [30]. Furthermore, it has to be mentioned, that this modulation strategy is also applicable to PFC rectifiers enabling reactive power compensation.

V. ηρ-Pareto Optimization

In the following the ηρ-Pareto optimization procedure of the inverter system is described with respect to efficiency (η) and power density (ρ). Since the optimization of the PPB can be performed separately [16], in this paper only the optimization procedure of the output stage is presented. However, the Pareto fronts and the system designs with highest power density derived in this paper, also include the losses and volume of the optimal PPB, which are determined as described in [16]. The only interface (common variable) between the output stage and PPB optimization procedure is the additional reactive power consumption of the output filter. This means that the PPB not only delivers the 120 Hz AC-power component of the load, but also the additional reactive (capacitive) power drawn from the output filter, which actually depends on the output filter design, namely the value of the DM-capacitors. Due to the vectorial addition of these two power components, the critical operating point of the whole system is given for capacitive load.

In the ηρ-Pareto optimization all available degrees of freedom, i.e all design space variables, are considered for both topologies and modulation schemes (cf. **Fig. 10**). For the full-bridge topology with TCM modulation, for example, the number of interleaved bridge-legs, the number of parallel GIT devices/chips per switch, the external capacitance C_{ext}, the output inductor value L and the output capacitor C_1 can be iterated, while with PWM modulation additionally the switching frequency f_{s} can be selected independently in a certain range. Based on the selected inverter topology, modulation scheme and design space parameters, the resulting current and voltage waveforms are calculated for each component, which then are used to optimize the semiconductors, the output inductors and the output filter, while additional circuit components such as the measurement and control circuit or the auxiliary supply are also considered (cf. **Fig. 10**). There, each component is optimized independently with an iterative temperature/loss calculation, in order to take the temperature dependent losses into account. For the calculation of the semiconductor losses, which consist of conduction, switching and gate drive losses, for example, the conduction losses are calculated based on the temperature and current-dependent on-state resistance $R_{\mathrm{ds,on}}$ given in the manufacturer's datasheet; for the switching losses a loss map obtained from switching loss measurements [7] is used. For the design of the output inductor, different core shapes with different core materials and air gap sizes as well as different winding types, such as

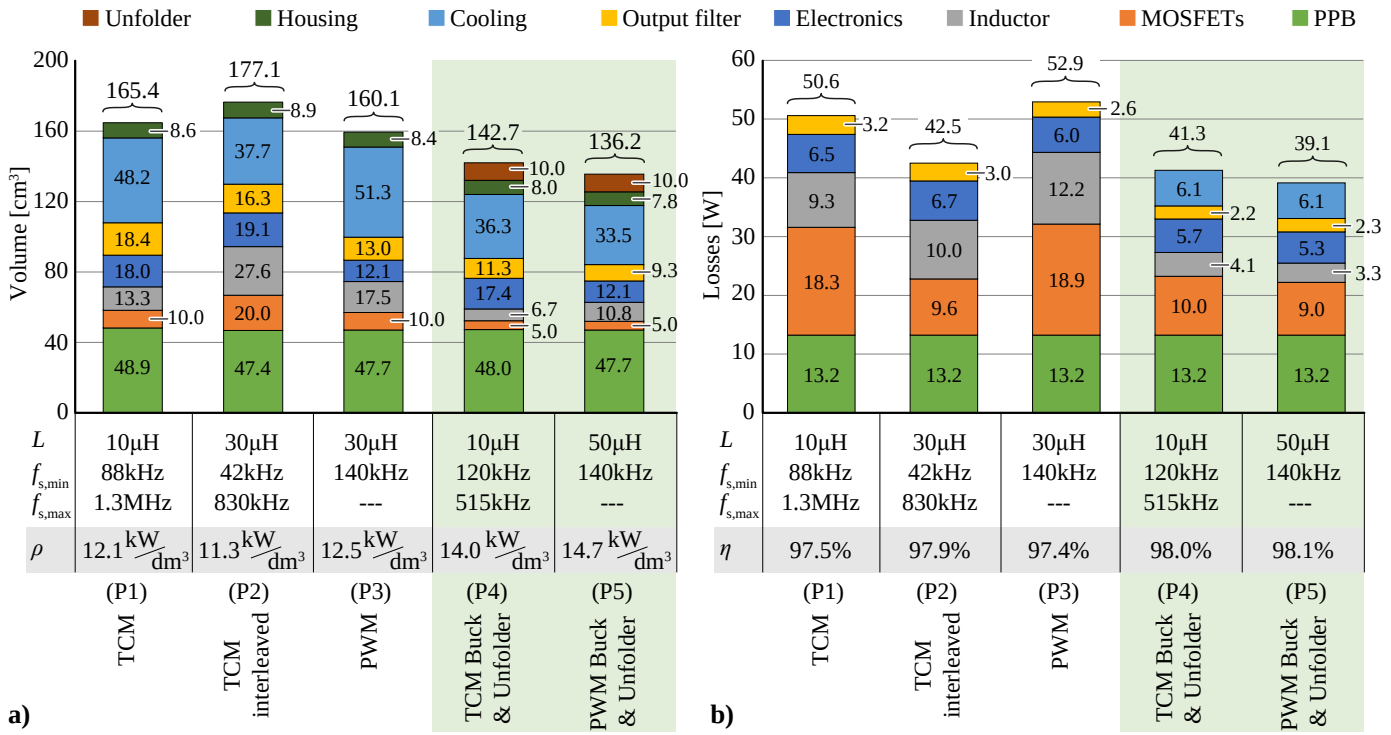


Fig. 11: a) Volume distribution and **b)** loss distribution of all designs achieving the respective highest power density (P1-P5).

litz, foil or solid wire with different winding numbers, are considered, while the optimal inductor design is again determined by calculating the losses and temperatures of the core and the winding iteratively. Similarly, after calculating the quasi peak noise spectrum, the optimal EMI output filter is found by searching through all parameters for the CM/DM-inductors and CM/DM-capacitors. For example, with the iteration of the reactive power consumption of the output filter, the maximum total DM-capacitance can be directly calculated and thus,

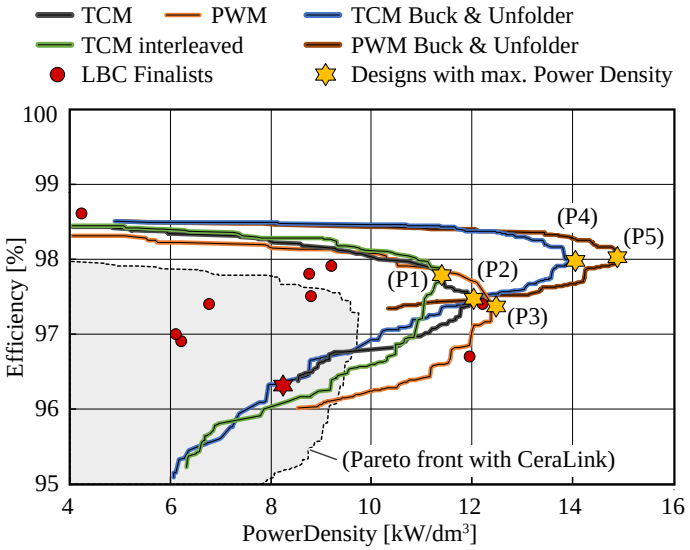


Fig. 12: Calculated Pareto fronts with respect to efficiency (η) and power density (ρ) of the described circuit topologies with different modulation schemes (TCM/PWM) and with/without interleaving of bridge-legs.

the DM-inductance values needed to achieve the filter attenuation are also given. Based on the determined filter values, the inductors and capacitors can then be designed arbitrarily considering again volume, losses and temperature. Finally, also the additional circuit components, such as the measurement circuits (voltage, current and zero crossing measurement), control circuits (DSP/FPGA), auxiliary supply, fans, PCB, connectors and housing, have to be taken into account, since these circuit parts are needed in any converter design and thus, with their initial volume and losses, already define the maximum achievable efficiency and power density. In **Fig. 12** the calculated Pareto fronts with respect to efficiency (η) and power density (ρ) as well as the designs with highest power density (P1)-(P5) are visualized for the two described circuit topologies with different modulation schemes (TCM/PWM) and with/without interleaving of bridge-legs. In addition, also the achieved performances of other LBC finalists are indicated. As already mentioned, for the design and dimensioning of the PPB and output filter capacitors the X6S ceramic capacitors are used. Furthermore, the inductors are designed with commercially available core types (N87 as core material) and with different litz wires. It can be noticed that compared to the full-bridge topology (P1-P3) with the conventional DC-|AC| buck converter & unfolder topology (P4, P5) approximately a $15-20\,\%$ higher power density at even higher efficiency (around $+0.5\,\%$) can be achieved. Furthermore, for both circuit topologies, PWM (P3, P5) results in a slightly higher power density than TCM (P1, P2, P4) and as already identified, interleaving of bridge-legs (P1) is not beneficial for the given specifications and the objective of high power density. The performance of the system presented at the GOOGLE LBC finals is indicated with a red star. As explained, the system is built with CeraLink capacitors and with multiple air gap multiple parallel foil winding inductors, which both strongly decrease the achievable efficiency. Furthermore, the switching and conduction losses were higher than expected. Taking these factors into account,

a (re-)optimization of the realized system still employing CeraLink capacitors would now result in the dashed Pareto front with the grey shaded performance space, where the maximum power density is achieved with lower switching frequency.

A more detailed comparison of the designs with highest power density (P1)-(P5) with respect to the volume and loss distribution of each design is given in **Fig. 11**. Considering the full-bridge topology, TCM modulation and interleaving of two bridge-legs results in the highest efficiency, however, also in the largest volume. This can be explained by the fact that, due to the interleaving, twice the number of semiconductors devices and inductors are used and thus, on the one hand the volume is increased (cf. **Fig. 11 a)**), but on the other hand the output current is shared between the bridge-legs resulting in lower GIT losses (cf. **Fig. 11 b)**). The highest power density is obtained with PWM modulation, however, with the drawback of the lowest efficiency. Compared to TCM modulation, the volume is mainly saved in the electronics, since with PWM modulation no zero crossing detection circuits and FPGA are needed, and in the output filter, since the (constant) switching frequency is selected below the lower CISPR limit of $150\,\mathrm{kHz}$ and thus only higher-order harmonics have to be filtered. In contrast, the volume occupied by the inductor and heat sink slightly increases due to the higher losses.

For the DC-|AC| buck converter & unfolder topology, the gain in power density is mainly achieved with the volume reduction of the GITs and the output inductors, since only one bridge-leg is needed for the buck stage. Compared to this, the volume increase due to the unfolder is much smaller. Furthermore, even though additional conduction losses are generated by the unfolder, with the DC-|AC| buck converter & unfolder topology the highest overall converter efficiency is achieved resulting also in a decreased heat sink volume. The difference in system performance between TCM and PWM modulation is again found in the electronics and output filter.

VI. Conclusion

In this paper the system performance of two inverter concepts considered for the GOOGLE Little Box Challenge (LBC), a full-bridge inverter and a DC-|AC| buck converter with a subsequent output-frequency unfolder, both either operated with zero voltage switching (ZVS) triangular current mode (TCM) modulation or PWM modulation, is compared. Based on a multi-objective Pareto-optimization concerning achievable efficiency and power density it is shown that, despite of the higher switching losses generated with the hard-switched PWM modulation compared to the soft-switched TCM modulation, for both inverter concept operated with PWM modulation the highest power density is achieved. This is justified by the fact that in order to achieve a high power density for TCM modulation a high switching frequency range has to be selected, which, in combination with the high current ripple and the larger RMS current compared to PWM, results in higher inductor and conduction losses. Hence, the advantages of low soft-switching losses achieved with TCM modulation are lost. Furthermore, it is shown that with the DC-|AC| buck converter & unfolder operated with PWM modulation the highest power density of $14.7\,\mathrm{kW/dm^3}$ ($240\,\mathrm{W/in^3}$) with a maximum efficiency of $98.1\,\%$ at $2\,\mathrm{kW}$ output power is obtained. Compared to the full-bridge inverter concept this means that the power density is increased by around $15-20\,\%$ and the efficiency at full output power by around $1.7\,\%$.

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