Google Little-Box Reloaded

Advances In Ultra-Compact GaN Based Single-Phase DC/AC Power Conversion

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Power Electronic Systems Laboratory
www.pes.ee.ethz.ch

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Advances In Ultra-Compact GaN Based Single-Phase DC/AC Power Conversion

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Outline

- The Google Little Box Challenge
- *Little Box 1.0*
- *Concepts & Performances of Other Finalists*
- *Optimization & Advanced Analysis*
- *Little Box 2.0*
- Conclusions

Acknowledgement
O. Knecht
F. Krismer
M. Guacci
L. Camurca
M. Kasper
E. Hatipoglu

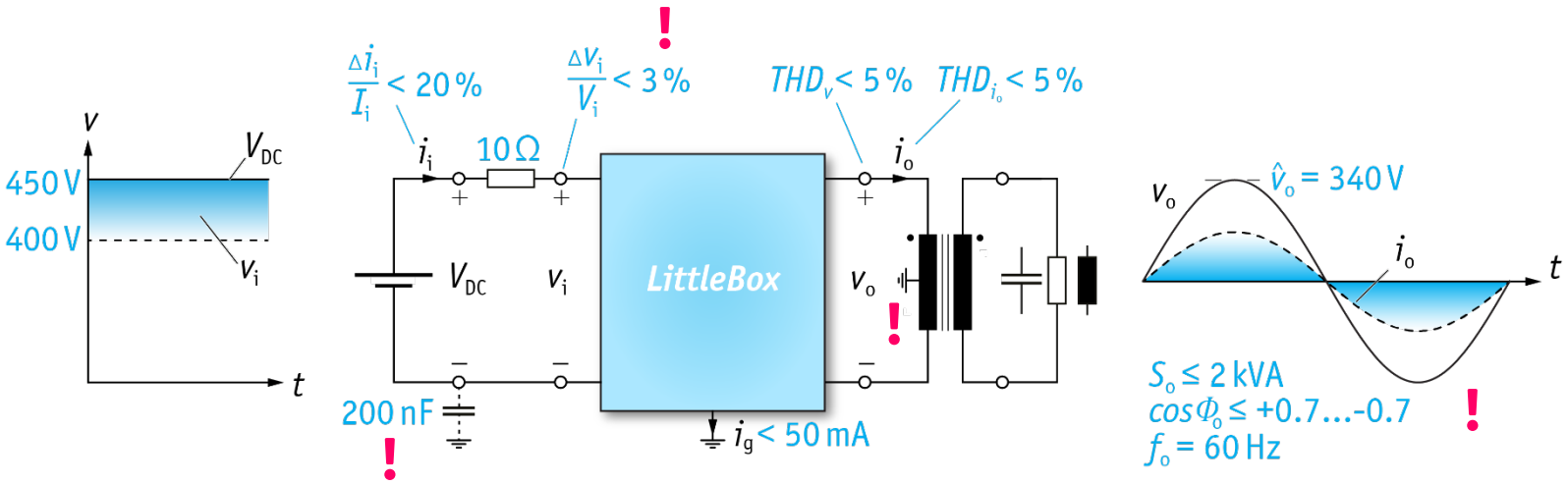
Google Little Box Challenge

Requirements
The Grand Prize
Finalists & Finals

LiTTLE BOX CHALLENGE

Google | IEEE

- Design / Build the 2kW 1-ΦSolar Inverter with the Highest Power Density in the World
- Power Density > 3kW/dm³ (> 50W/in³, multiply kW/dm³ by Factor 16)
- Efficiency > 95%
- Case Temp. < 60°C
- EMI FCC Part 15 B



- Push the Forefront of New Technologies in R&D of High Power Density Inverters

The Grand Prize

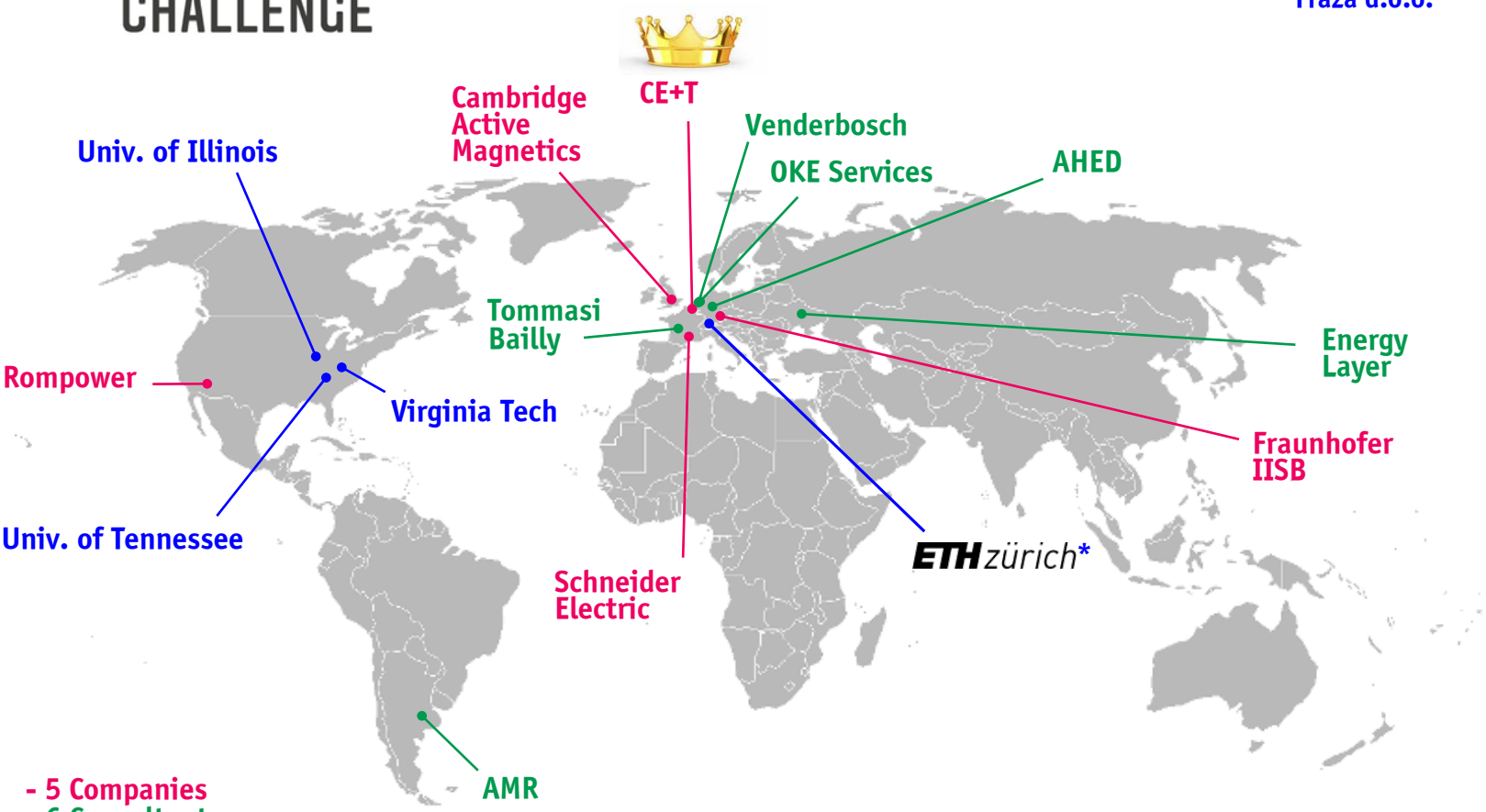
- **Highest Power Density (> 50W/in^3)**
- **Highest Level of Innovation**

$1,000,000

- Timeline
  - Challenge Announced in Summer 2014
  - **2000+ Teams Registered** Worldwide
  - 100+ Teams Submitted a Technical Description until July 22, 2015
  - **18 Finalists (3 No-Shows)**

LiTTLE BOX CHALLENGE Finalists

* and FH IZM / Fraza d.o.o.



- 5 Companies
- 6 Consultants
- 4 Universities

15 Teams/Participants in the Final @ NREL

LiTTLE BOX CHALLENGE Final Presentations

NREL
National Renewable Energy Laboratory
Innovation for Our Energy Future

- Finalists Invited to NREL / USA
- Presentations on Oct. 21, 2015
- Subsequent Testing by NREL

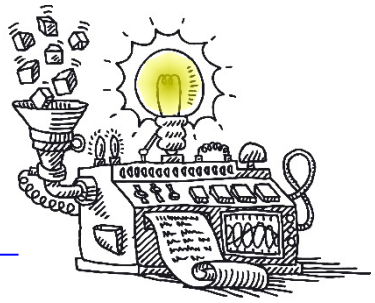
City of Golden

Little Box 1.0

Converter Topology
Modulation & Control
Technologies /Components
Mechanical Concept
Exp. Analysis

Acknowledgement

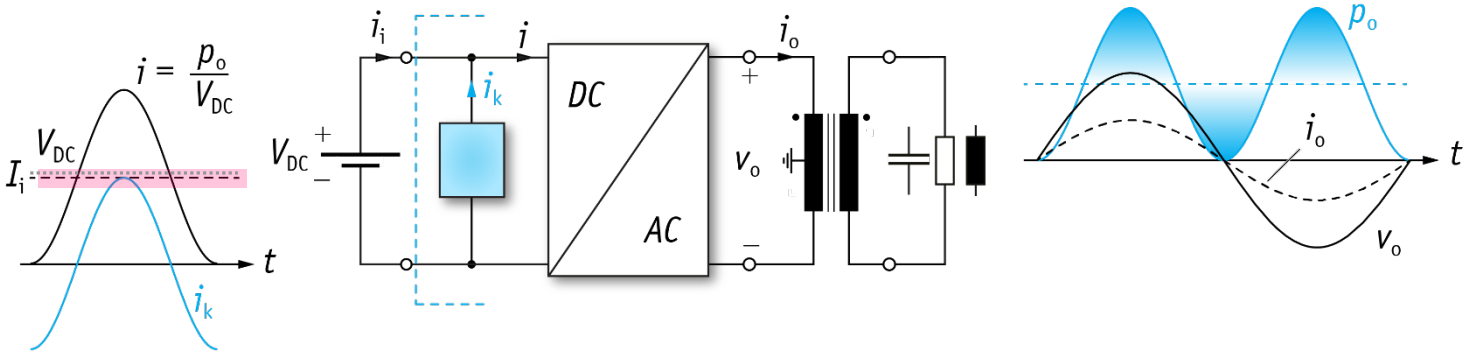
Derivation of Converter Concept



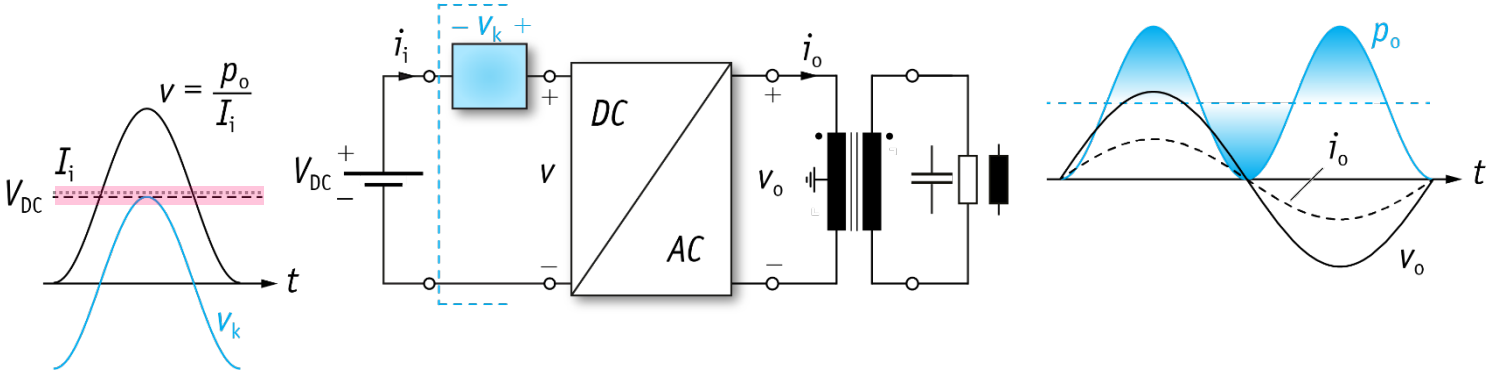
1-Φ Output Power Pulsation Buffer

Power Pulsation Buffer

- Parallel Buffer @ DC Input



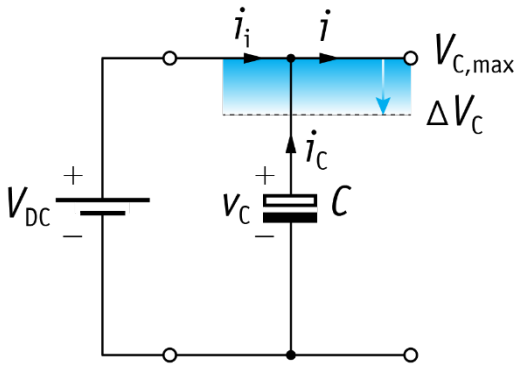
- Series Buffer @ DC Input

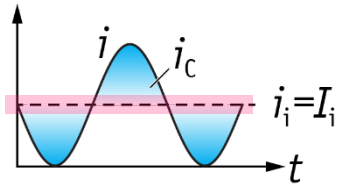


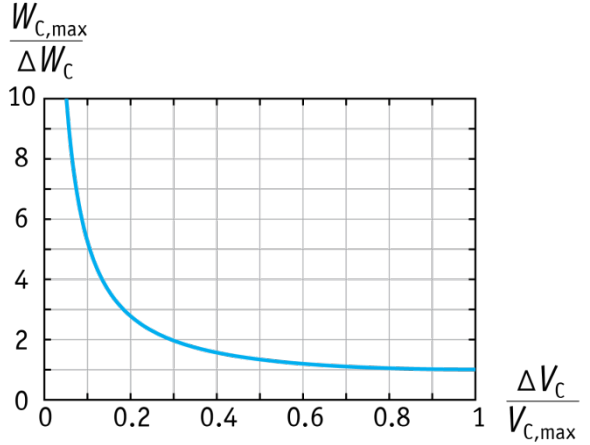
- Parallel Approach for Limiting Voltage Stress on Converter Stage Semiconductors

Passive Power Pulsation Buffer (1)

- Electrolytic Capacitor







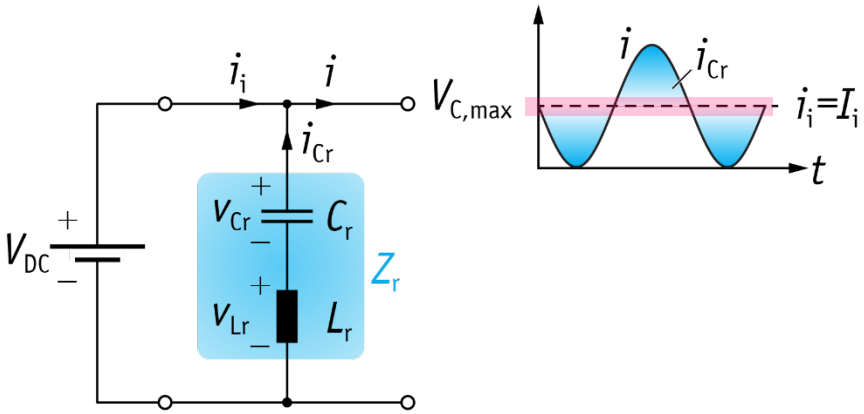
S_0 = 2.0 kVA
cos Φ_0 = 0.7
$V_{C,max}$ = 450 V
$\Delta V_C / V_{C,max}$=3 %

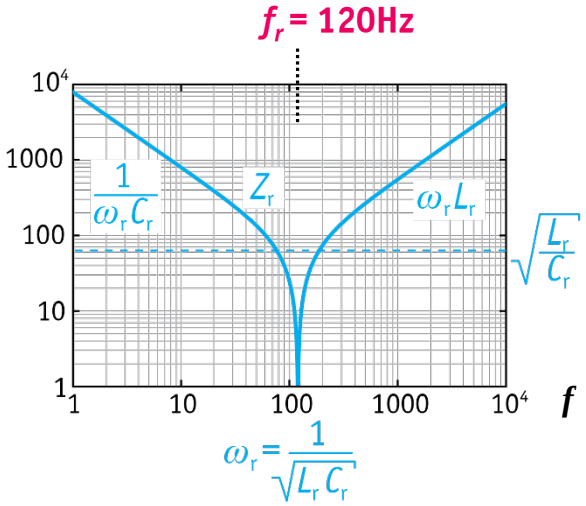
EPCOS
5 x 493µF/450 V
C= 2.46 mF

- C > 2.2mF / 166 cm³ → Consumes 1/4 of Allowed Total Volume !

Passive Power Pulsation Buffer (2)

- Series Resonant Circuit / Used in Rectifier Input Stage of Locomotives



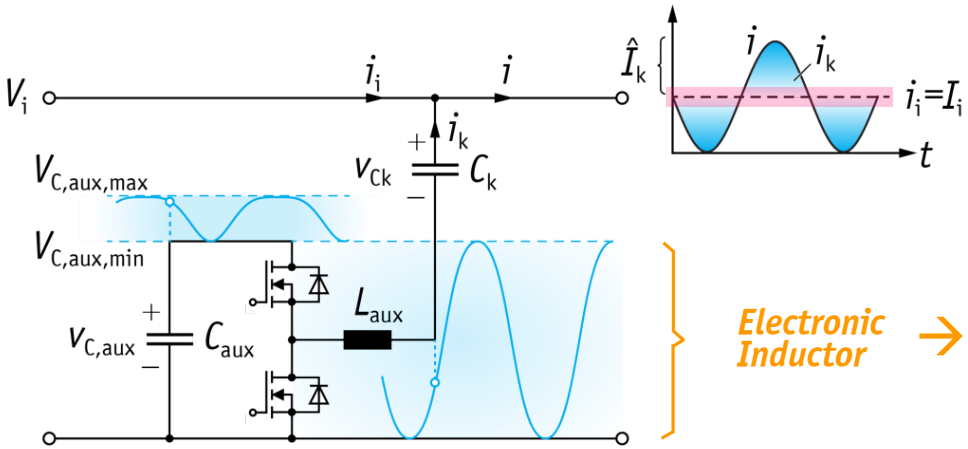


* C_r = 20 µF
* L_r = 127 mH @ v_{Lr} = 400 V

- Unacceptably Large Inductor Volume ! → Electronic Inductor

Partial Active Power Pulsation Buffer

- Coupling Capacitor & "*Electronic Inductor*" Processing Only *Partial Power*



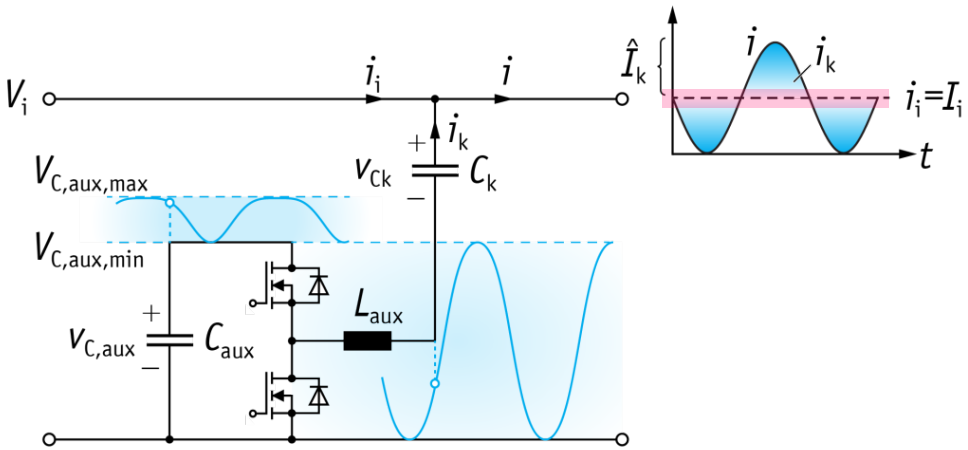
Electronic Inductor →

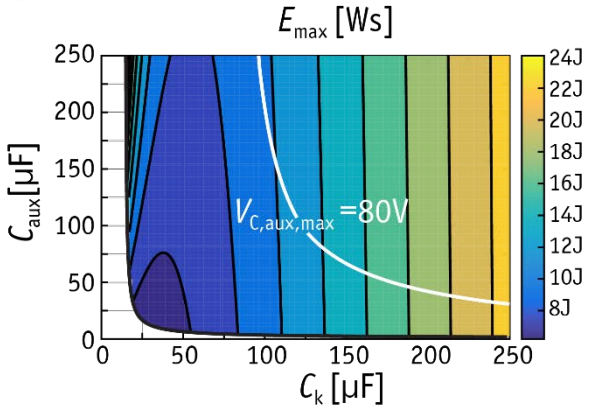
* Ertl (1999)
* Enslin (1991)
* Pilawa (2015)

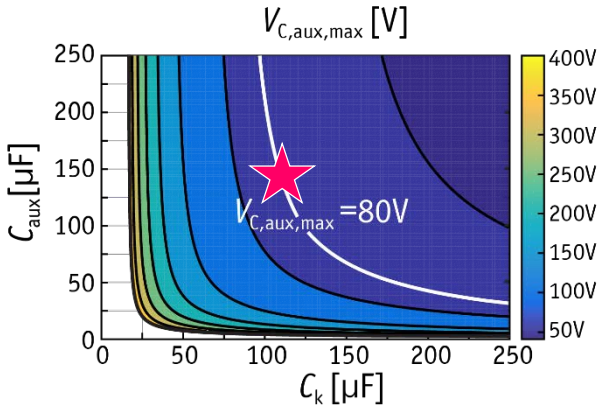
- Low $U_{C,aux}$ → Low Converter Losses
- High Values of C_K, C_{aux} Required for Low $U_{C,aux}$
- Full-Bridge Aux. Converter Allows Lower $U_{C,aux}$

Partial Active Power Pulsation Buffer

- Coupling Capacitor & "*Electronic Inductor*"







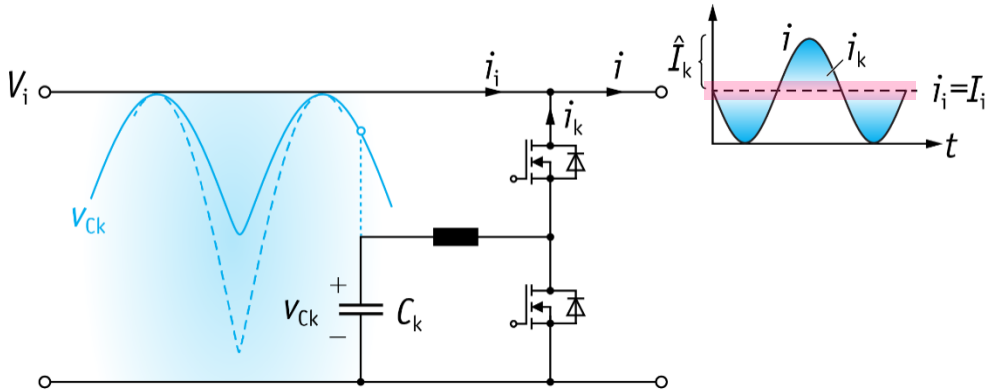
- Low $U_{C,aux}$ → Low Converter Losses
- High Values of C_K, C_{aux} Required for Low $U_{C,aux}$
- Full-Bridge Aux. Converter Allows Lower $U_{C,aux}$

▲ Properties of Full-Bridge Aux. Conv.

Full Active Power Pulsation Buffer

* Kyritsis (2007)

- Large Voltage Fluctuation Foil or Ceramic Capacitor
- Buck- or Boost-Type DC/DC Interface Converter
- Buck-Type allows Utilizing 600V Technology



CeraLink TDK

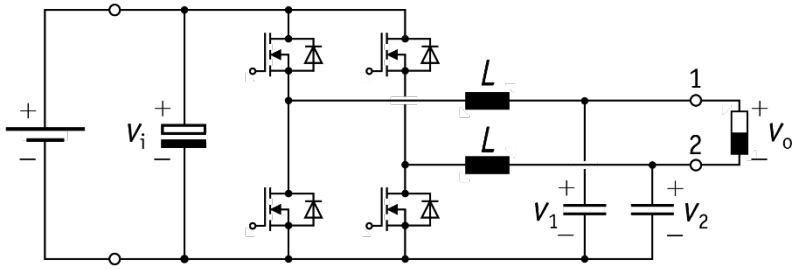
108 x 1.2 µF /400 V
$C_k \approx 140$ µF
$V_{Ck} = 23.7 cm^3$

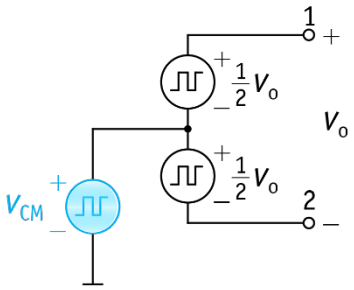
- Significantly Lower Overall Volume Compared to Electrolytic Capacitor

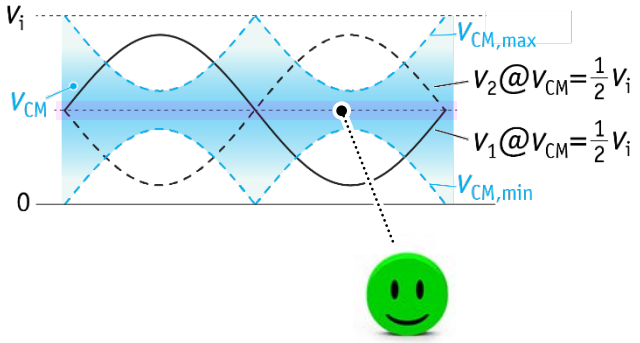
Output Stage
Topology / Modulation

Symmetric PWM Full-Bridge AC/DC Conv. Topology

- Symmetric PWM Operation of Both Bridge Legs
- No Low-Frequency CM Output Voltage Component





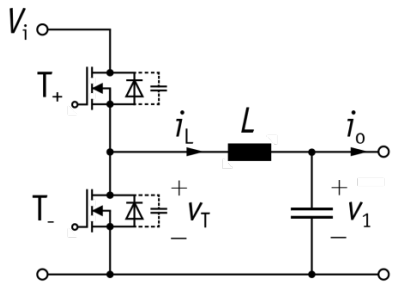


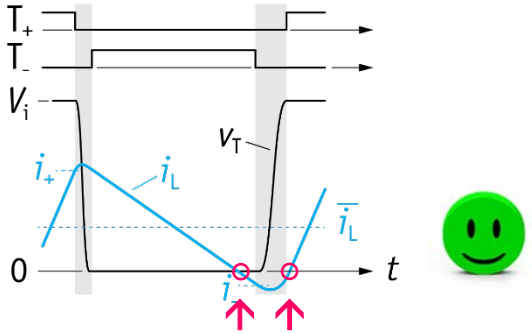
- DM Component of u_1 and u_2 Defines Output u_0
- CM Component of u_1 and u_2 Represents Degree of Freedom of the Modulation (!)

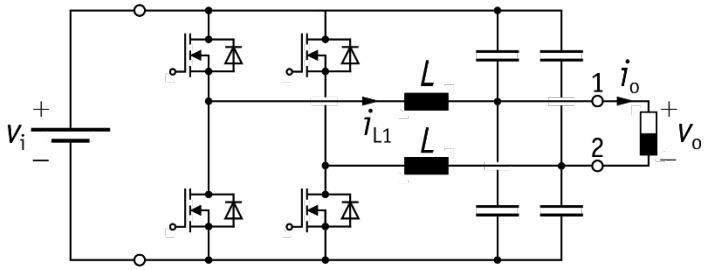
ZVS of Output Stage / TCM Operation

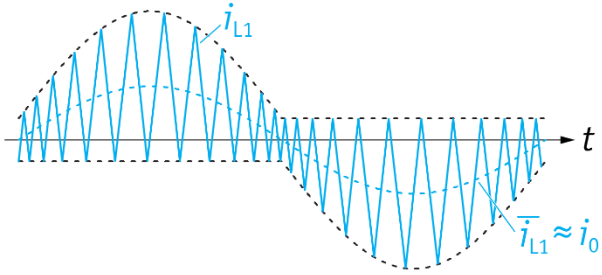
* Henze (1988)

- TCM Operation for Resonant Voltage Transition @ Turn-On/Turn-Off





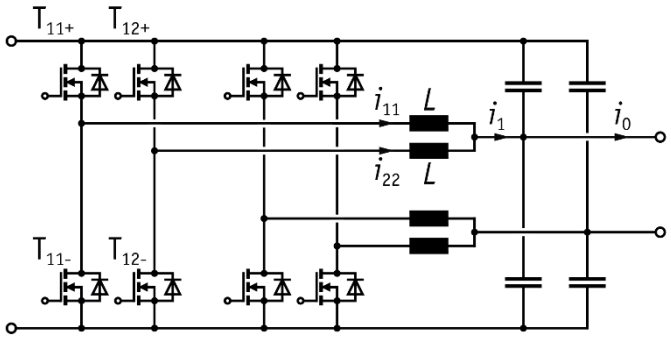


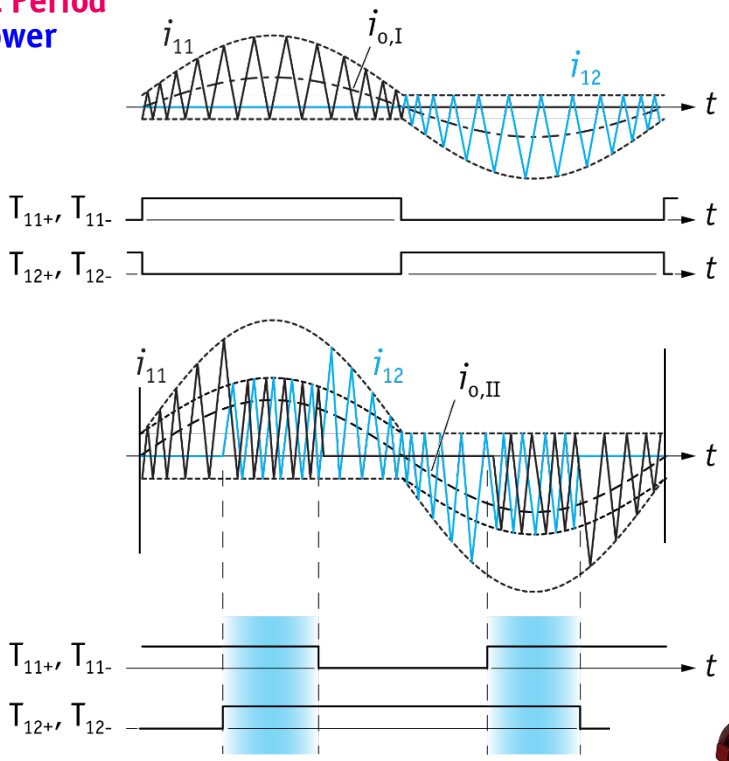


- Requires Only Measurement of Current Zero Crossings, i = 0
- Variable Switching Frequency Lowers EMI

4D-Interleaving

- Interleaving of 2 Bridge Legs per Phase - Volume / Filtering / Efficiency Optimum
- Interleaving in Space & Time – Within Output Period
- Alternate Operation of Bridge Legs @ Low Power
- Overlapping Operation @ High Power



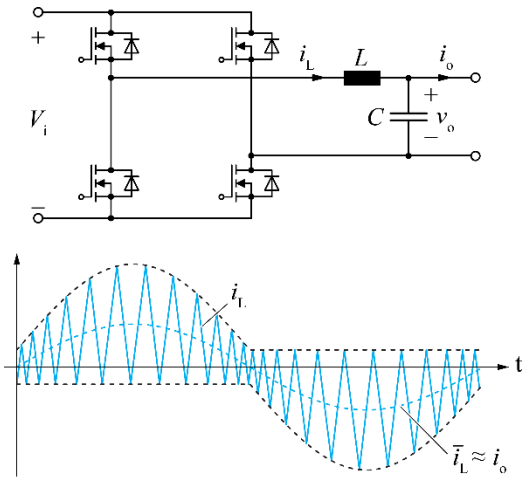


- Opt. Trade-Off of Conduction & Switching Losses / Opt. Distribution of Losses

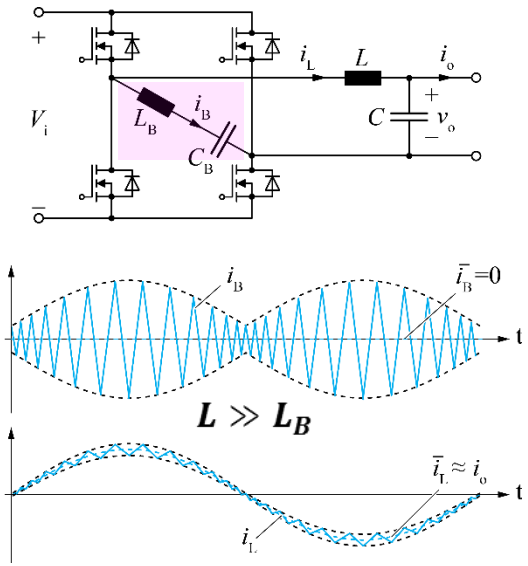
Remark: iTCM Inverter Topology

- TCM : Challenging Inductor Design → Superposition of HF & LF Currents
- iTCM: Adding LC-Circuit between Bridge Legs → Separation of LF & HF Currents → $L >> L_B$

– TCM



– iTCM

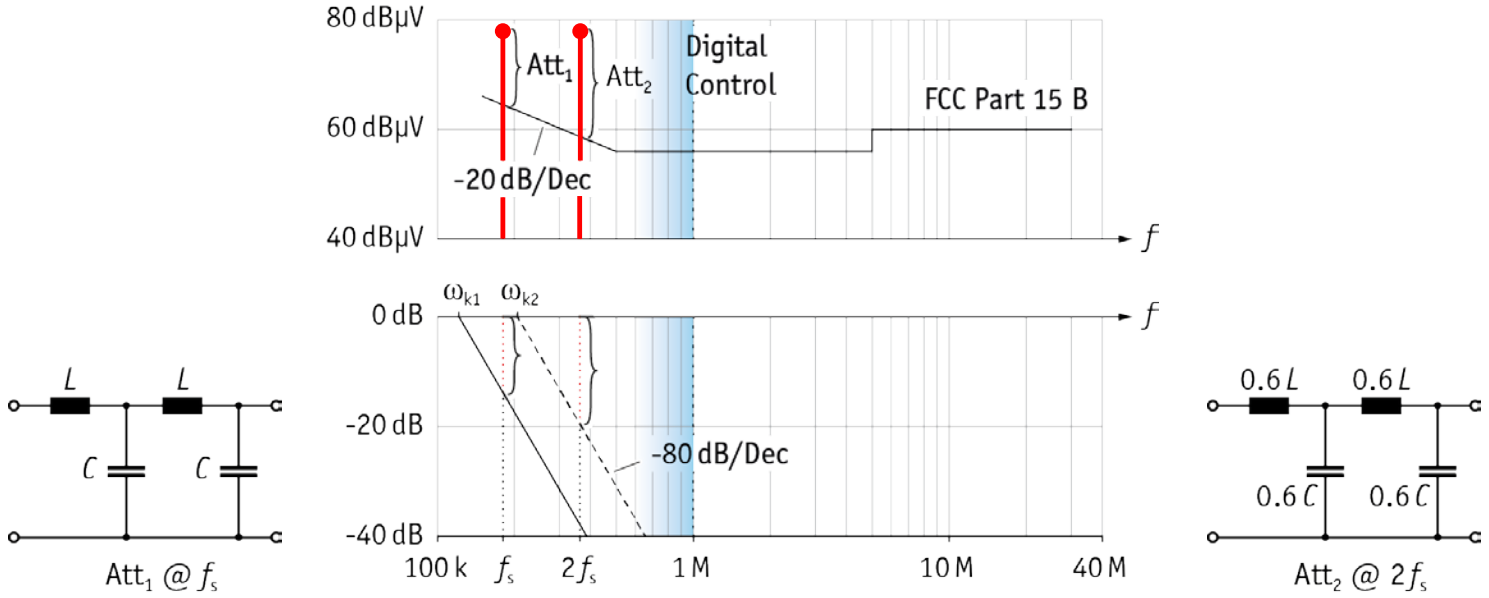


- Low Output Current Ripple → Reduced Filtering Effort
- PWM Modulation Applicable → Simple Control Strategy
- Dedicated LF and HF Inductor Designs Possible → Improved Converter Efficiency

* P. Jain (2015)

Selection of Switching Frequency

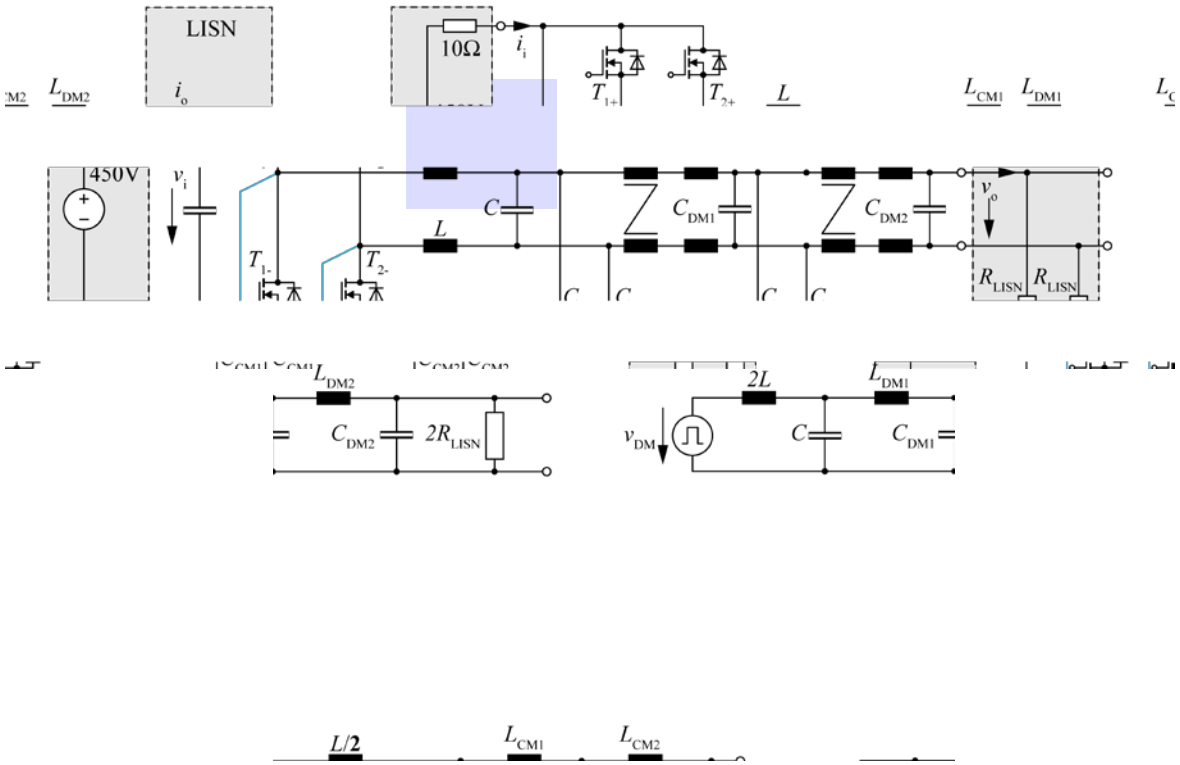
- Significant Reduction in EMI Filter Volume for Increasing Sw. Frequency



- Doubling Sw. Fequ. f_S Cuts Filter Volume in Half
- Upper Limit due to Digital Signal Processing Delays / Inductor & Sw. Losses – Heatsink Volume

EMI Filter Topology (1)

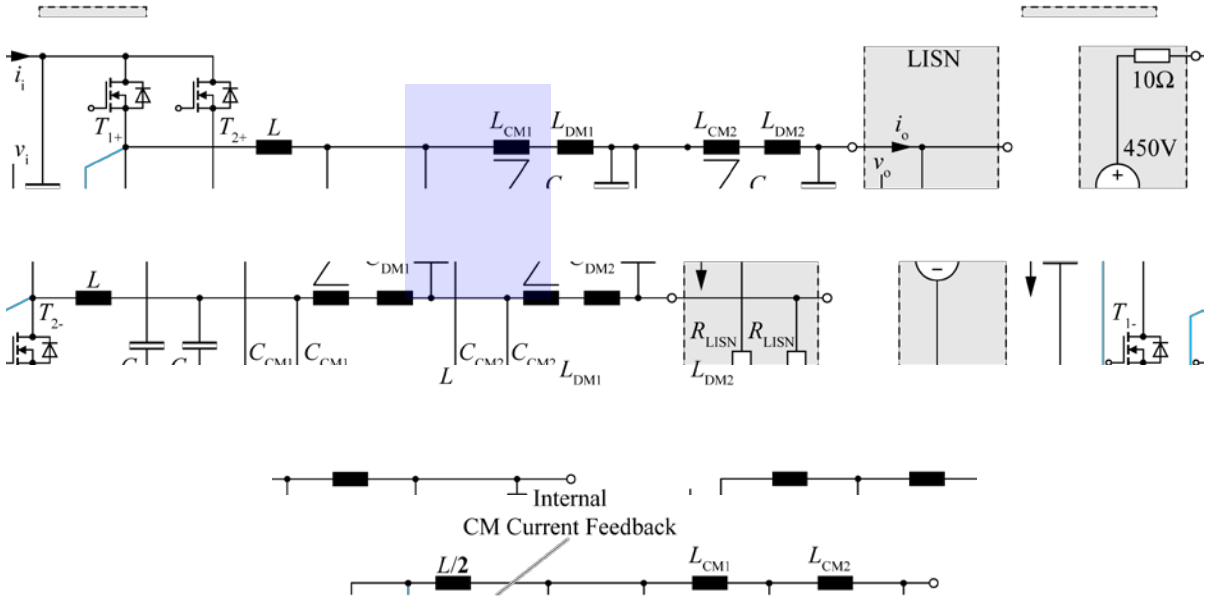
- Conventional Filter Structure
  - DM Filtering Between the Phases
  - CM Filtering Between Phases and PE



- CM Cap. Limited by Earth Current Limit – Typ. 3.5mA for PFC Rectifiers (GLBC: 5mA then 50mA !)
- Large CM Inductor Needed – Filter Volume Mainly Defined by CM Inductors

EMI Filter Topology (2)

- Filter Structure with Internal CM Capacitor Feedback
- Filtering to DC- (and optional to DC+)

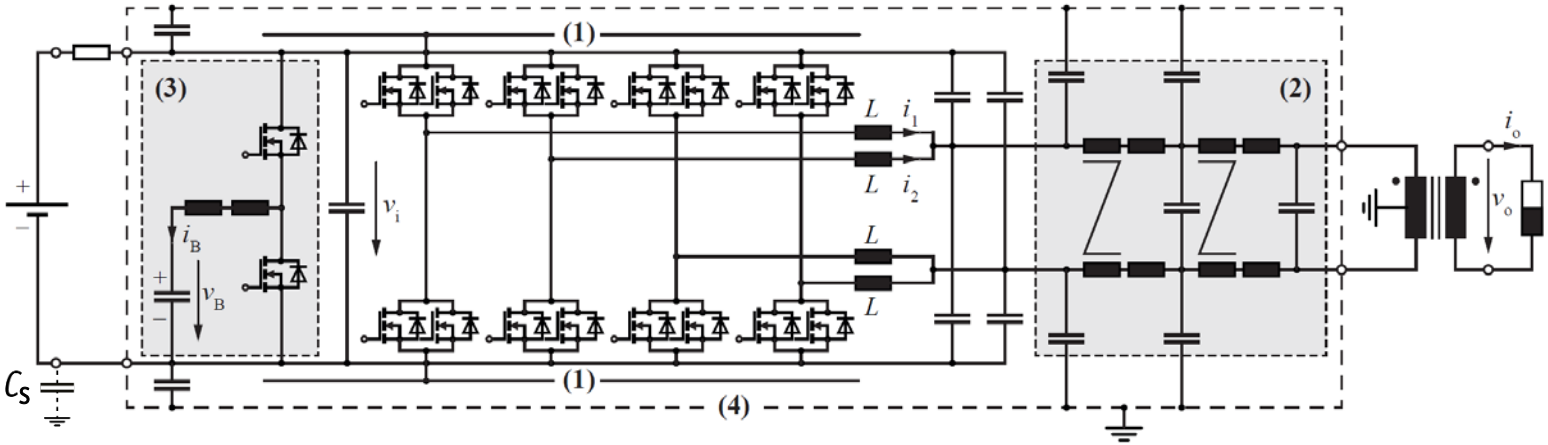


- No Limitation of CM Capacitor C_1 Due to Earth Current Limit → µF Instead of nF Can be Employed
- Allows Downsizing of CM Inductor and/or Total Filter Volume

Final Converter Topology

- Interleaving of 2 Bridge Legs per Phase
- Active DC-Side Buck-Type Power Pulsation Buffer
- 2-Stage EMI AC Output Filter

(1) Heat Sink
(2) EMI Filter
(3) Power Pulsation Buffer
(4) Enclosure



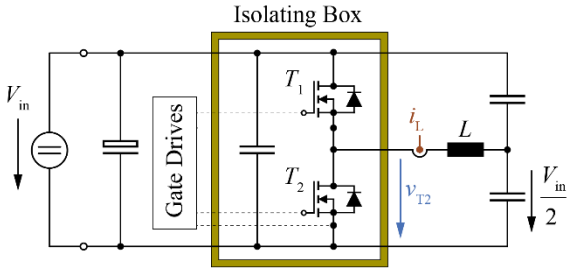
- ZVS of All Bridge Legs @ Turn-On/Turn-Off in Whole Operating Range (4D-TCM-Interleaving)
- Heatsinks Connected to DC Bus / Shield to Prevent Cap. Coupling to Grounded Enclosure

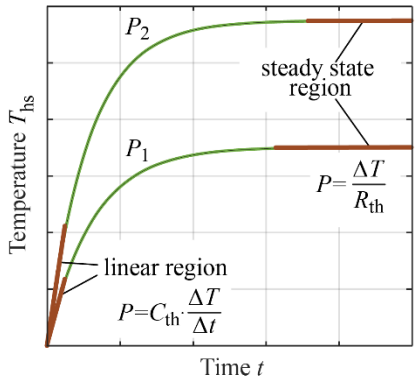
Technologies

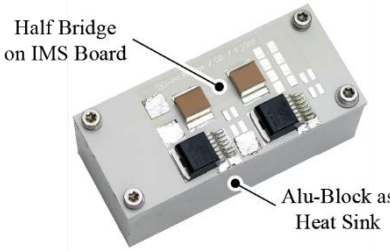
- Power Semiconductors
- Cooling
- DSP/FPGA
- Auxiliary

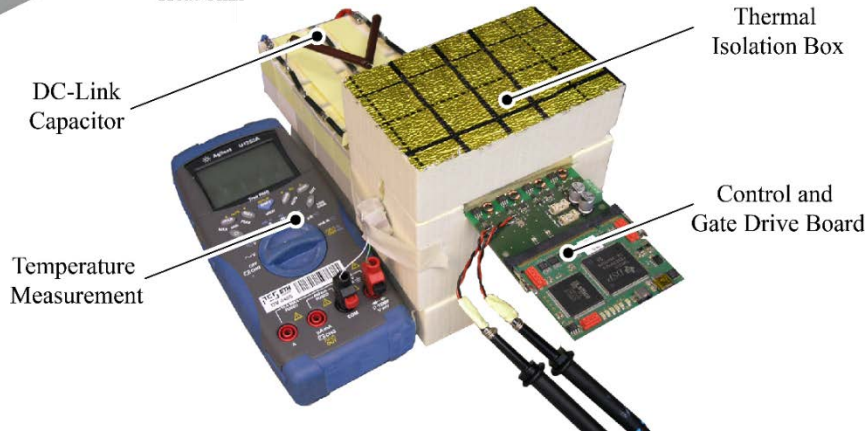
Evaluation of Power Semiconductors (1)

- Accurate Measurement of ZVS Losses Using Calorimetric Approach
- High Sw. Frequency for Large Ratio of Sw. and Conduction Losses





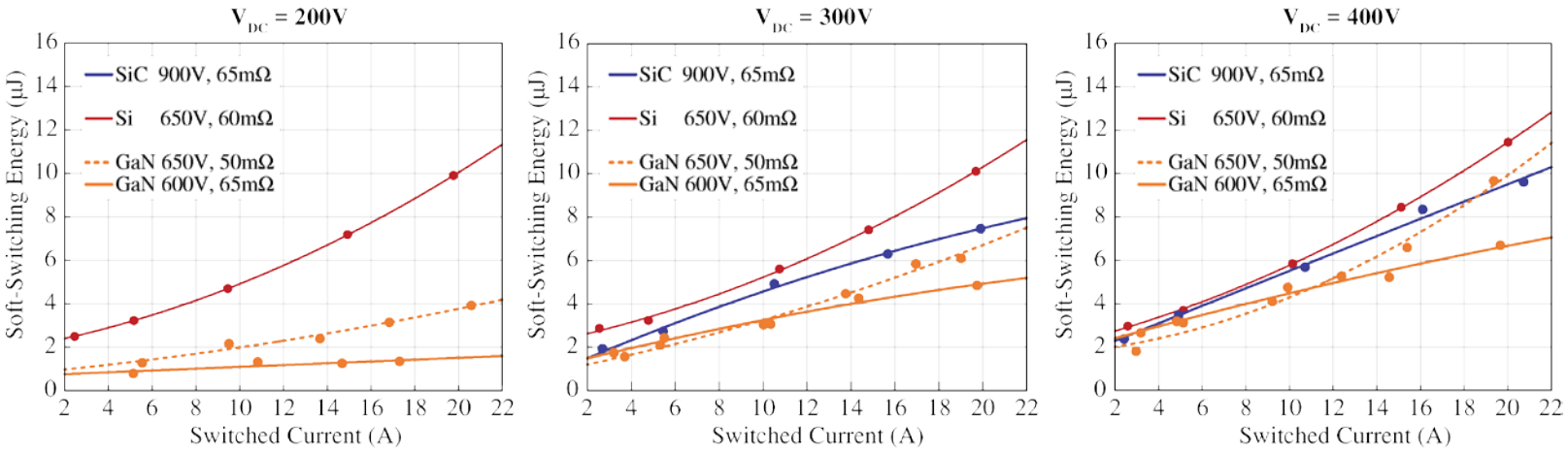




- Direct Measurement of the Sum of Sw. and Conduction Losses
- Subtraction of the Conduction Losses Known from Calibration
- Fast Measurement by $C_{th}.\Delta T/\Delta t$ Evaluation

Evaluation of Power Semiconductors (2)

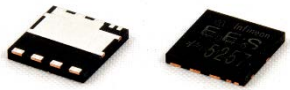
- Comparison of Soft-Switching Performance of ~60mΩ, 600V/650V/900V GaN, SiC, Si MOSFETs
- Measurement of Energy Loss per Switch and Switching Period



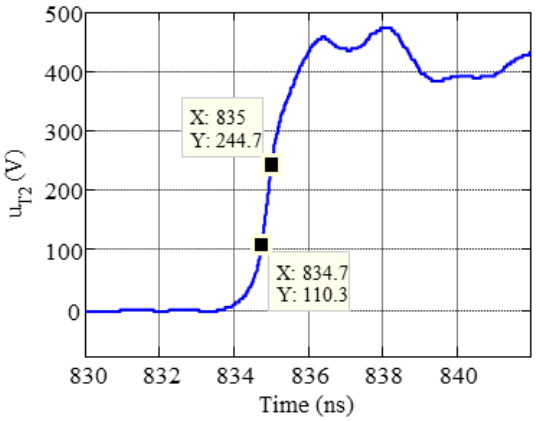
- GaN MOSFETs Feature Highest Soft-Switching Performance
- Similar Soft-Switching Performance Achieved with Si and SiC
- Almost No Voltage-Dependency of Soft-Switching Losses for Si-MOSFET

Selected Power Semiconductors

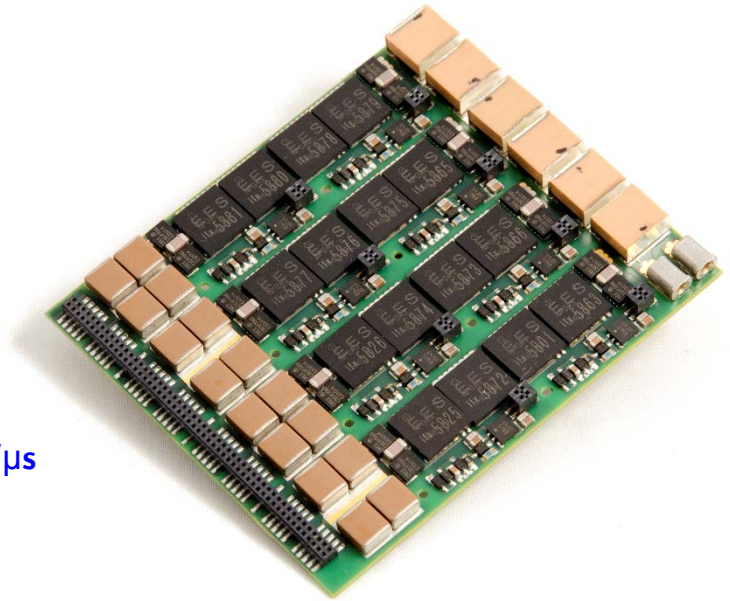
- 600V IFX Normally-Off GaN GIT - ThinPAK8x8
- 2 Parallel Transistors / Switch
- Antiparallel CREE SiC Schottky Diodes



- 1.2V typ. Gate Threshold Voltage
- 55 mΩ $R_{DS,on}$ @ 25°C, 120mΩ @ 150°C
- 5Ω Internal Gate Resistance



dv/dt = 500kV/µs

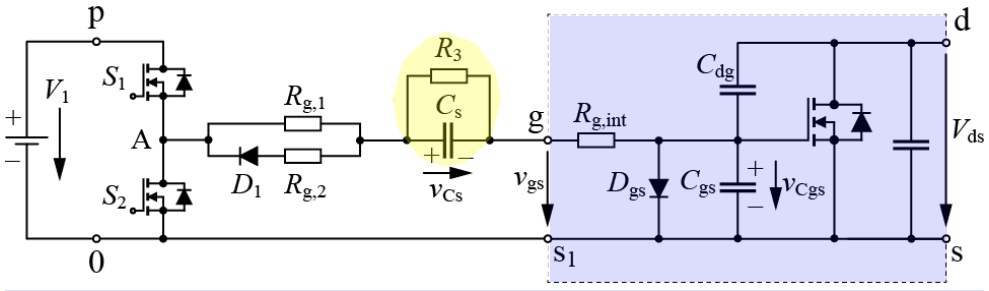


- CeraLink Capacitors for DC Voltage Buffering

High dv/dt-Immunity Gate Drive (1)

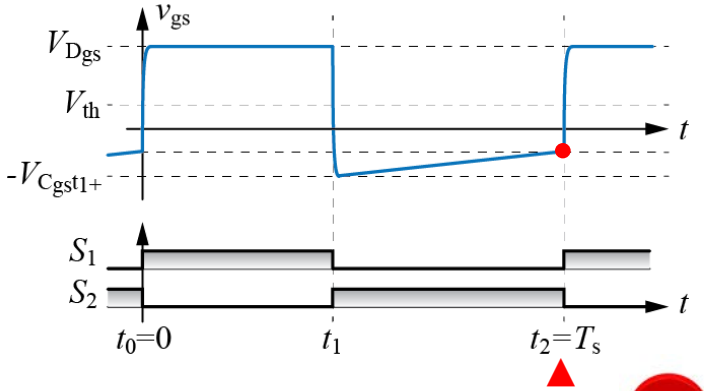
- Low Threshold-Voltage of GaN GIT Devices → Negative Gate Voltage During Off-State Needed
- Internal Diode Characteristic → Gate Current Limitation During On-State Needed

- State-of-the-Art Gate Drive with Additional RC-Circuit



– C_s Enables High Gate Current for Fast Turn-On

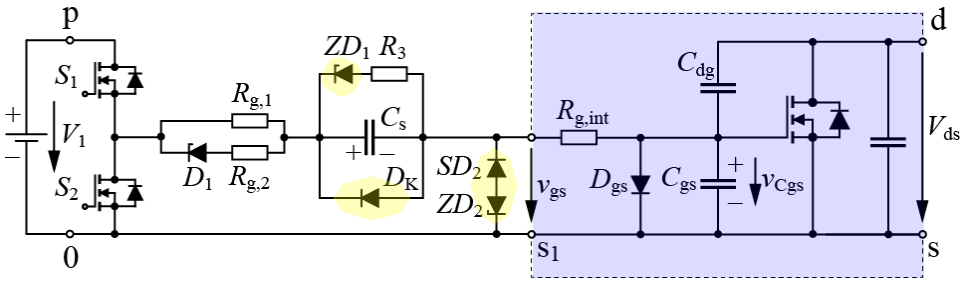
– R_3 Discharges C_s During Off-State



- Duty Cycle and Frequency Dependent Gate Voltage
- Risk of Parasitic Turn-on Due to Switching of Complementary Switch

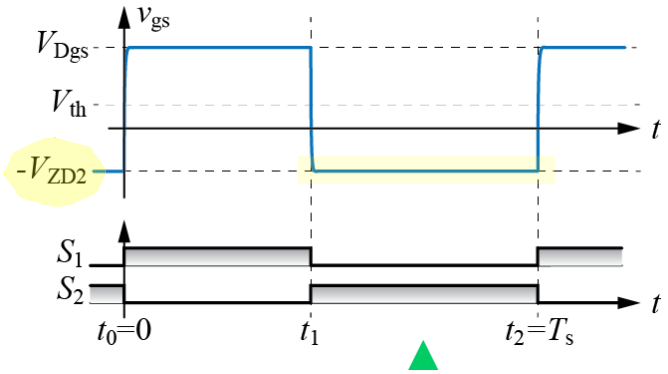
High dv/dt-Immunity Gate Drive (2)

- Improved Gate Drive Circuit with RC-Circuit and Added Clamping Diodes
- High Current for Fast Turn-On as Conventional Approach



– Diode ZD_2 Quickly Discharges C_s to V_{ZD2} @ Turn-Off

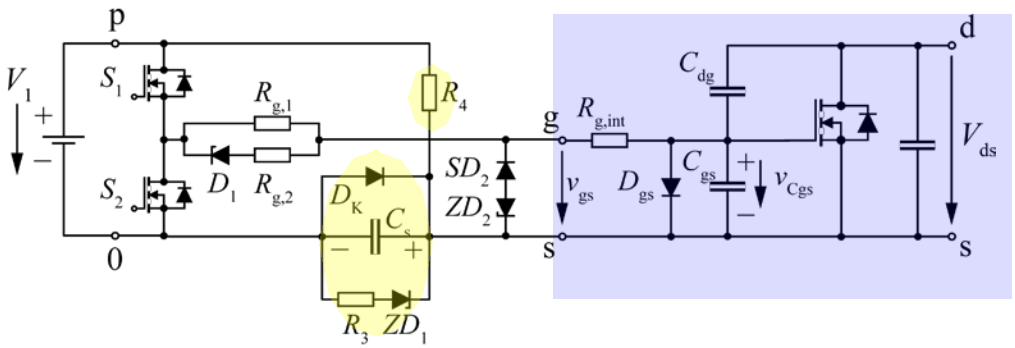
– Diode ZD_1 Prevents C_s from Complete Discharge During Off-State



- Fixed Neg. Turn-Off Gate Voltage Independent of Duty Cycle and @ Start-Up

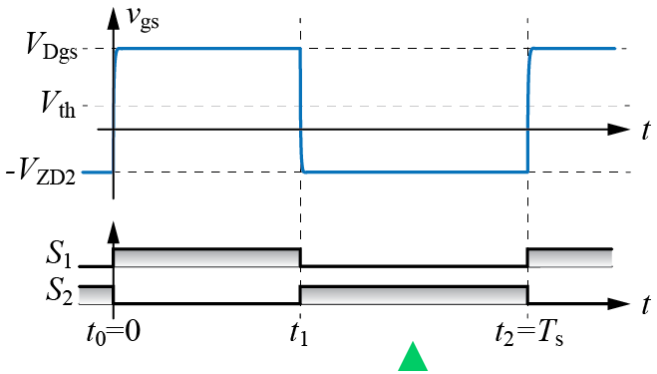
High dv/dt-Immunity Gate Drive (3)

- Improved Gate Drive Circuit with RC-Circuit and Added Clamping Diodes
- High Current for Fast Turn-On as Conventional Approach



– Diode ZD_2 Quickly Discharges C_s to V_{ZD2} @ Turn-Off

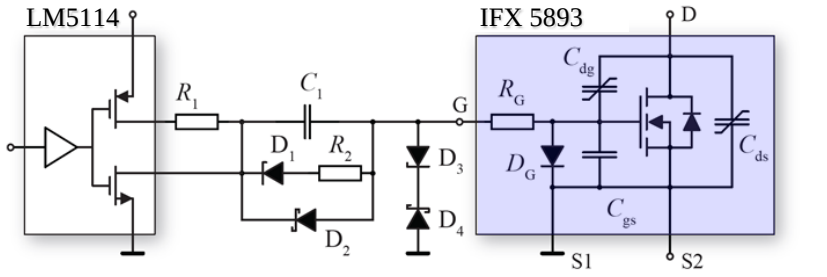
– Diode ZD_1 Prevents C_s from Complete Discharge During Off-State

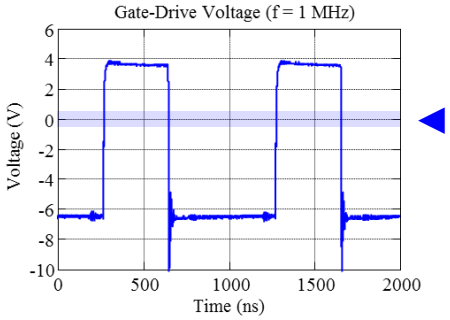


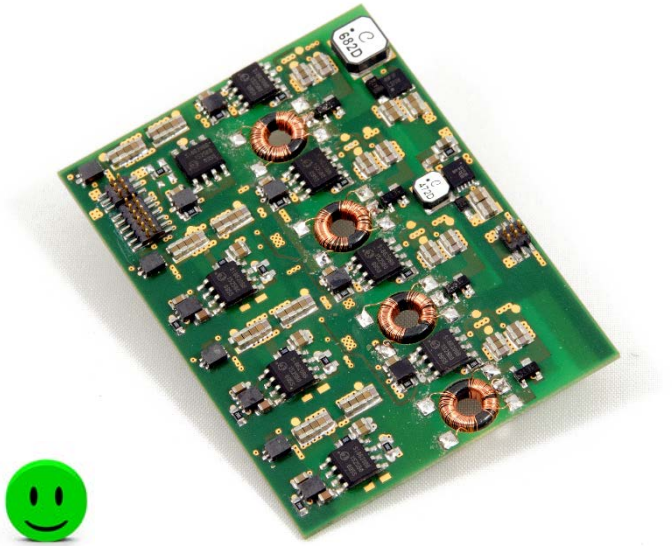
- Fixed Neg. Turn-Off Gate Voltage Independent of Duty Cycle and @ Start-Up
- RC-Circuit in Neg. Rail Enables Precharge of C_s with R_4

Final Advanced Gate Drive

- Fixed Negative Turn-off Gate Voltage - Independent of Sw. Frequency and Duty Cycle
- Extreme dv/dt Immunity (500 kV/µs) - Due to CM Choke at Signal Isolator Input





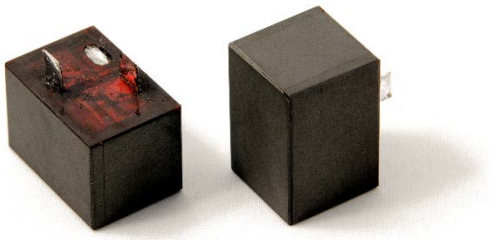


- Total Prop. Delay < 30ns incl. Signal Isolator, Gate Drive, and Switch Turn-On Delay

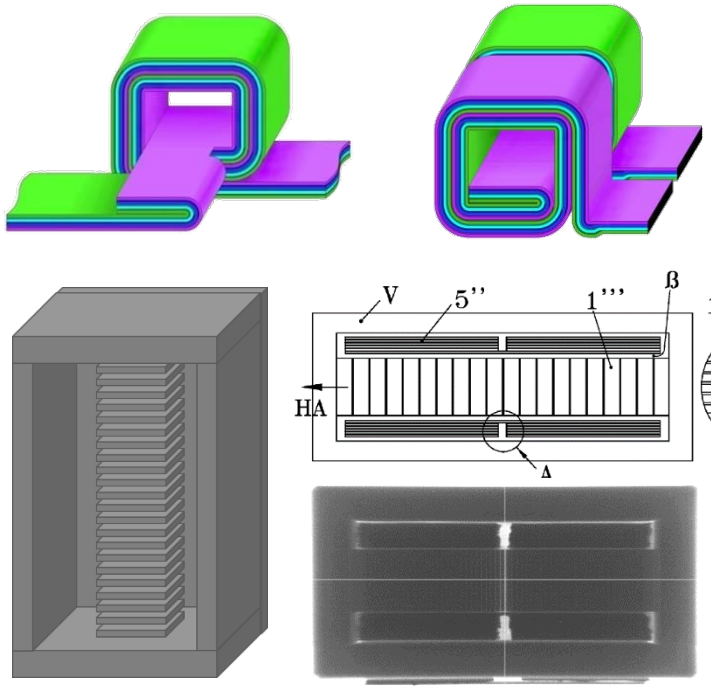
High Frequency Inductors (1)

- Multi-Airgap Inductor with Multi-Layer Foil Winding Arrangement Minim. Prox. Effect
- Very High Filling Factor / Low High Frequency Losses
- Magnetically Shielded Construction Minimizing EMI
- Intellectual Property of F. Zajc / Fraza

- L= 10.5µH
- 2 x 8 Turns
- 24 x 80µm Airgaps
- Core Material DMR 51 / Hengdian
- 0.61mm Thick Stacked Plates
- 20 µm Copper Foil / 4 in Parallel
- 7 µm Kapton Layer Isolation
- 20mΩ Winding Resistance / Q≈600
- Terminals in No-Leakage Flux Area

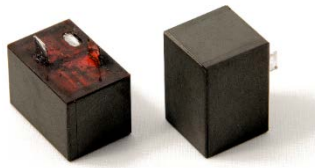


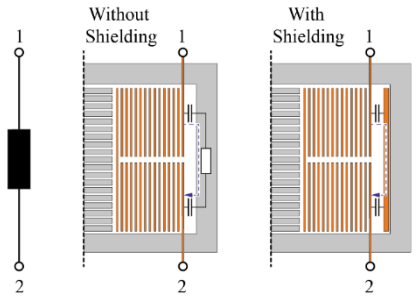
■ Dimensions - 14.5 x 14.5 x 22mm³

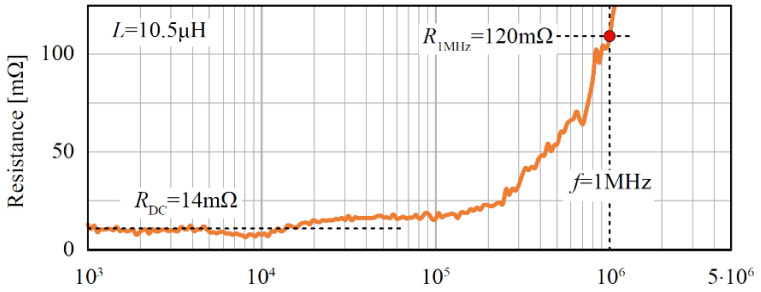


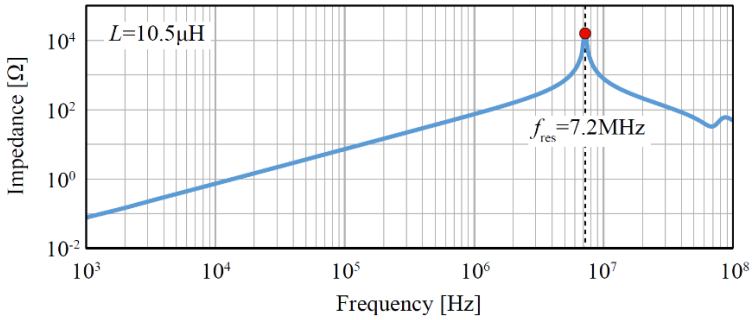
High Frequency Inductors (2)

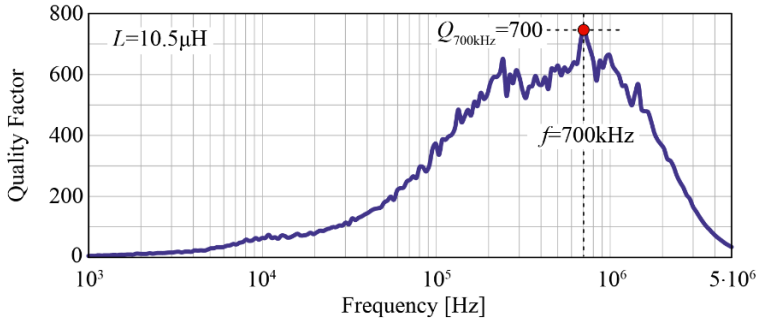
- High Resonance Frequency → Inductive Behavior up to High Frequencies
- Extremely Low AC-Resistance → Low Conduction Losses up to High Frequencies
- High Quality Factor









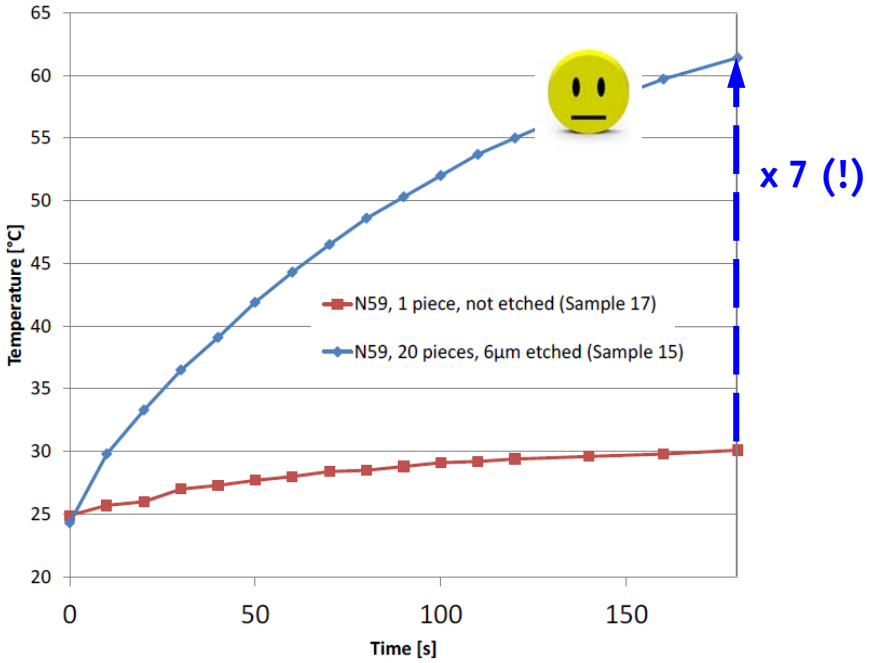


- Shielding Eliminates HF Current through the Ferrite → Avoids High Core Losses
- Shielding Increases the Parasitic Capacitance

High Frequency Inductors (3)

* Knowles (1975!)

- Cutting of Ferrite Introduces Mech. Stress
- Significant Increase of the Loss Factor
- Reduction by Polishing / Etching (5 µm)

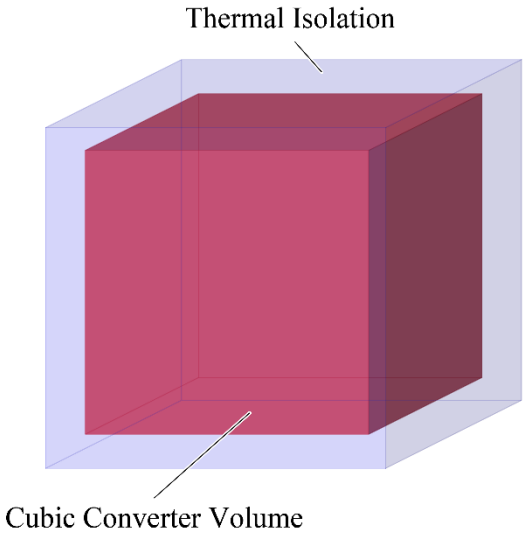


- Comparison of Temp. Increase of a Bulk and a Sliced Sample @ 70mT / 800kHz

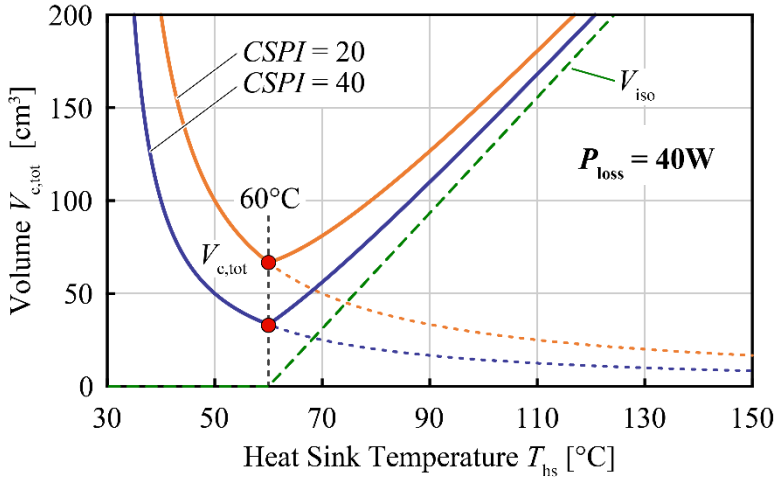
Thermal Management

- 30°C max. Ambient Temperature
- 60°C max. Allowed Surface and Air Outlet Temperature

- Evaluation of Optimum Heatsink Temperature for Thermal Isolation of Converter



$$CSPI\left[\frac{W}{K\cdot liter}\right] = \frac{G_{th,S-a}^{(HS)}\left[\frac{W}{K}\right]}{Vol_{CS}\left[liter\right]} = \frac{1}{R_{th,S-a}^{(HS)}\left[\frac{K}{W}\right]\cdot Vol_{CS}\left[liter\right]}$$

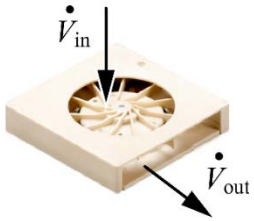


- Minimum Volume Achieved w/o Thermal Isolation with Heatsink @ max. Allowed Surface Temp.

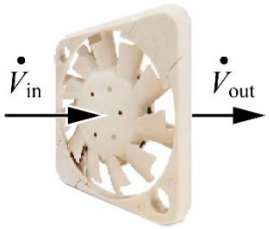
Thermal Management

- Overall Cooling Performance Defined by Selected Fan Type and Heatsink

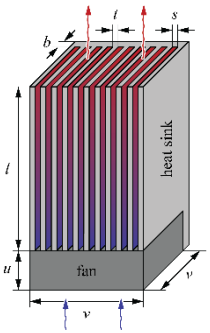
– Radial Blower



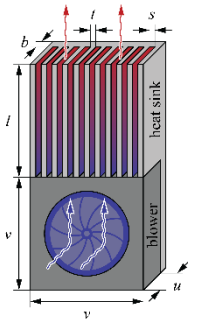
– Axial Fan

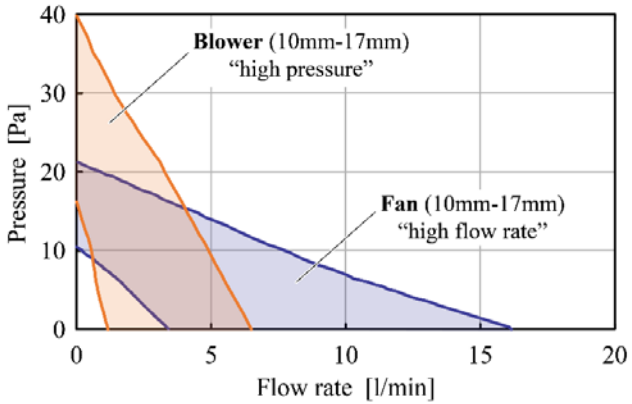


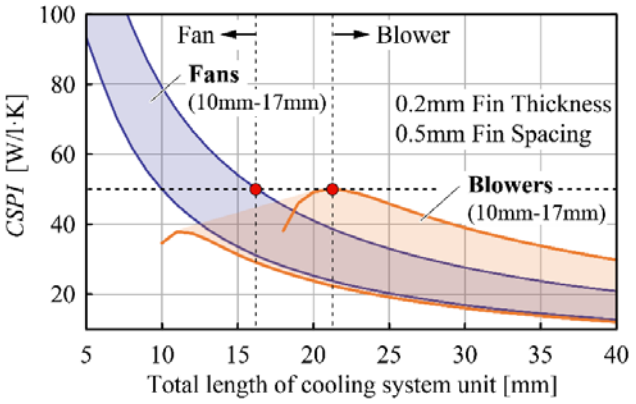
– Square Cross Section of Heatsink for Using a Fan



– Flat and Wide Heatsink for Blower





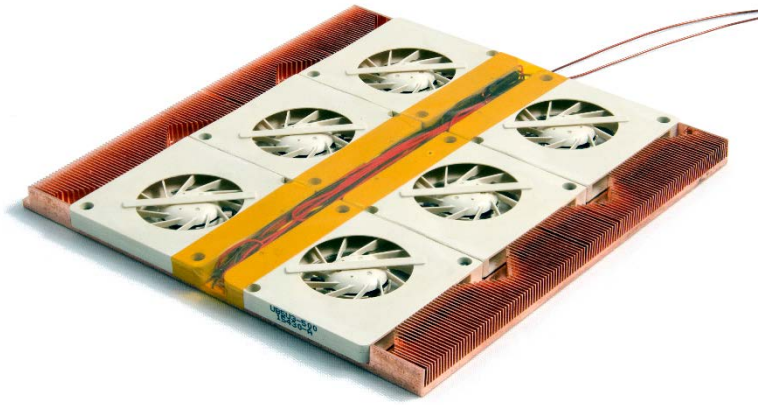


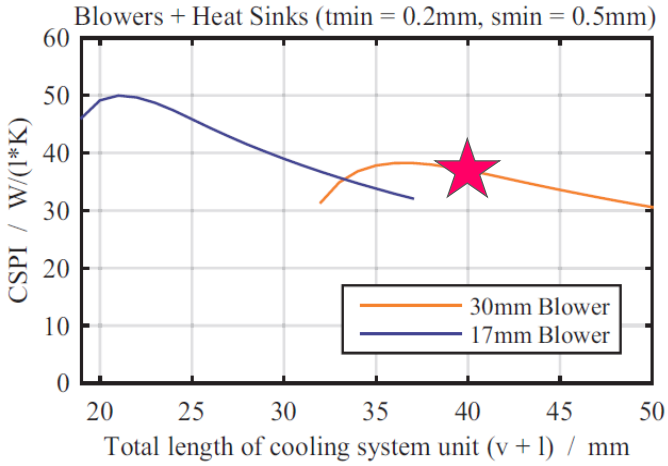
- Optimal Fan and Heat Sink Configuration Defined by Total Cooling System Length
- Cooling Concept with Blower Selected → Higher *CSPI* for Larger Mounting Surface

Final Thermal Management Concept (1)

- 30mm Blowers with Axial Air Intake / Radial Outlet
- Full Optimization of the Heatsink Parameters

- 200um Fin Thickness
- 500um Fin Spacing
- 3mm Fin Height
- 10mm Fin Length
- CSPI = 37 W/(dm³.K)
- 1.5mm Baseplate





- $CSPI_{eff}$= 25 W/(dm³.K) Considering Heat Distribution Elements
- Two-Side Cooling → Heatsink Temperature = 52°C @ 80W (8W by Natural Convection)

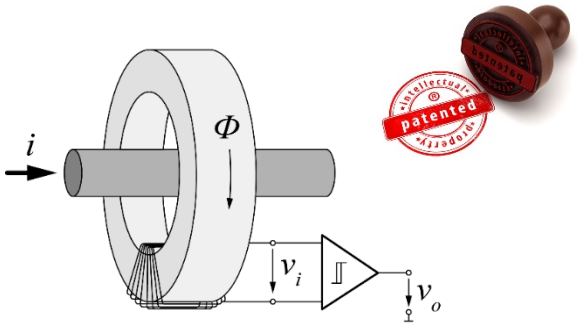
i=0 Detection

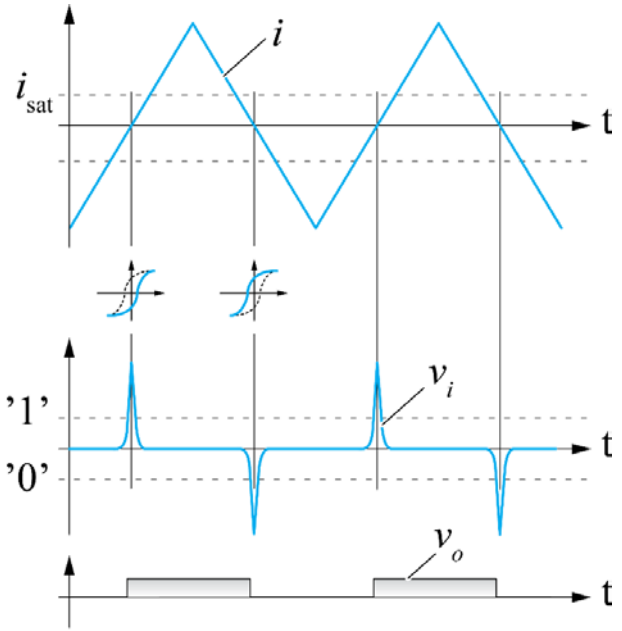
- Analyzed Methods
  - Shunt Current Measurement
  - Measurement of the $R_{ds,on}$
  - Two Antiparallel Diodes
  - Giant Magneto-Resistive Sensor
  - Hall Element

  Various Drawbacks

  Losses, No Galvanic Isolation, Low Signal-to-Noise Ratio (SNR), Size, Bandwidth, Realization Effort

  - Saturable Inductor

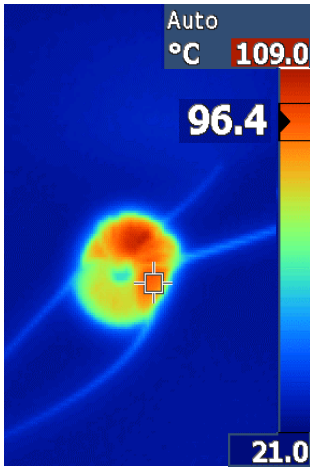


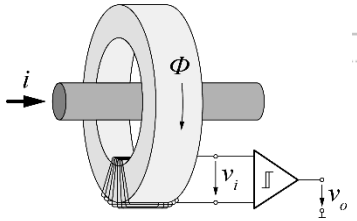


- Galvanic Isolation, High SNR, Small Size, High Bandwidth, Simple Design
- Min. Core Volume/Cross Section for Min. Core Losses

i=0 Detection

- Saturable Inductor
  - Toroidal Core — R4 x 2.4 x 1.6, EPCOS (4mm Diameter)
  - Core Material — N30, EPCOS



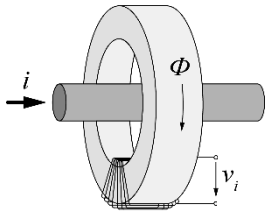


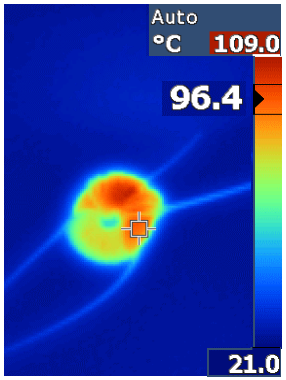
Digital Signal v_o
Induced Voltage v_i
Current i

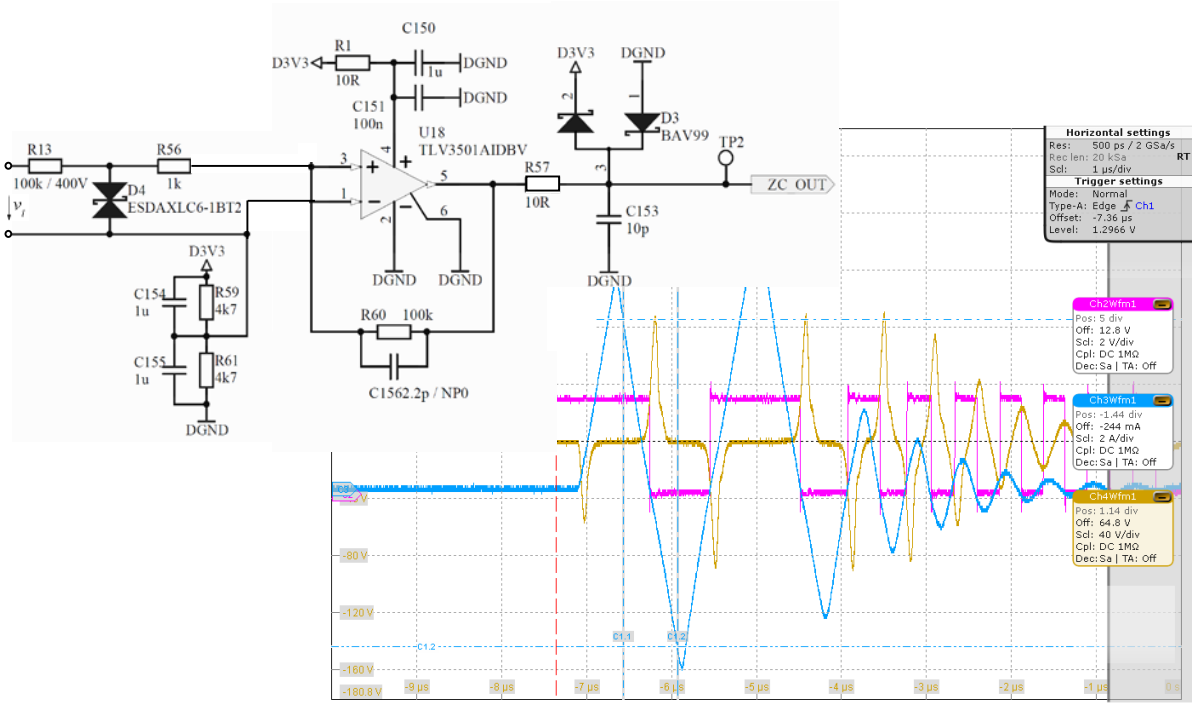
- Operation Tested up to 2.5MHz Switching Frequency

i=0 Detection

- Saturable Inductor – Toroidal Core R4 x 2.4 x 1.6, EPCOS (4mm Diameter)
  – Core Material N30, EPCOS





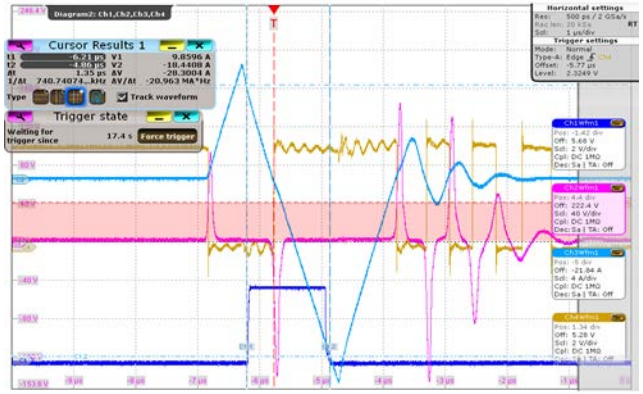


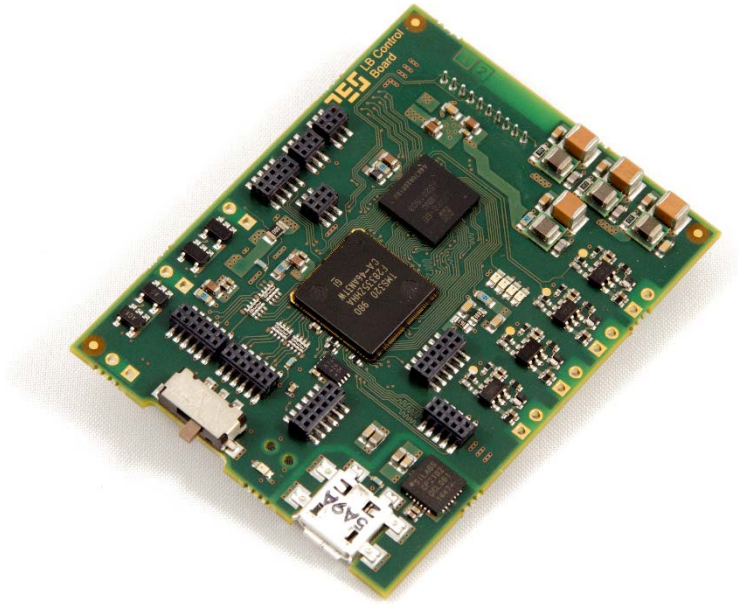
- Operation Tested up to 2.5MHz Switching Frequency

Control Board & *i=0* Detection

- Fully Digital Control - Overall Control Sampling Frequency of 25kHz
- TI DSC TMS320F28335 / 150MHz / 179-pin BGA / 12mm x 12mm
- Lattice FPGA LFXP2-5E / 200MHz / 86-pin BGA / 8mm x 8mm

- TCM Current / Induced Voltage / Comparator Output



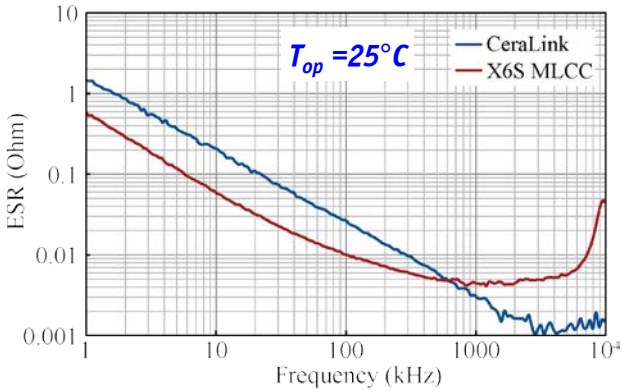


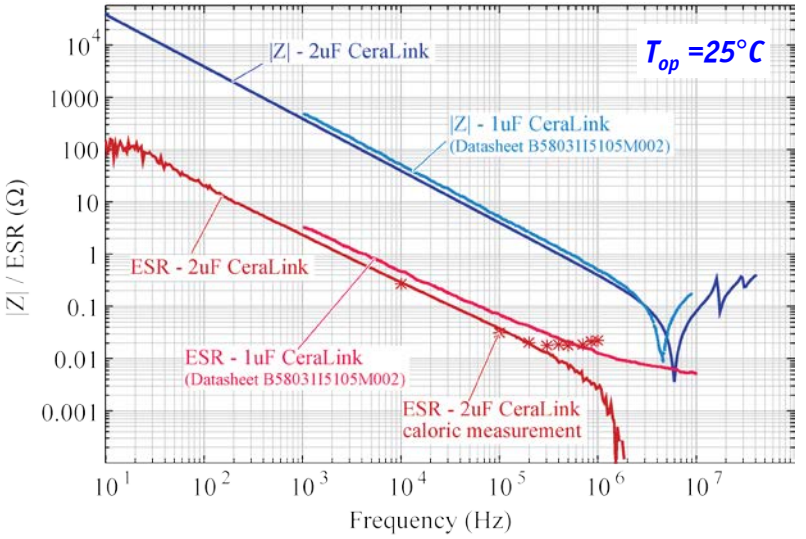
- *i=0* Detection of TCM Currents Using R4/N30 Saturable Inductors
- Galv. Isolated / Operates up to 2.5MHz Switching Frequency / <10ns Delay

Active Power Pulsation Buffer Capacitor

- Electrolytic Capacitors – Limited by Lifetime-Relevant Current Limit
- 2.2µF, 450 V Class II X6S MLCC – Highest Energy Density but Cap. Decreases with DC Bias

- Novel 1 µF /2 µF, 650 V CeraLink™ Cap. (PLZT Ceramic) Features High Cap. @ High DC Bias
- Allows 125°C Operating Temp. & Shows Very Low ESR @ High Frequencies



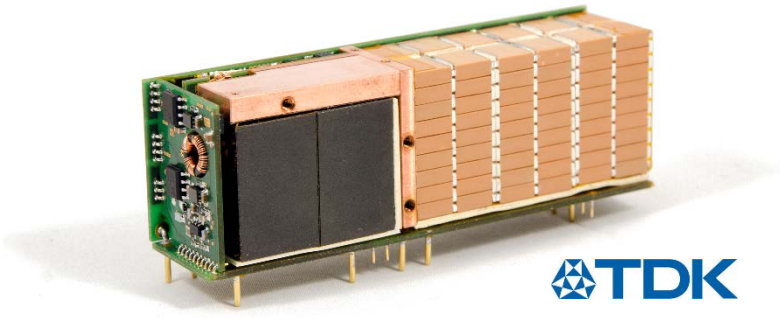


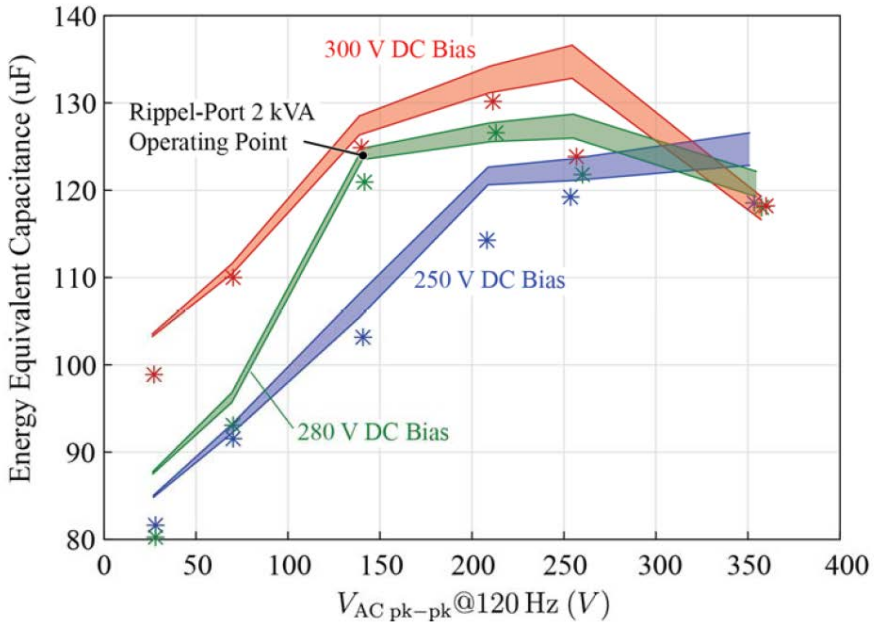
- CeraLink Resonance Frequency at Several MHz
- Small-Signal ESR of CeraLink in MHz Frequ. Range Sign. Lower Comp. to X6S MLCC

Final Active Power Pulsation Buffer

- High Energy Density 2nd Gen. 400VDC CeraLink Capacitors Utilized as Energy Storage
- Highly Non-Linear Behavior → Optimal DC Bias Voltage of 280VDC
- Losses of 6W @ 2kVA Output Power

- 108 x 1.2µF /400 V
- 23.7cm³ Capacitor Volume

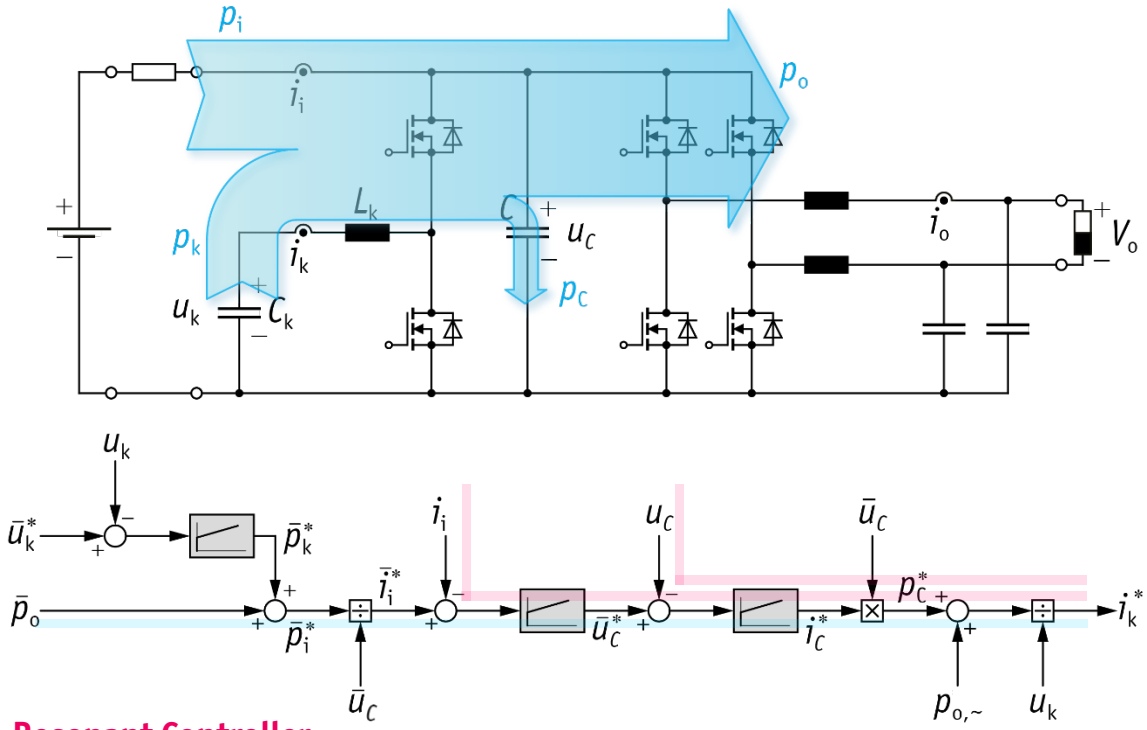




- Effective Large Signal Capacitance of C ≈160µF

Active Power Pulsation Buffer Control (1)

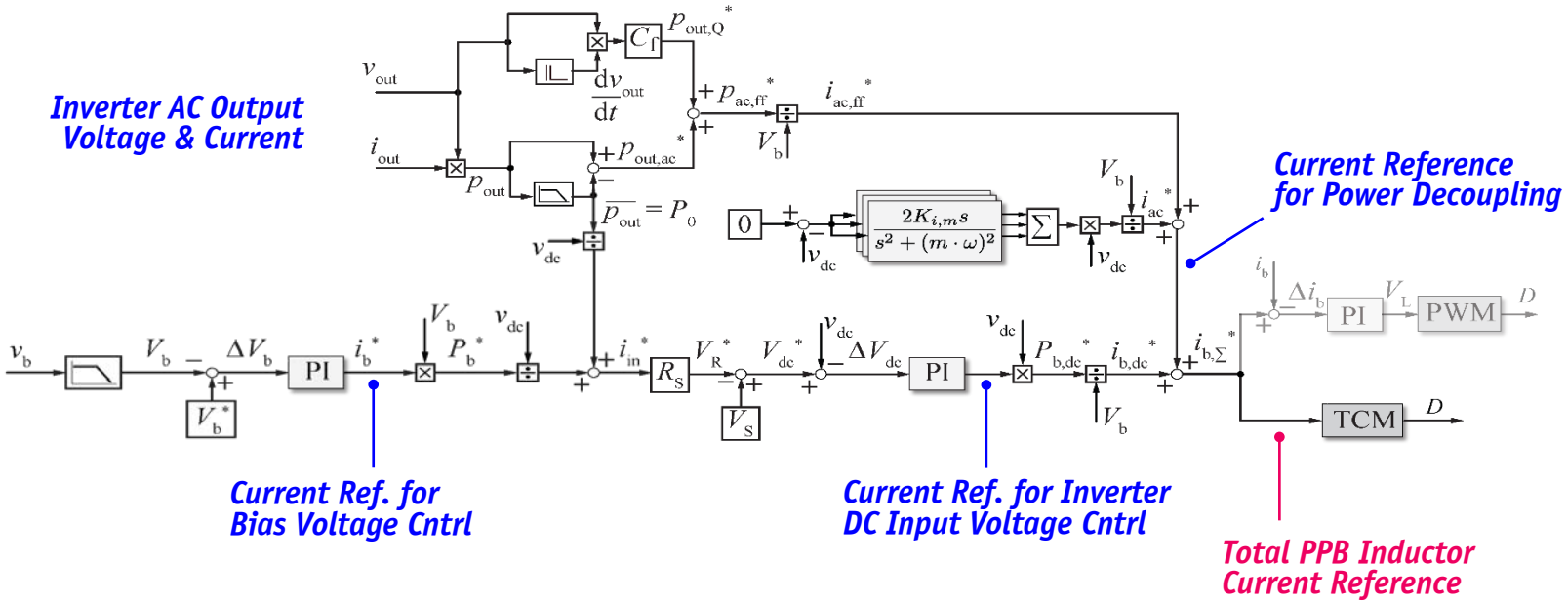
- New Cascaded Control Structure



- P-Type Resonant Controller
- Feedforward of Output Power Fluctuation
- Underlying Input Current (i_i) / DC Link Voltage (u_C) Control

Active Power Pulsation Buffer Control (2)

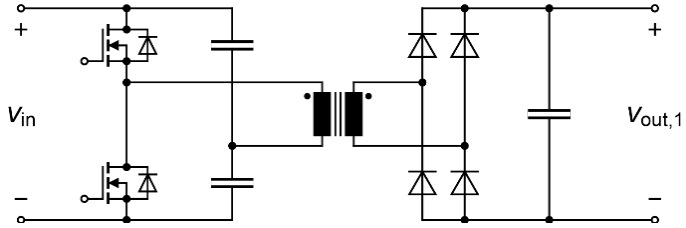
- Multiple Controller Outputs Combined in a Single Current Reference

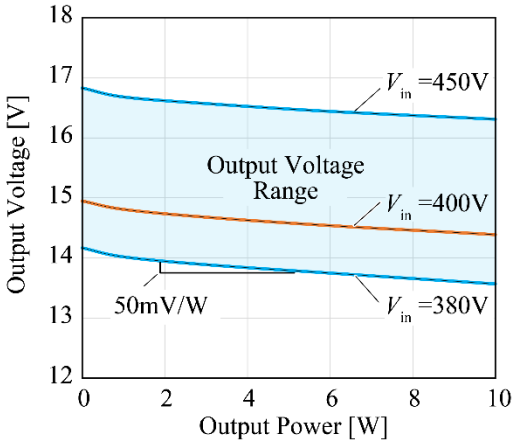


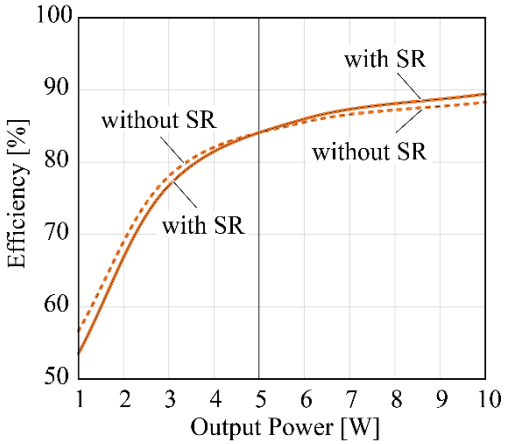
- Regulation of Mean Buffer Voltage (Bias Voltage)
- Tight Control of Inverter DC Link Voltage also During Transients
- Active Power Decoupling – Rejection of 2 x Line-Frequ. Ripple in Inverter DC Input Voltage

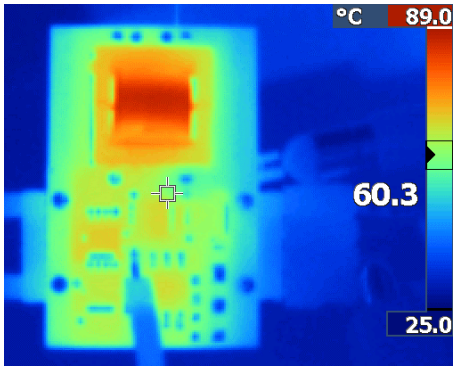
Auxiliary Supply

- Constant 50% Duty Cycle Half Bridge w. Diode Rect. or Synchr. Rectification (SR)
- ZVS → Compact / Efficient / Low EMI









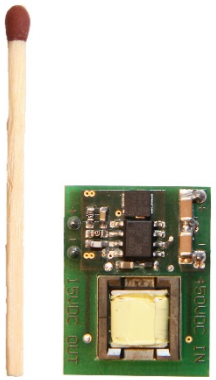
@ V_{in} = 380V, P_{out} = 10W

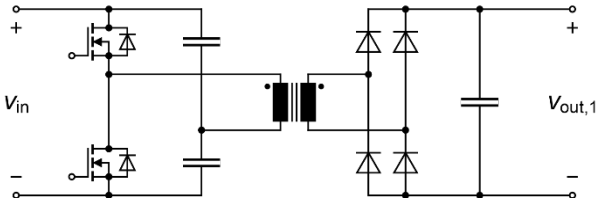
- Only Marginal Eff. Gain with Synchr. Rectification for Output Power Levels > 5W

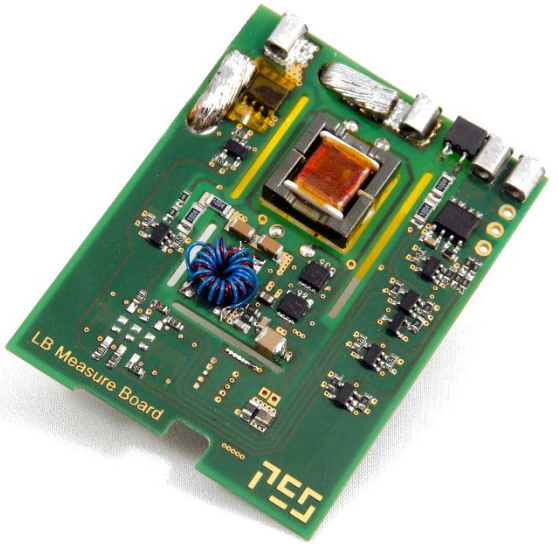
Auxiliary Supply & Measurement Circuits

- Constant 50% Duty Cycle Half Bridge with Synchr. Rectification
- ZVS → Compact / Efficient / Low EMI (f_s=465 kHz)

- 10W Max. Output Power
- 390V...450V Input Operating Range
- 13.8V...16.8V DC Output in Full Inp. Voltage / Output Power Range
- 90% Efficiency @ P_{max}





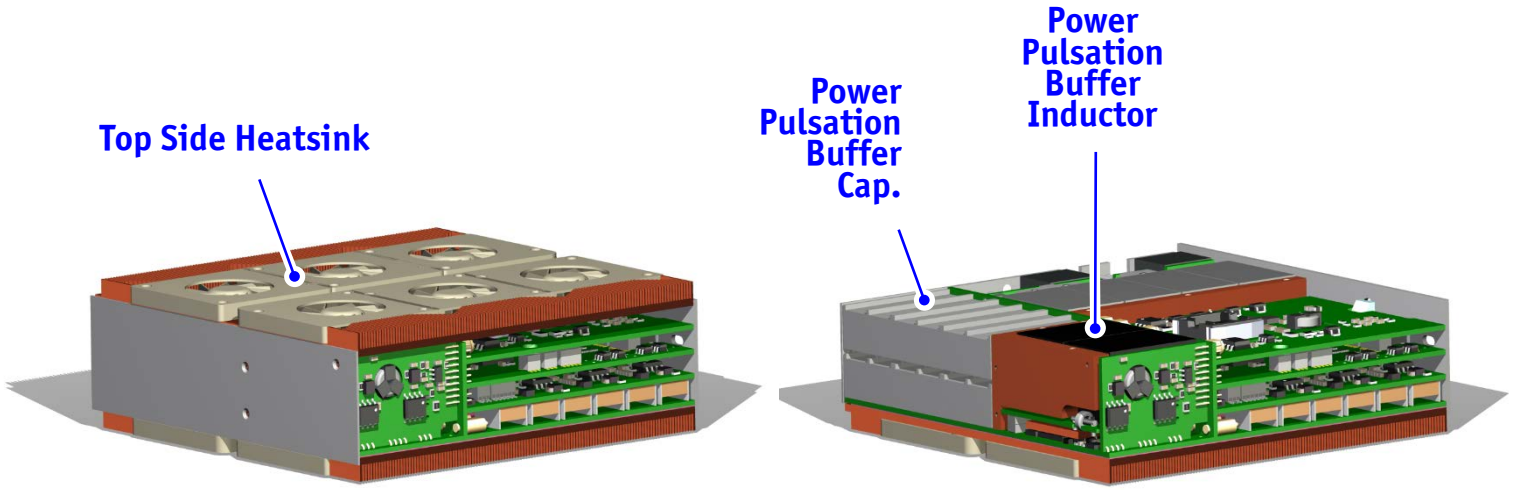


- 19mm x 24mm x 4.5mm (2cm^3 Volume)

3D-CAD Construction →

Mechanical Construction (1)

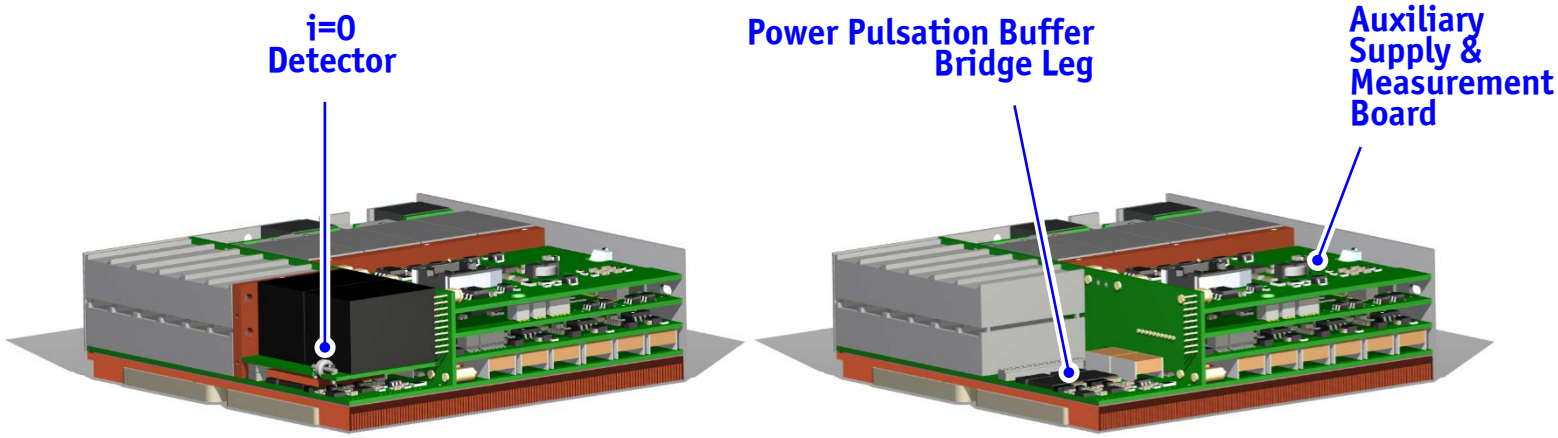
- Built to the Power Density Limit @ η= 95% / T_c < 60°C



- 88.7mm x 88.4mm x 31mm = 243cm³ (14.8in³) → 8.2 kW/dm³

Mechanical Construction (2)

- Built to the Power Density Limit @ η= 95% / T_c < 60°C



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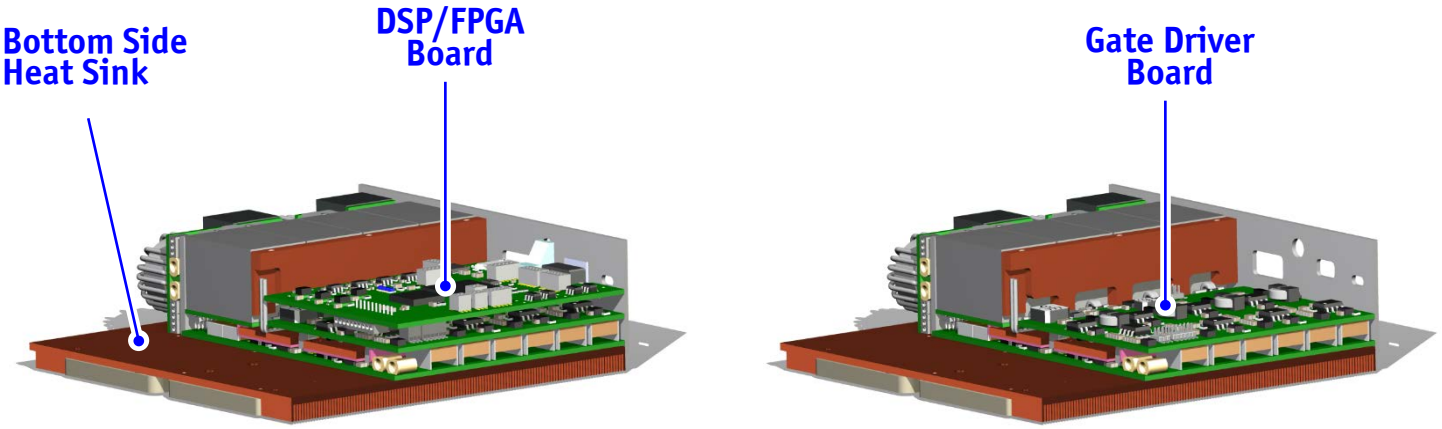

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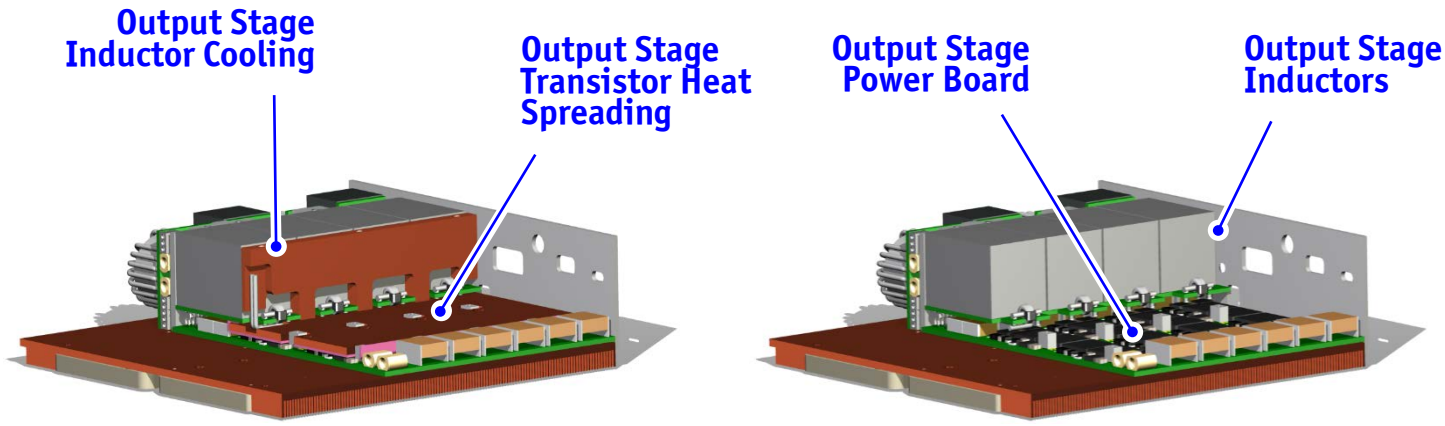
Mechanical Construction (4)

- Built to the Power Density Limit @ η= 95% / T_c < 60°C



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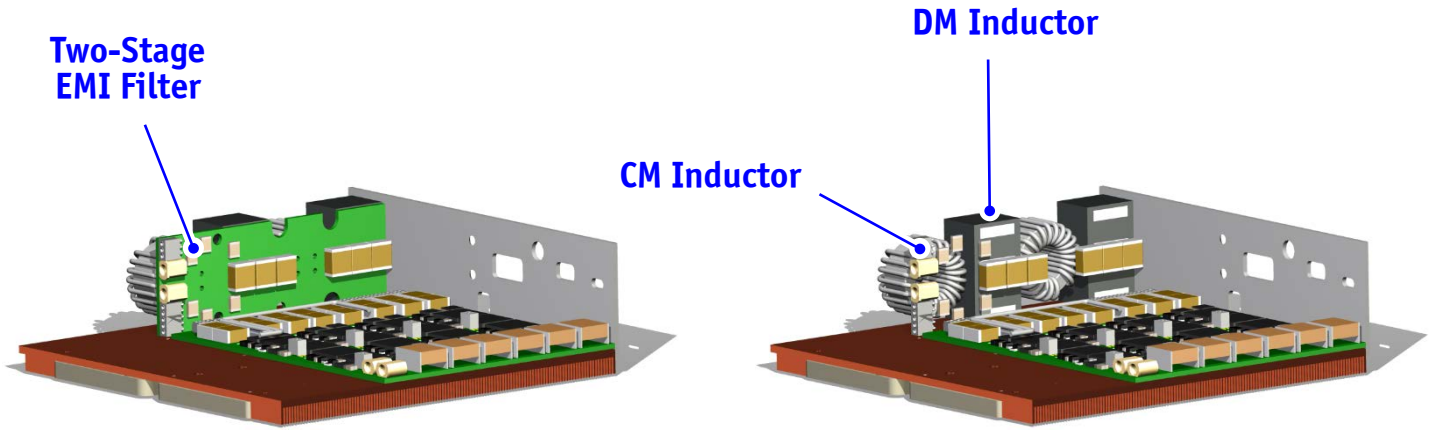
Mechanical Construction (5)

- Built to the Power Density Limit @ η= 95% / T_c < 60°C



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Experimental Results

Hardware
Output Voltage/Input Current Quality
Thermal Behavior
Efficiency
EMI →

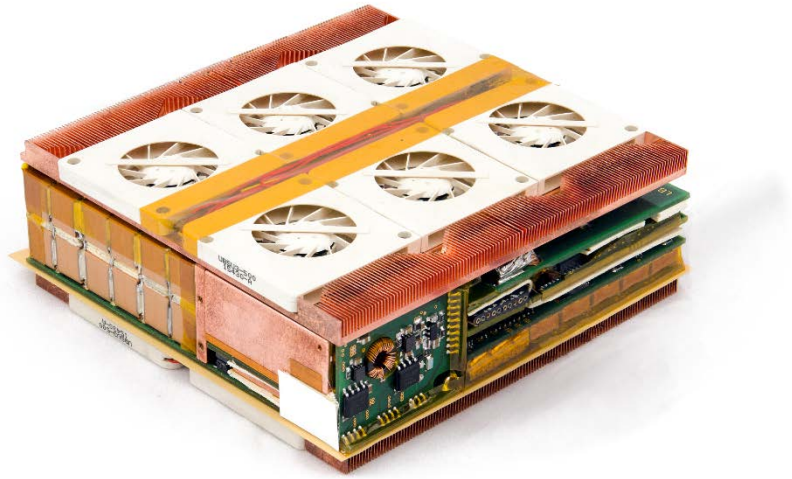
Little Box 1.0 - Prototype

- System Employing Active Ceralink 1-Φ Power Pulsation Buffer

- 8.2 kW/dm³
- 8.9cm x 8.8cm x 3.1cm
- 96,3% Efficiency @ 2kW
- T_c=58°C @ 2kW

- $\Delta u_{DC,pp}$ = 1.1%
- $\Delta i_{DC,pp}$ = 2.8%
- $THD+N_U$ = 2.6%
- $THD+N_I$ = 1.9%

★ 135 W/in³



- Compliant to All *Original* Specifications (!)

- No Low-Frequ. CM Output Voltage Component
- No Overstressing of Components
- All Own IP / Patents

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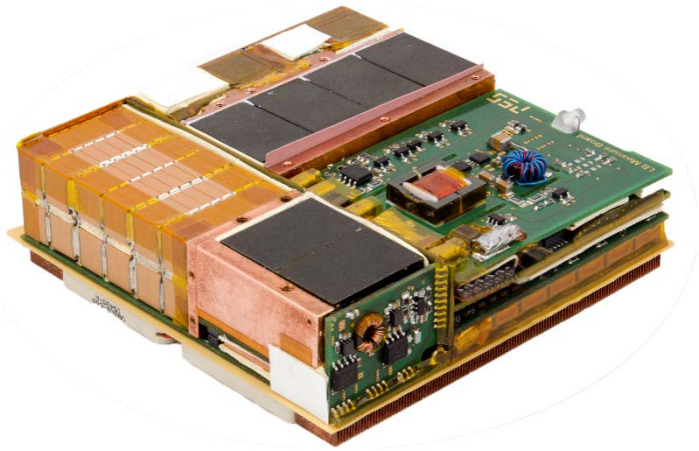

■ Compliant to All *Original* Specifications (!)

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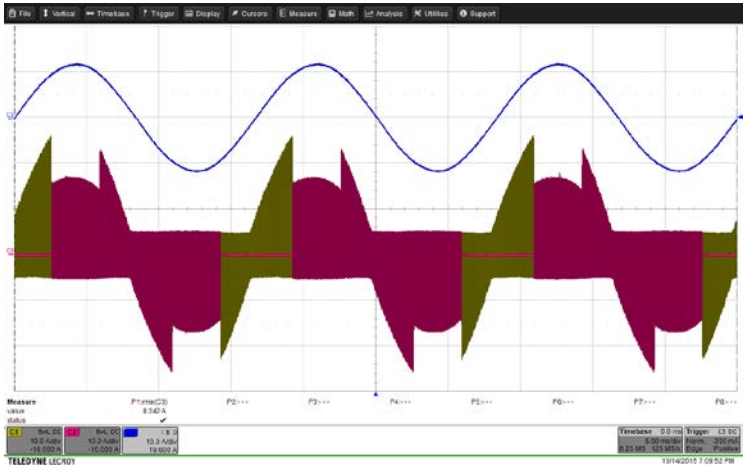
- No Overstressing of Components
- All Own IP / Patents

Little Box 1.0 Measurement Results (1)

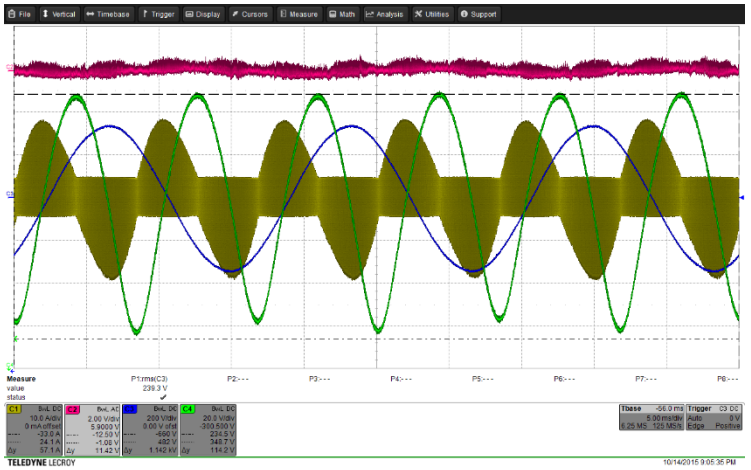
- System Employing Active Ceralink 1-Φ Power Pulsation Buffer

- Ohmic Load / 2kW

Output Current (10 A/div)
Inductor Current Bridge Leg 1-1 (10 A/div)
Inductor Current Bridge Leg 1-2 (10 A/div)



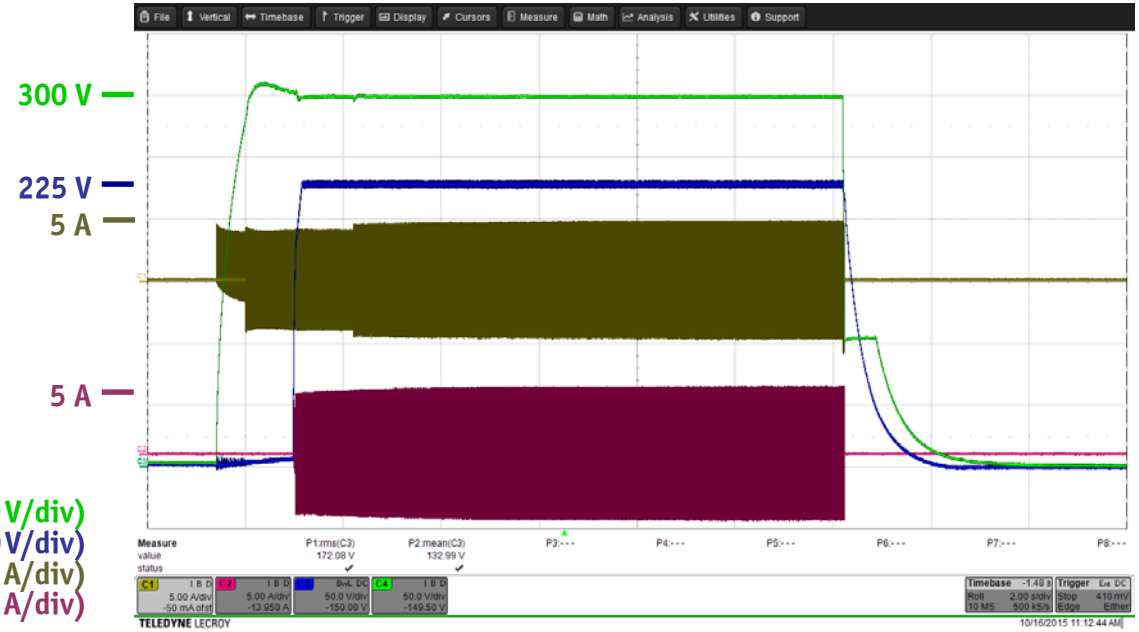
DC Link Voltage (AC-Coupl., 2 V/div)
Buffer Cap. Voltage (20 V/div)
Buffer Cap. Current (10 A/div)
Output Voltage (200 V/div)



- Compliant to All Specifications

Little Box 1.0 Measurement Results (2)

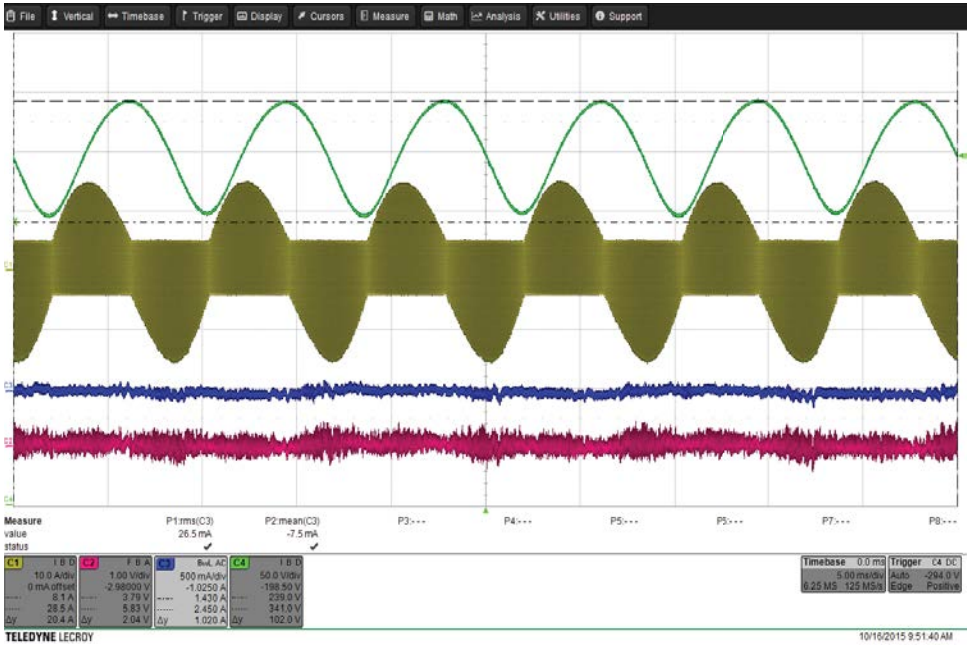
- System Employing Active Ceralink 1-Φ Power Pulsation Buffer



- Start-up and Shut-Down (No Load Operation)

Little Box 1.0 Measurement Results (3)

- System Employing Active Ceralink 1-Φ Power Pulsation Buffer



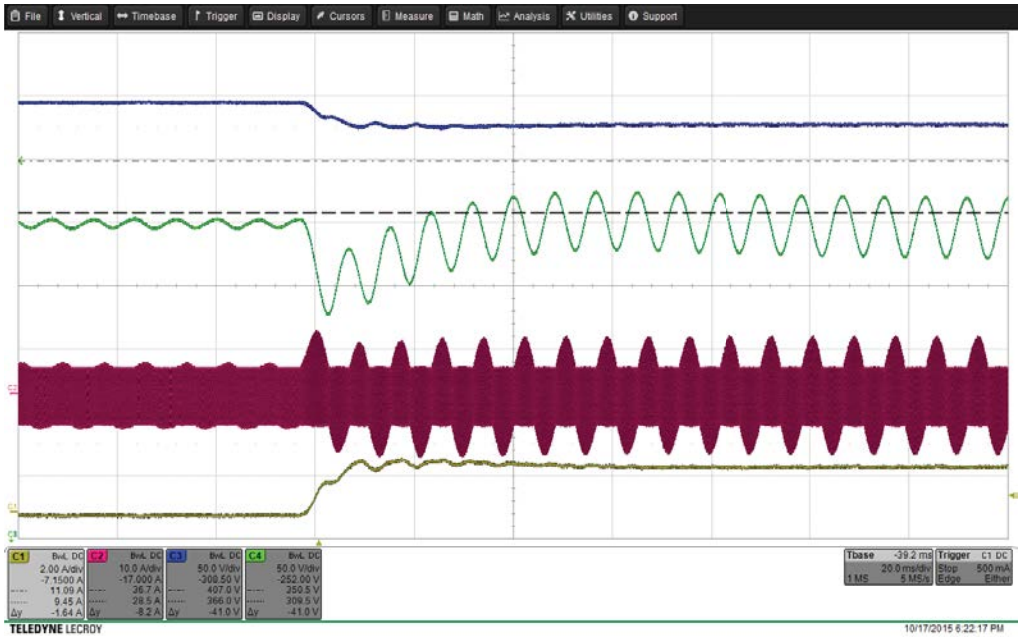
Buffer Cap. Voltage (50 V/div)
Buffer Cap. Current (10 A/div)
Conv. Inp. Curr. (AC Coupl. 500 mA/div)
DC Link Voltage (AC Coupl. 1 V/div)

- Stationary Operation @ 2kW Output Power

Little Box 1.0 Measurement Results (4)

- System Employing Active Ceralink 1-Φ Power Pulsation Buffer

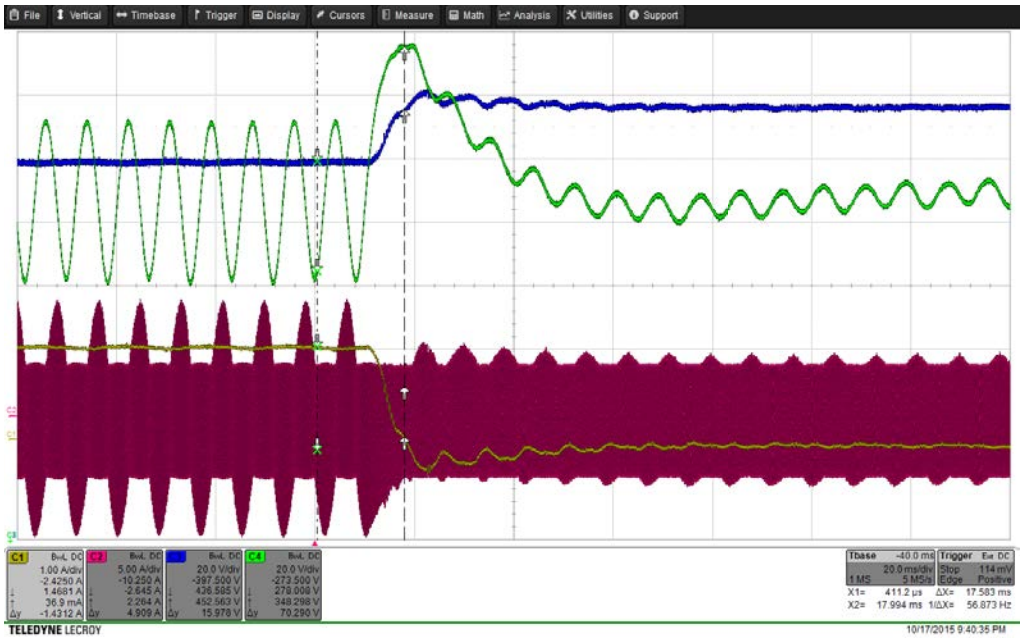
DC Link Voltage (50 V/div)
Buffer Cap. Voltage (50 V/div)
Buffer Cap. Current (10 A/div)
Conv. Input Current (2 A/div)



- Transient Response for Load-Step of 0 Watt → 700 Watt

Little Box 1.0 Measurement Results (5)

- System Employing Active Ceralink 1-Φ Power Pulsation Buffer

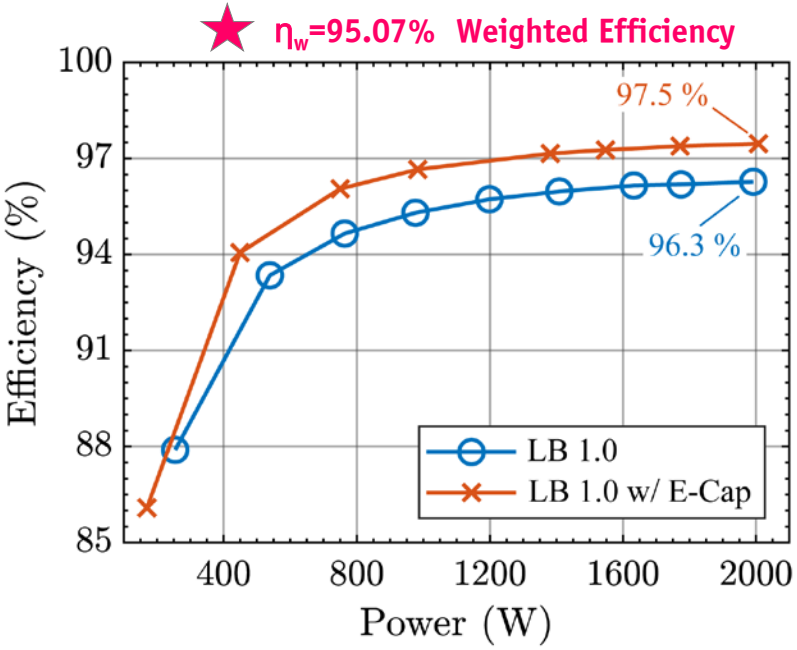


DC Link Voltage (20 V/div)
Buffer Cap. Voltage (20 V/div)
Buffer Cap. Current (5 A/div)
Conv. Input Current (1 A/div)

- Transient Response for Load-Step of 700 Watt → 0 Watt

Little Box 1.0 Measurement Results (6)

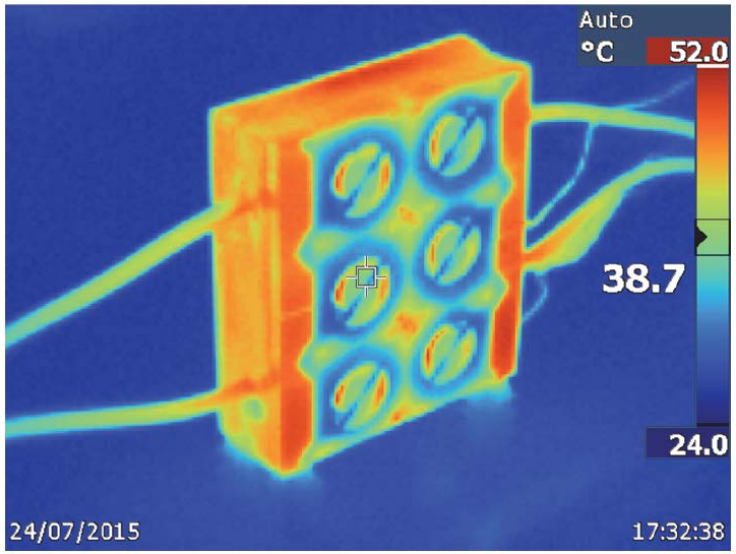
- System Employing Active Ceralink 1-Φ Power Pulsation Buffer



- Compliant to All Specifications

Little Box 1.0 - Measurement Results (6)

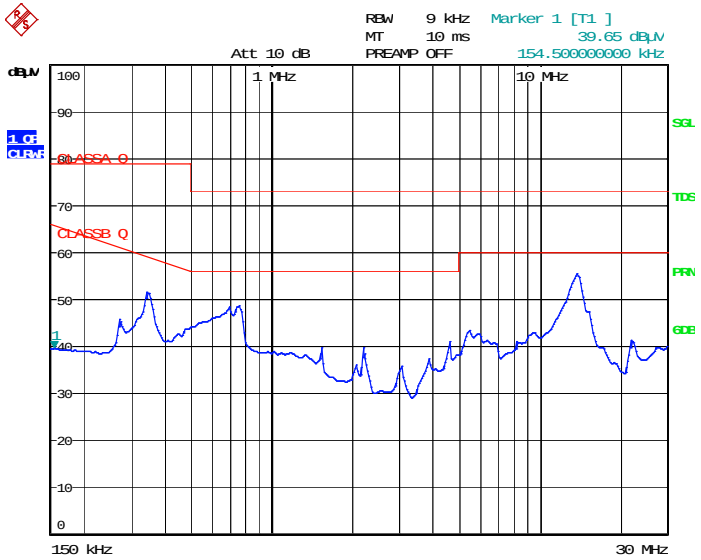
- CSPI = 37 W/(dm³.K)
- 30mm Blowers with Axial Air Intake / Radial Outlet
- Full Optimization of the Heatsink Parameters



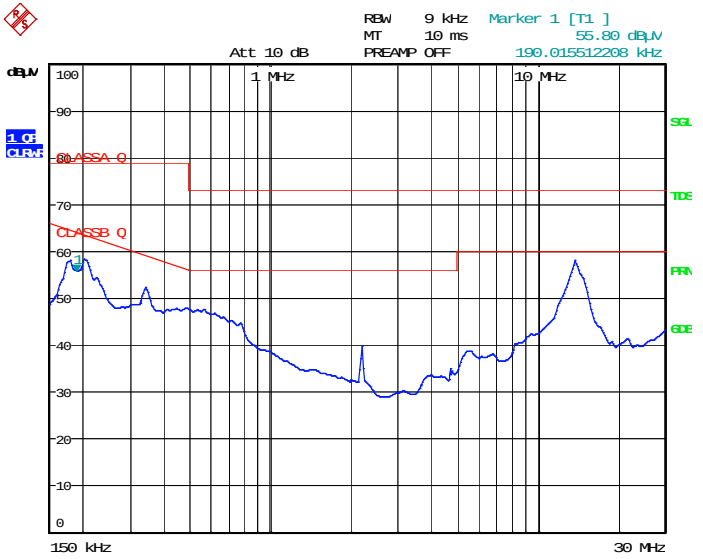
- $CSPI_{eff}$= 25 W/(dm³.K) Considering Heat Distribution Elements
- Two-Side Cooling → Heatsink Temperature = 52°C @ 2kW Output Power (74 W Loss)

Little Box 1.0 Measurement Results (7)

P_{out}= 400W



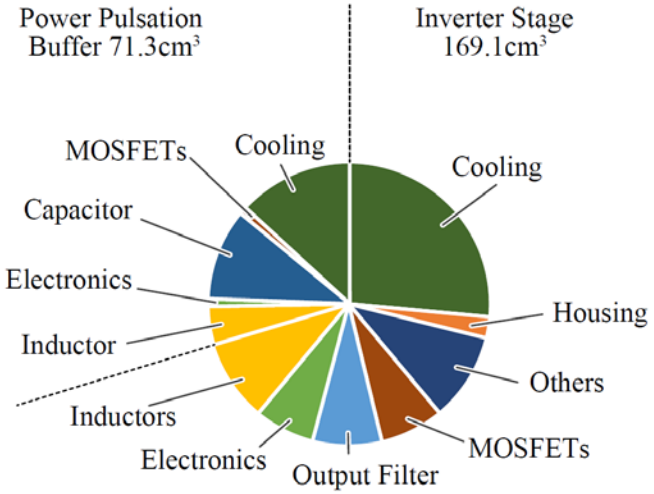
P_{out}= 2kW



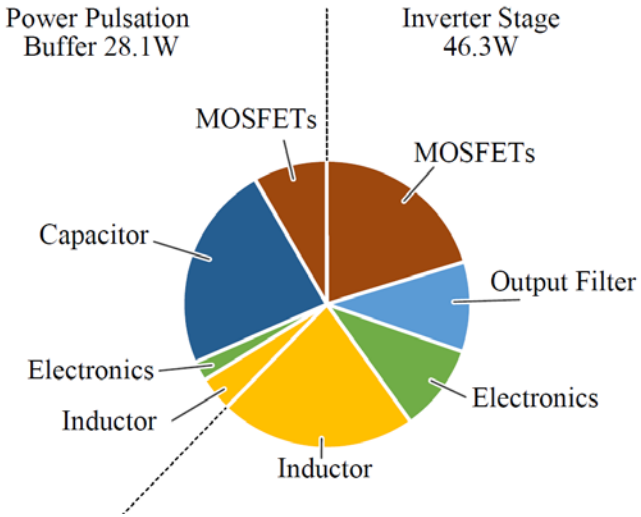
- Compliant to All Specifications

Little Box 1.0 Volume and Loss Distribution

- Volume Distribution (240cm³)



- Loss Distribution (75W)



- Large Heatsink (incl. Heat Conduction Layers)
- Large Losses in Power Fluctuation Buffer Capacitor (!)
- TCM Causes Relatively High Conduction & Switching Losses @ Low Power
- Relatively Low Switching Frequency @ High Power – Determines EMI Filter Volume

Other Finalists

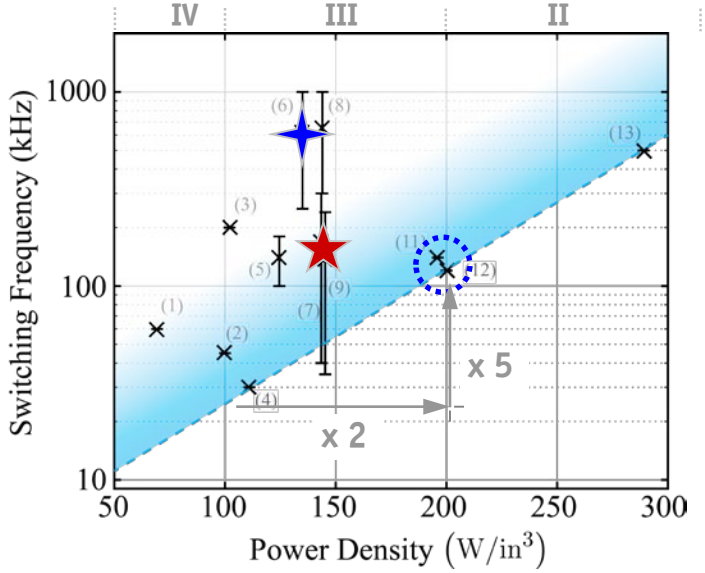
Topologies
Switching Frequencies
Power Density / Efficiency Comparison →

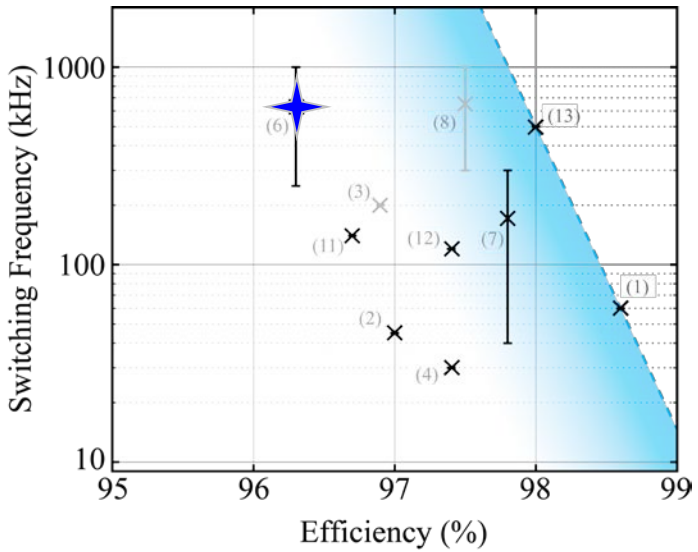
Detailed Descriptions:
www.LittleBoxChallenge.com

Finalists - Performance Overview

- **18 Finalists (3 No-Shows)**
- 7 Groups of Consultants / 7 Companies / 4 Universities

Note: Numbering of Teams is Arbitrary





- **70…300 W/in³**
- **35 kHz…500kHz…1 MHz** (up to 1MHz: 3 Teams)
- Full-Bridge or DC/|AC|Buck Converter + Unfolder
- Mostly Buck-Type Active Power Pulsation Filters (Ceramic Caps of Electrolytic Caps)
- **GaN (11 Teams)** / SiC (2 Teams) / Si (2 Teams)

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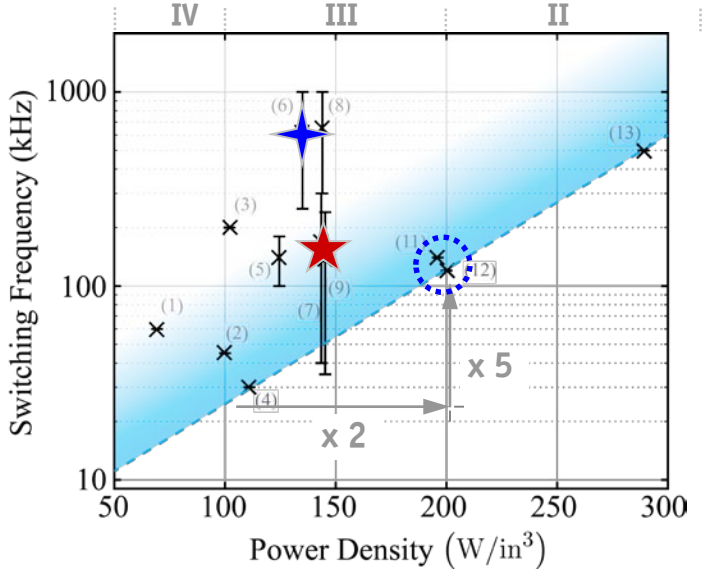

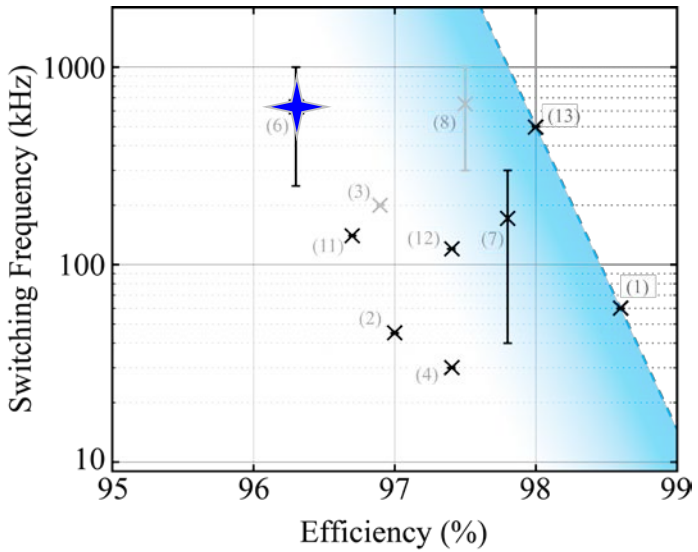

(1) Virginia Tech
(2) Schneider Electric
(3) EPRI (Univ. of Tennessee)
(4) Venderbosch
(5) Energy Layer
(6) ETH Zurich
(7) Rompower
(8) Tommasi-Bailly
(9) Red Electric Devils
(10) AHED
(11) FH IISB
(12) Univ. of Illinois
(13) AMR
(14) OKE
(15) Cambridge Magnetics

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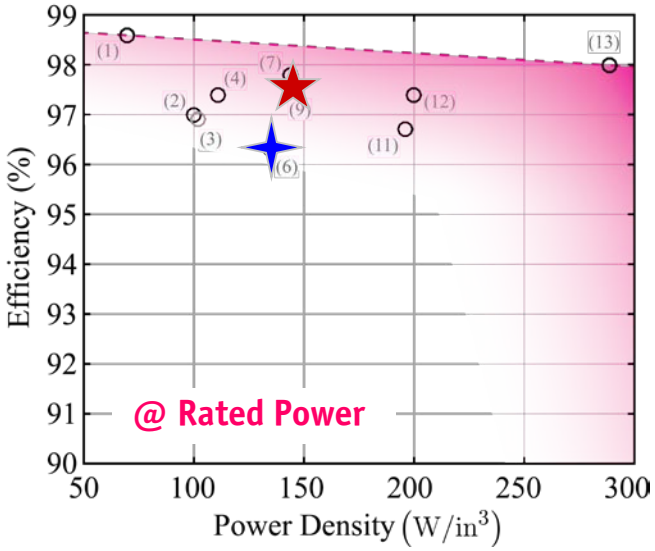

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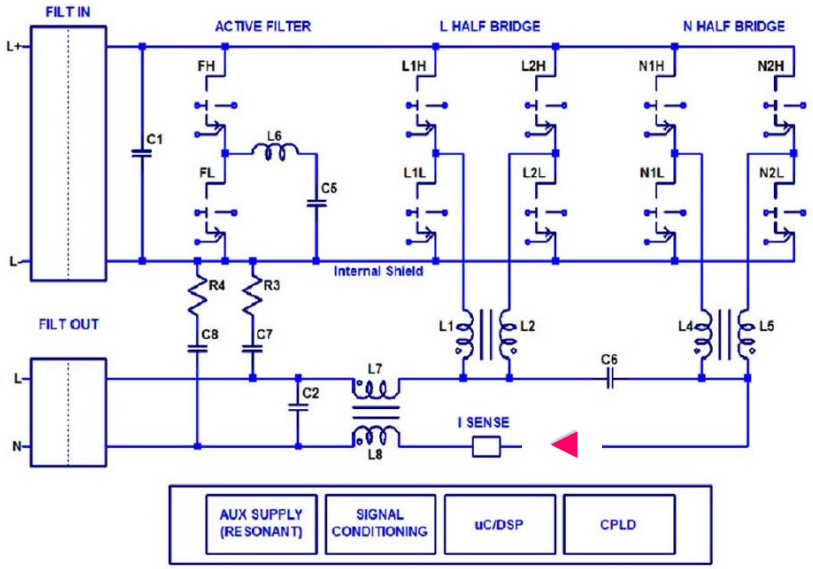
Red Electric Devils

★ 145 W/in³

- No Low-Frequ. Common-Mode Output Voltage Comp. → i_{gnd} < 5mA (!)
- Buck-Type DC-Side Active Power Pulsation Filter (MLCC Cap. <150µF, 200V_{pp})



- 2 x Interleaved Bridge Legs for Each Half-Bridge
- DM Inductors (L_1/L_2 and L_4/L_5) and Series Connected CM Inductor (L_7/L_8)
- Single Open-Loop Hall Sensor Outp. Curr. Measurement + Observer-Based Curr. Reconstruction

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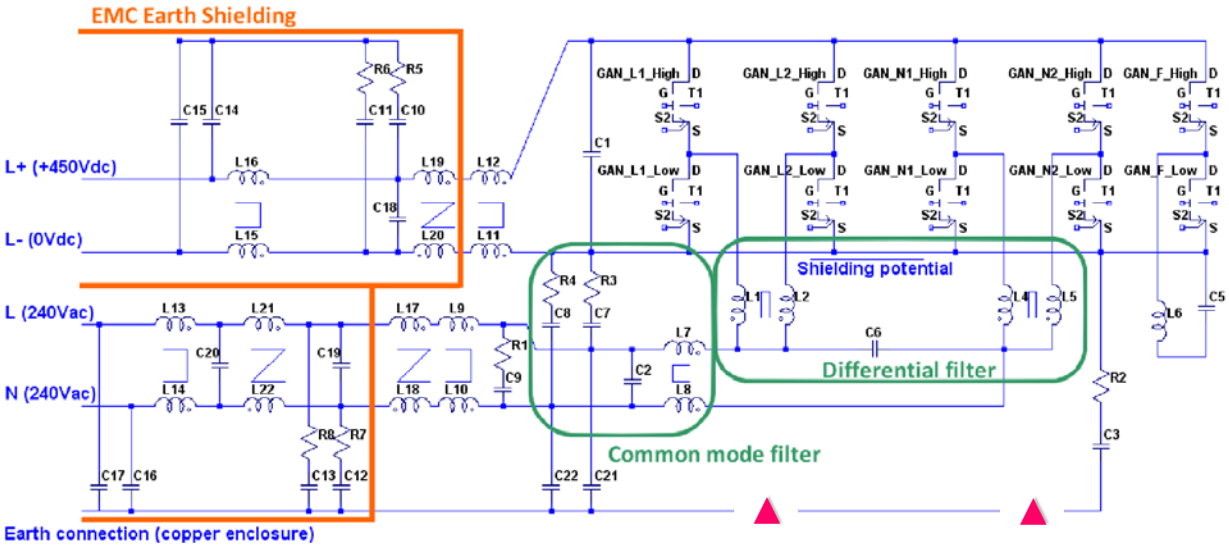
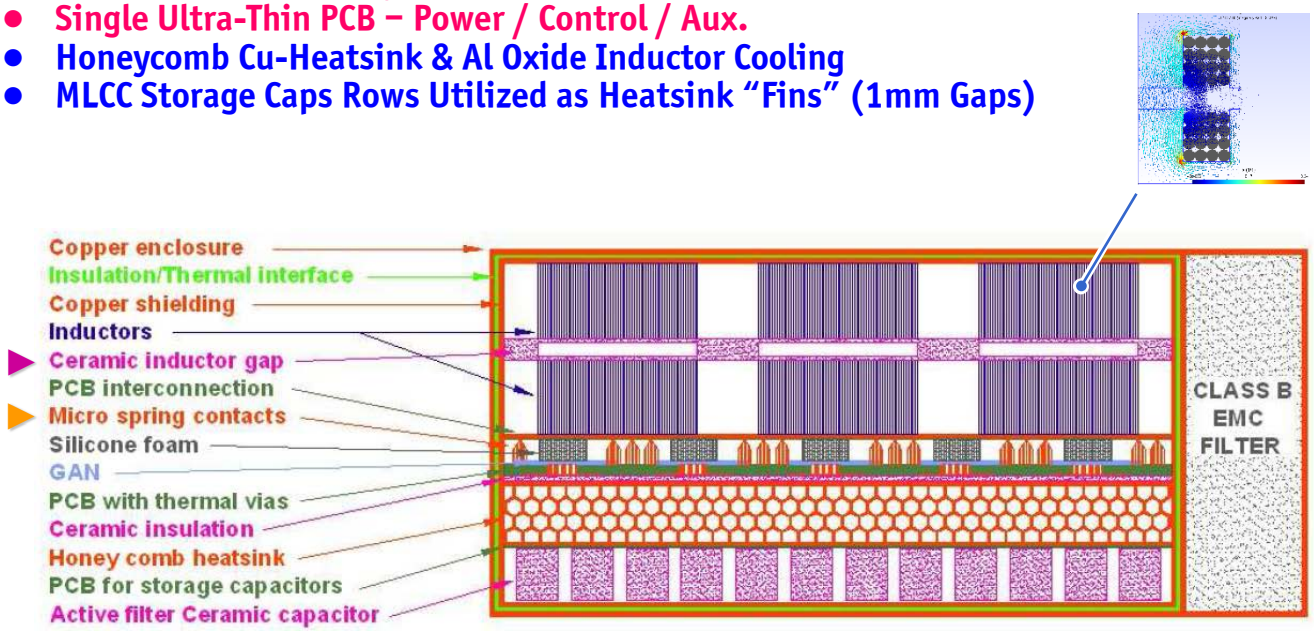


- DSP & CPLD Control
- GaN Systems @ ZVS (35kHz ... 240kHz)
- Shielded Multi-Stage EMI Filter @ DC Input & AC Output

Red Electric Devils

★ 145 W/in³

- 3D Sandwich Assembly
- Single Ultra-Thin PCB – Power / Control / Aux.
- Honeycomb Cu-Heatsink & Al Oxide Inductor Cooling
- MLCC Storage Caps Rows Utilized as Heatsink "Fins" (1mm Gaps)



- 145 W/in³
- 95.4 % CEC Efficiency
- i_{gnd} < 5mA (!)
- CSPI = 22.6 W/(dm³.K) - Heatsink & Axial Fan

Red Electric Devils

★ 145 W/in³

- 3D Sandwich Assembly
- Single Ultra-Thin PCB – Power / Control / Aux.
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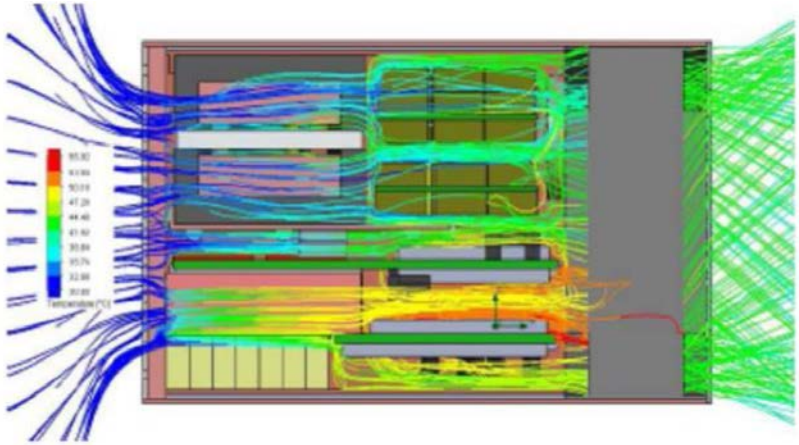
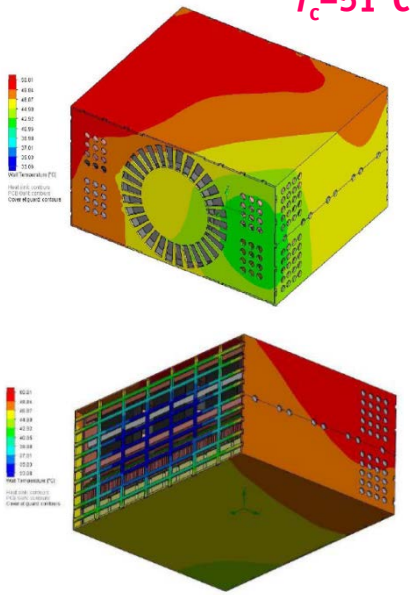


T_c=51°C



- 145 W/in³
- 95.4 % CEC Efficiency
- i_{gnd} < 5mA (!)
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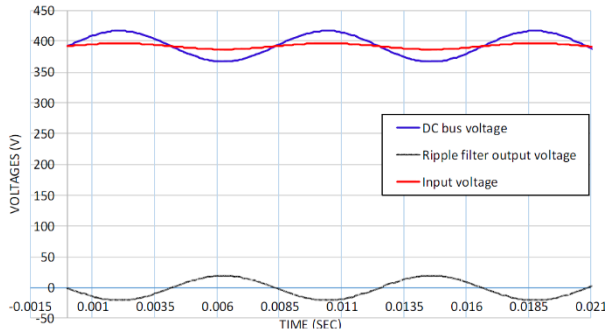
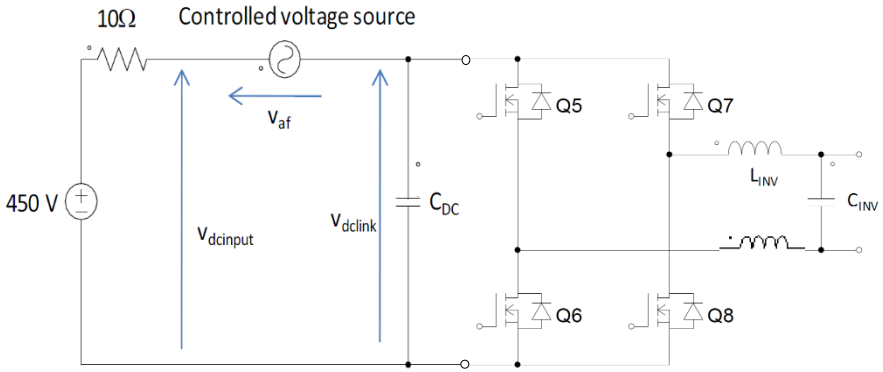
Schneider Electric Global Team

★ 100 W/in³

- High Efficiency & Robustness Preferred → Larger Size
- DC-Side Series (!) Active Power Puls. Filter → Compensates 120Hz DC Link Volt. Variation





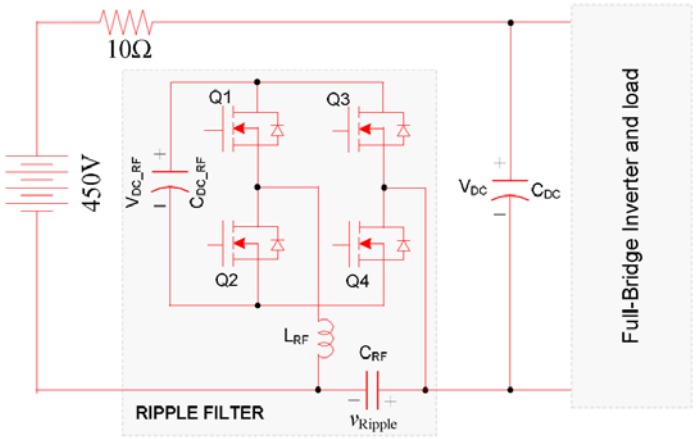
- C_{DC} = 400uF / 450V
- 1/5 Volume Comp. to only Bulk Capacitors
- $V_{dcinput}$ Ripple <10% (<30V_{pp}) @ Full Load

- Nanocrystalline CM Choke
- DC-Side & AC-Side EMI/RF Filter
- $Q_{5...8}$ – TO247 SiC MOSFETs, 45kHz of Both Legs

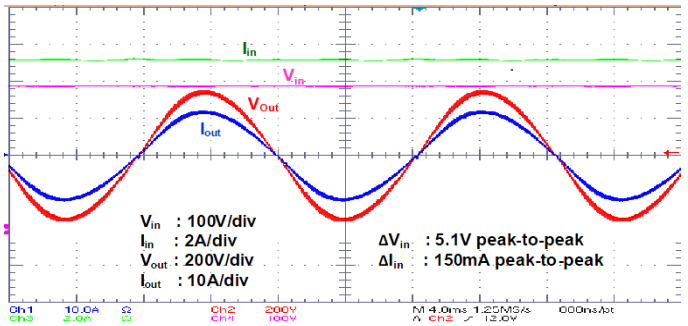
Schneider Electric Global Team

★ 100 W/in³

- High Efficiency & Robustness Preferred → Larger Size
- PWM of Both Legs of Output Full-Bridge → No Low. Frequ. CM Output Voltage Comp.
- DC-Side Series (!) Active Power Puls. Filter → Compensates 120Hz DC Link Volt. Variation



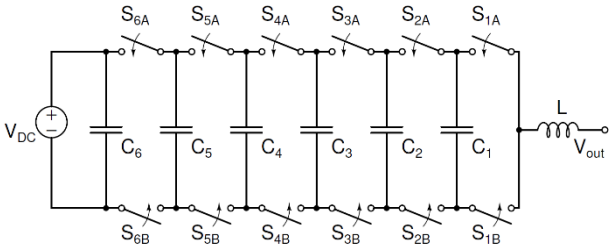
- i_{gnd} < 25mA (!)
- 97.2 % CEC Efficiency

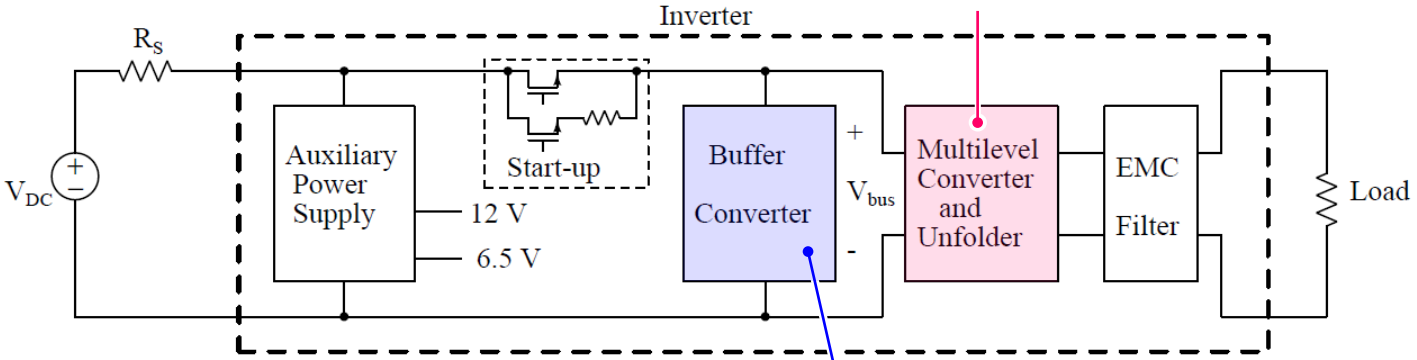


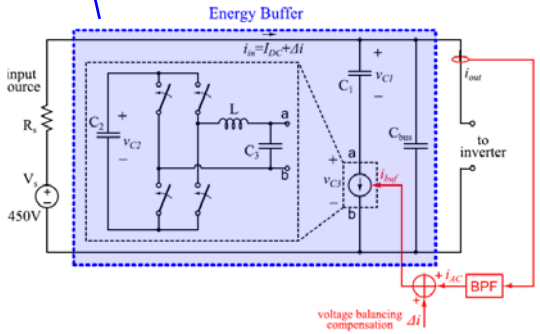
- C_{DC_RF}=2 x 1500uF/25V, U_{DC_RF}=15V
- Only 52VA Processed Ripple Filter Power @ Rated Output (!)
- Q_1/Q_2 & Q_3/Q_4 - $R_{ds,on}$= 2.2mΩ MOSFETs (40V, 100A), w/o Heatsink, f_S= 130kHz of Both Legs
- TI Piccolo DSP Control of Entire System / Open Loop Control of 120Hz Comp. Filter

Prof. Pilawa-Podgurski & Team

- 7-Level Flying Capacitor Converter
- Series-Stacked Active Power Buffer







- 216 W/in³
- 100V GaN
- Integrated Switching Cell
- 720kHz Eff. Sw. Frequ. (7 x 120kHz)

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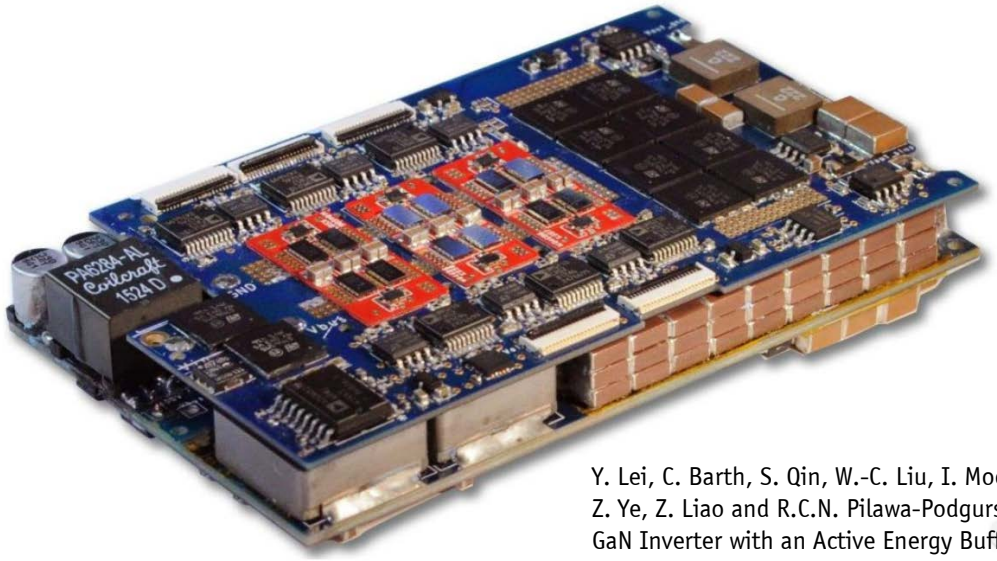

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Y. Lei, C. Barth, S. Qin, W.-C. Liu, I. Moon, A. Stillwell, D. Chou, T. Foulkes, Z. Ye, Z. Liao and R.C.N. Pilawa-Podgurski "A 2 kW, Single-Phase, 7-Level, GaN Inverter with an Active Energy Buffer Achieving 216 W/in^3 Power Density and 97.6% Peak Efficiency", IEEE Applied Power Electronics Conference, Long Beach, CA, 2016

- ***Competition***
- ***Conclusions***
  - ***Key Technologies***
  - ***Power Density Limit*** →

Google Little Box Challenge Summary

Overall

- Engineering "Jewels"
- No (Fundamentally) New Approach / Topology
- Passives & 3D-Packaging are Finally Defining the Power Density
- Careful Heat Management (Adv. Heat Sink, Heat Distrib., 2-Side Integr. Cooling, etc.)
- Careful Mechanical Design (3D-CAD, Single PCB, Avoid Connectors, etc.)
- Clear Power Density / Efficiency Trade-Off

200W/in³ (12kW/dm³) Achievable

- f_s < 150kHz (Constant)
- SiC (Not GaN)
- ZVS (Partial, i.e. Around i=0)
- Full-Bridge Output Stage
- Active Power Pulsation Buffer (Buck-Type, X6S Cap.)
- Conv. EMI Filter Structure
- Multi-Airgap Litz Wire Inductors
- DSP Only (No FPGA)

100+ Teams
3 Members / Team, 1 Year
300 Man-Years
3300 USD / Man-Year

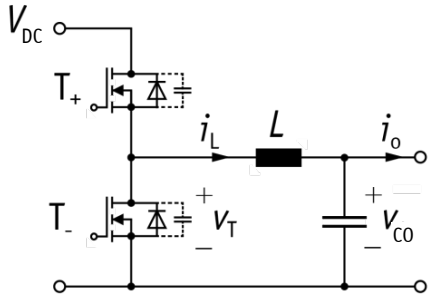
Optimization & Advanced Analysis

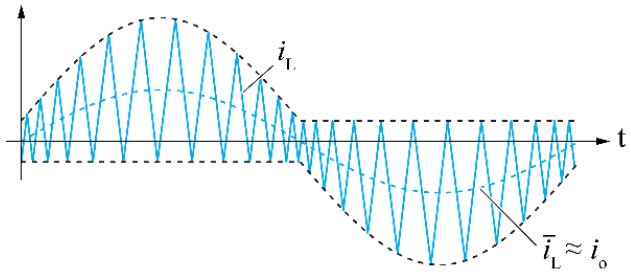
Adv. Modulation / Circuit Concepts
Measurement of Buffer Cap. Performance
Measurement of GaN ZVS & On-State Losses
Measurement of Multi-Airgap Core Losses

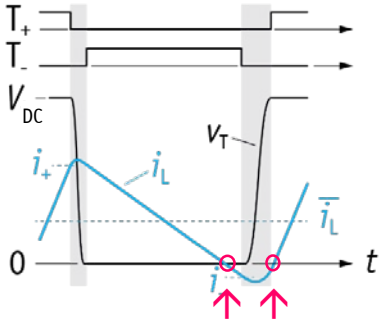
Eff. Optimal f_S-Modulation

- TCM → ZVS but Large Current Ripple & Wide Frequency Variation
- PWM → Const. Sw. Frequency but Hard Sw. @ Current Maximum

- Opt. Combination of TCM & PWM → Optim. Frequ. Variation Over Output Period
- Exp. Determination of Loss-Opt. Sw. Frequency f_{OFM} Considering DC/DC Conv. Stage







- DC/AC Properties Calculated Assuming Local DC/DC Operation
- Loss-Optimal Local Sw. Frequ. f_{OFM} for Given V_{DC} & Local i_0 & v_{CO}

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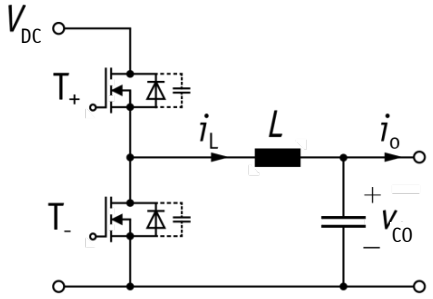

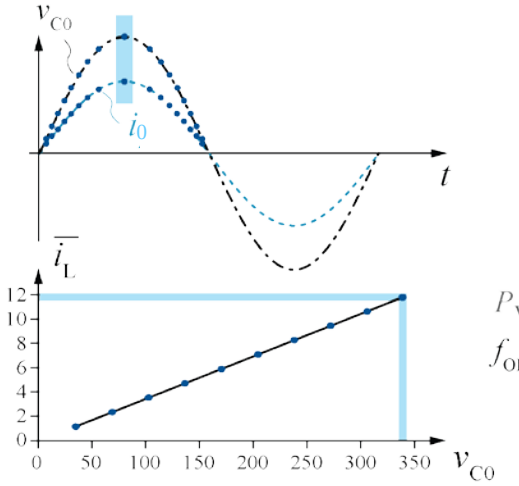

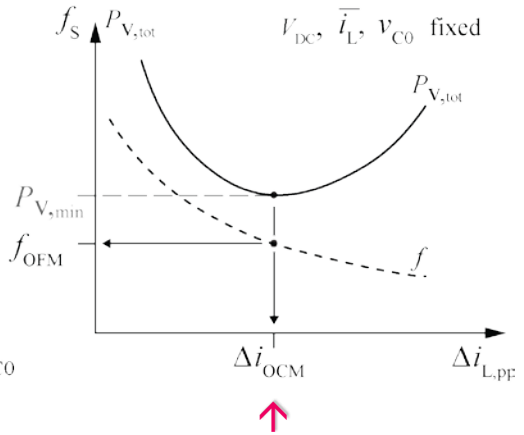

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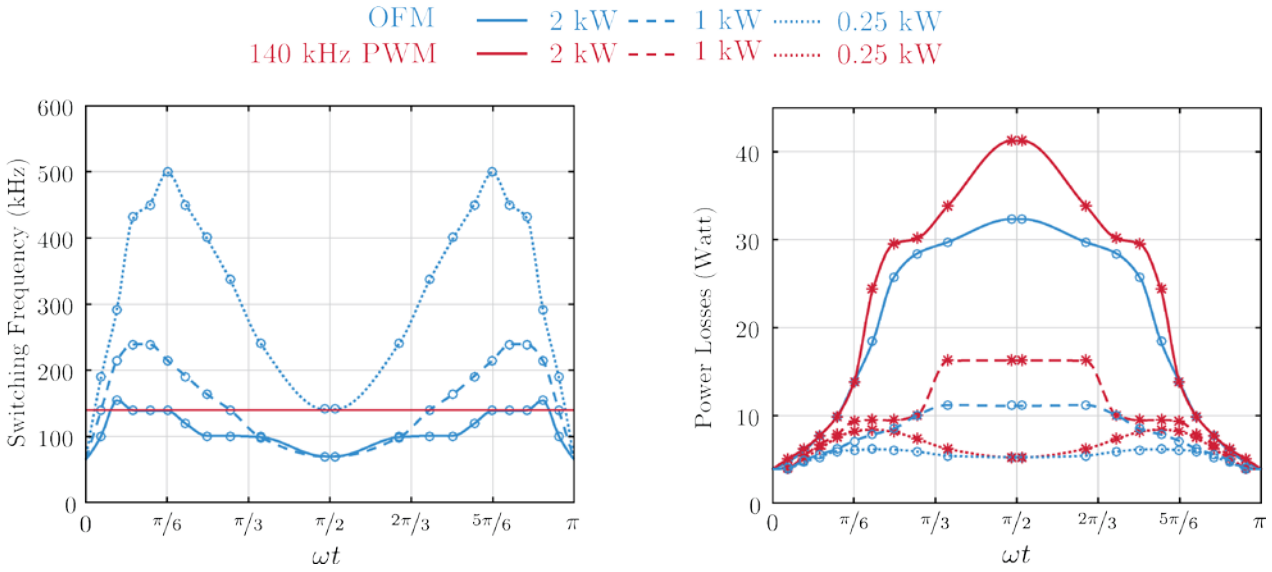
Eff. Optimal f_S-Modulation

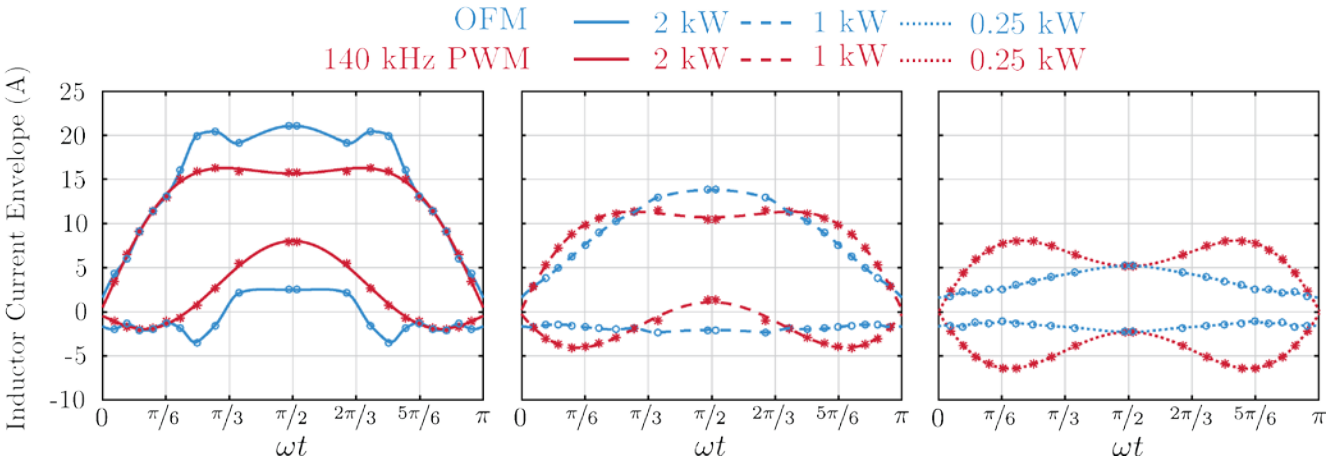
- Resulting Time-Dependency of Optimal Sw. Frequ. & Power Loss
- Comparison with 140 kHz Const. Sw. Frequency PWM



- Higher Average Switching Frequency f_s @ Light Loads
- Reduction of f_s @ Mains Voltage Peak (for Ohmic Load) for Sustaining ZVS

Eff. Optimal f_S-Modulation

- **Optimal Inductor Current Envelope for Diff. Output Power Levels**



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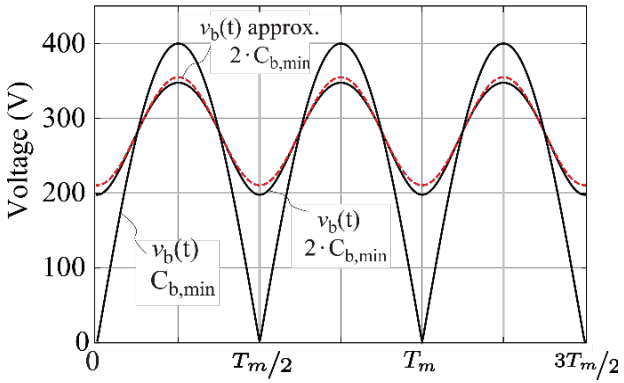
- **Reduction of f_s @ Mains Voltage Peak (for Ohmic Load) for Sustaining ZVS**

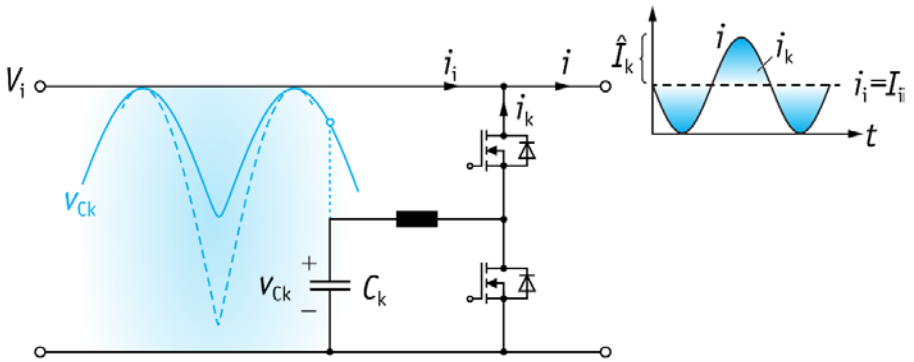
Measurements

Buffer Capacitor Losses / Cap.
Power Semicond. ZVS & On-State Losses
Ferrite Multi-Airgap Core Losses

CeraLink vs. X6S

- Electrolytic Capacitors → Limited by Lifetime Current Limit
- X6S MLCC, 2.2µF, 450 V Class II → Highest Energy Density but Low Cap. @ High DC Bias
- CeraLink™,1µF /2µF, 650 V → PLZT Ceramic, High Cap. @ High DC Bias
- CeraLink™ Allows Op. @ 125°C → Very Low ESR @ High Frequencies





- PPB Design Optimiz. Requires Large-Signal Capacitance and Power Loss Data in All Operating Points

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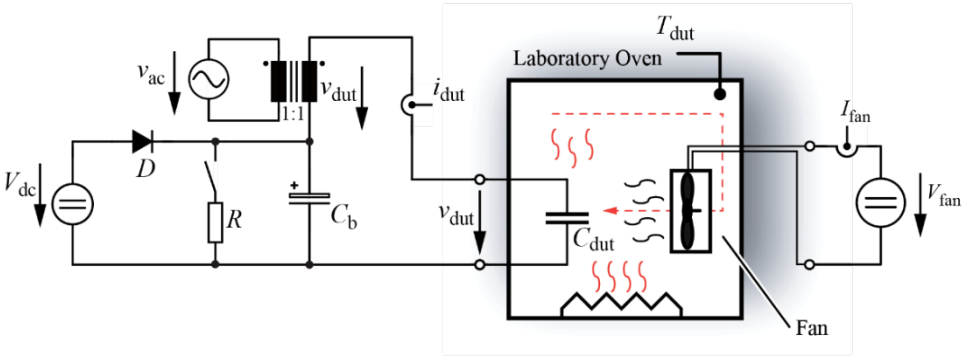
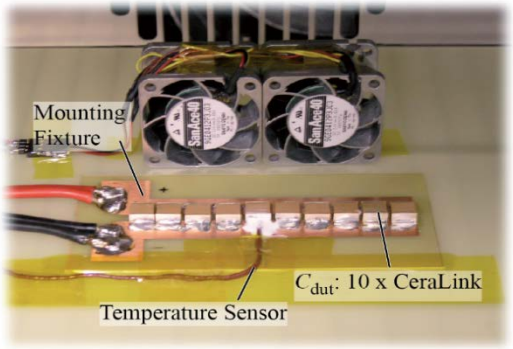




- Experimental Setup for Generation of DC Bias & Superimposed AC Voltage

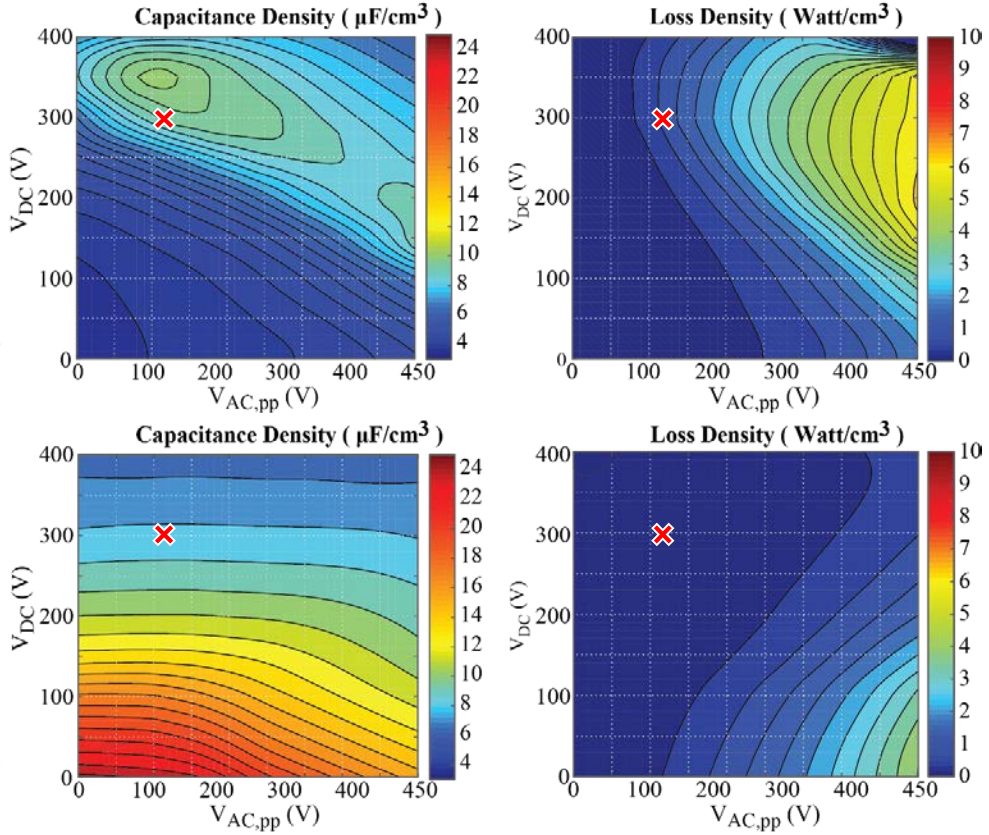
CeraLink vs. X6S

- Variation of DC Bias and Superimposed AC Voltage @ 60°C Operating Temp.

× Designed Op. Point

EPCOS/TDK CeraLink™ 2µF, 600V ▶

TDK Class II X6S MLCC 2.2µF, 450V ▶



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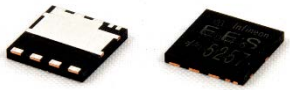
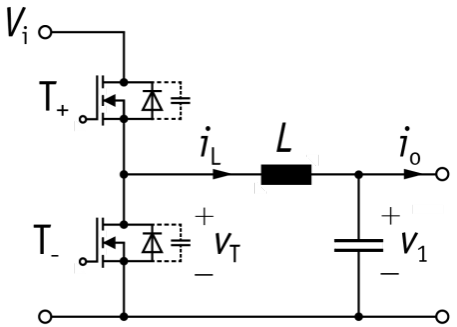
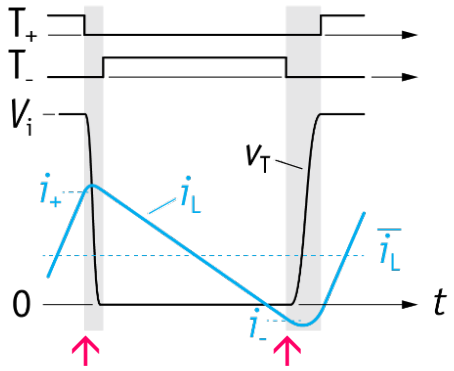
Measurement of
GaN ZVS & On-State Losses



Analysis of GaN Power Transistor ZVS Losses

- Little-Box 1.0 Experiments Indicated *Residual ZVS Losses of GaN Power Transistors*
- Losses Cannot be Explained by Remaining i_D, u_{DS} Overlap / Non-Ideal Gate Drive etc.





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- Accuracy only Guaranteed by Direct Loss Measurement → Calorimetric Approach

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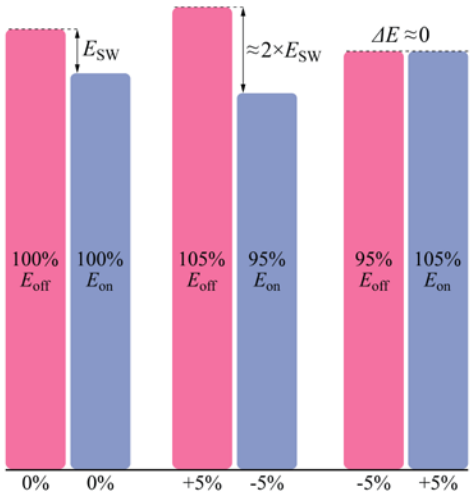

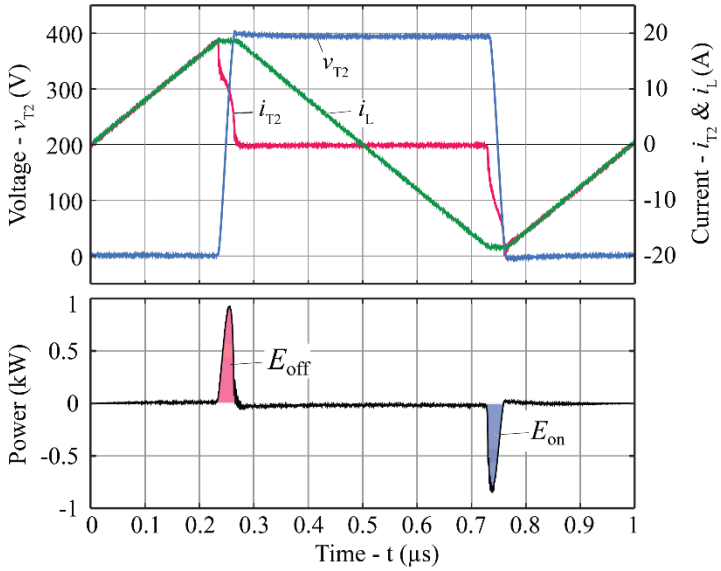

- Potentially Large Measurement Error for Electrical Double-Pulse Sw. Loss Measurement
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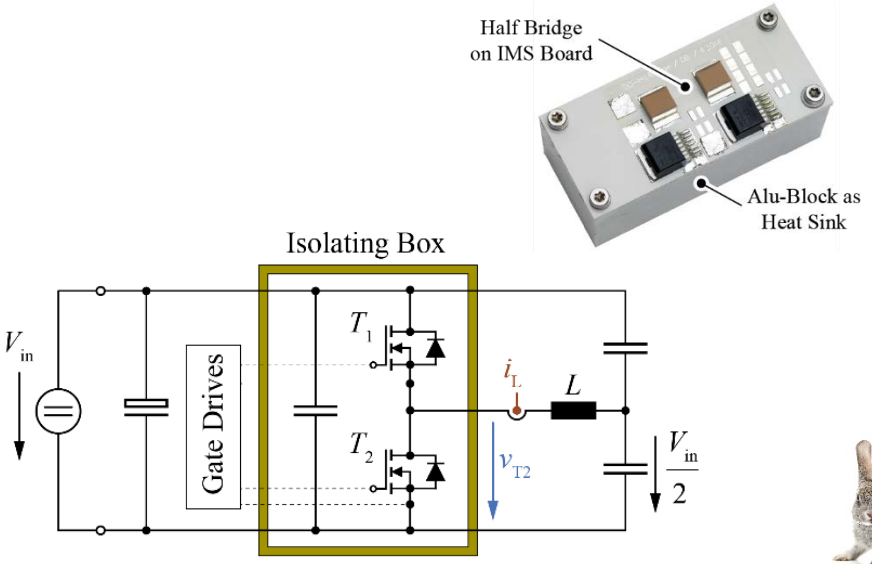
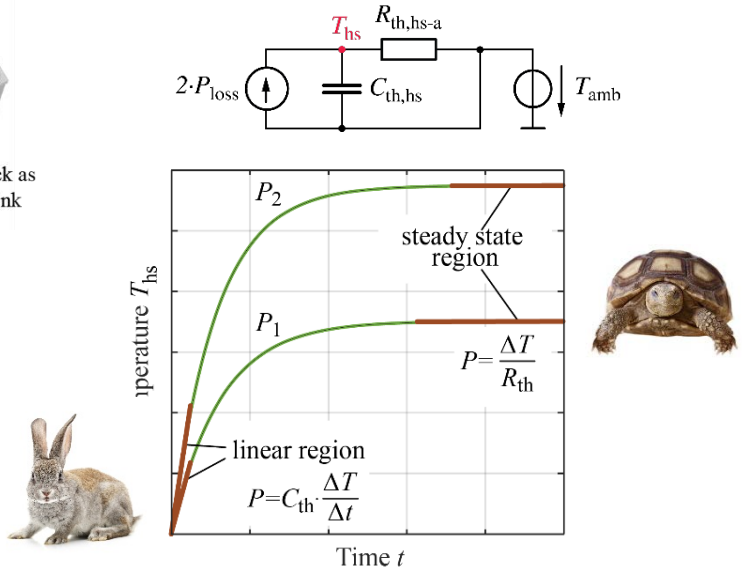
Calorimetric Measurement of ZVS Losses

- "Inductor in the Box" → Accurate DC Inp. & Outp. Power Measurement, Subtr. on Ind. Losses
- "Bridge Leg in the Box" → Direct Measurement of the Sum of Cond. & Sw. Losses





- "Bridge Leg in the Box" & Fast Measurement by $C_{th}.\Delta T/\Delta t$ Evaluation
- DC/DC Operation @ High Sw. Frequency for Large Ratio of Sw. and Conduction Losses
- Subtraction of the Cond. Losses from Datasheet or Dir. Measurement

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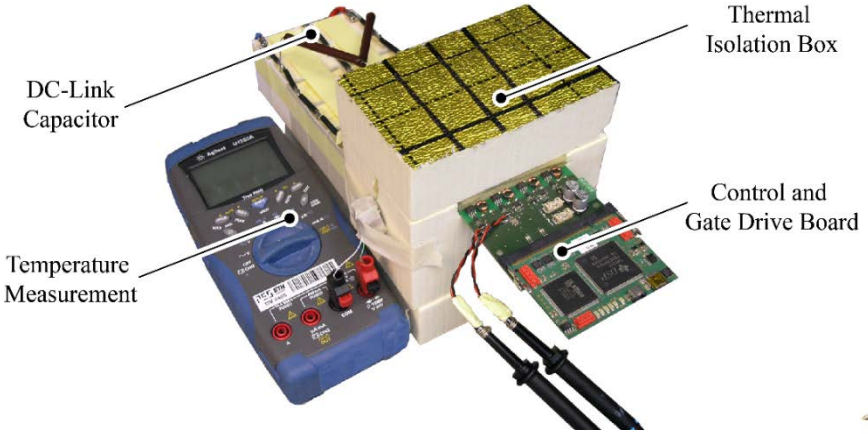
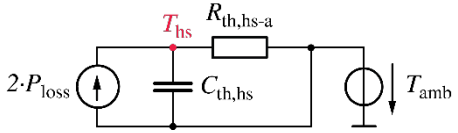
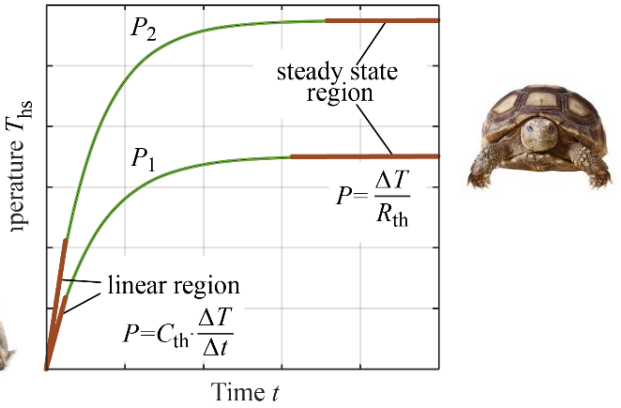




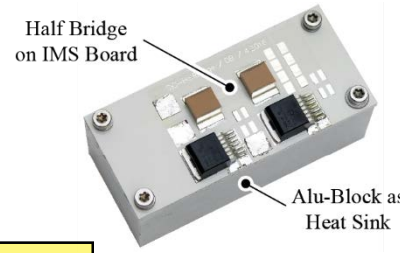


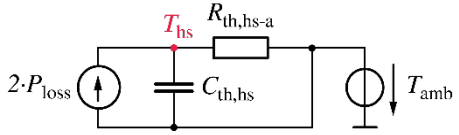
OPTOCON
OPTICAL SENSORS AND SYSTEMS

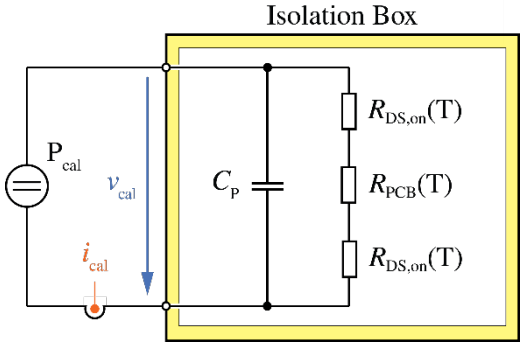
- Isolated Temp. Measurement with Optical Fiber (GaAs Crystal) Instead of Thermocouple
- Calibration by On-State of T_1 and T_2 & DC Current Operation / DC Power Loss Measurement

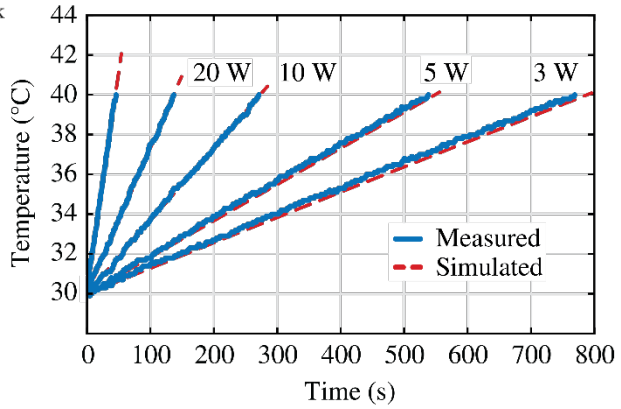
Calibration of "Bridge Leg in the Box" Setup

- Calibration by On-State of T_1 and T_2 & DC Current Operation / DC Power Loss Measurement
- Identification of Thermal Cap. C_{th} and Thermal Resistance R_{th}





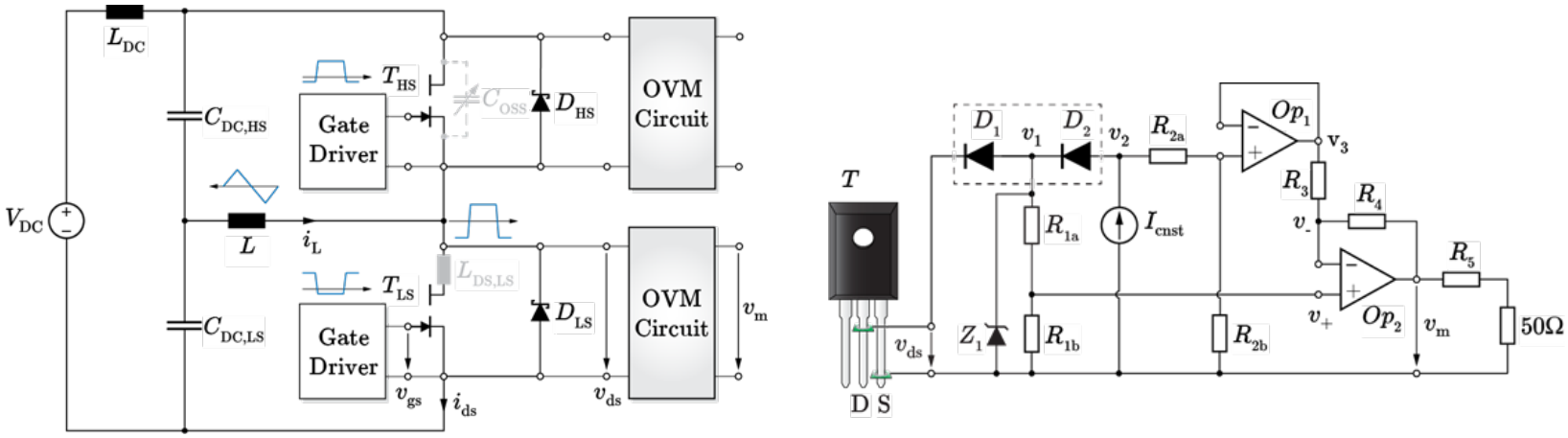




- DC Power Loss Measurement Ensures High Accuracy
- Thermal Behavior for Short Measurement Times Mainly Determined by C_{th}

Accurate On-State Voltage Measurement

- Clamping Diode for Limiting the On-State Voltage Measurement (OVM) to 2V
- Subtraction of the SiC Diode Forward Voltage Drop for High Accuracy (2mV)



- Only 50ns Blanking Time – OVM Circuit Can also be Used for Dynamic $R_{DS,on}$ Measurement

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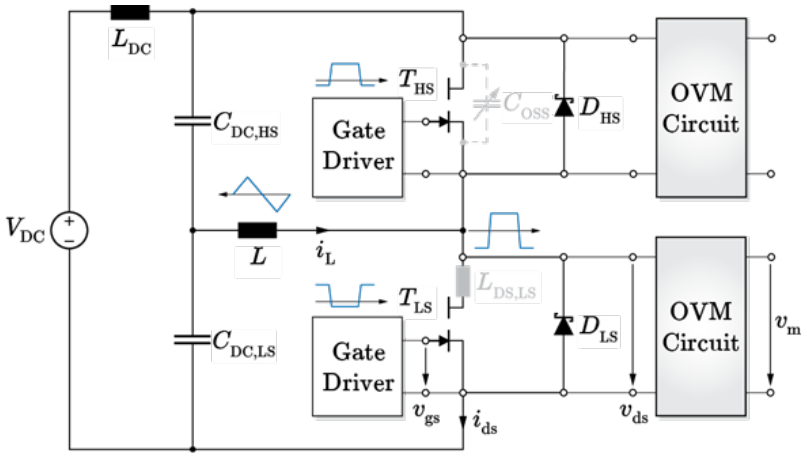
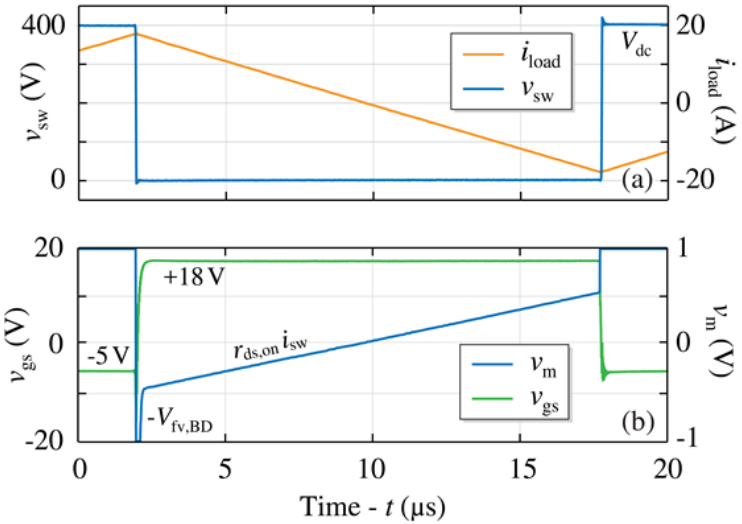
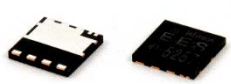


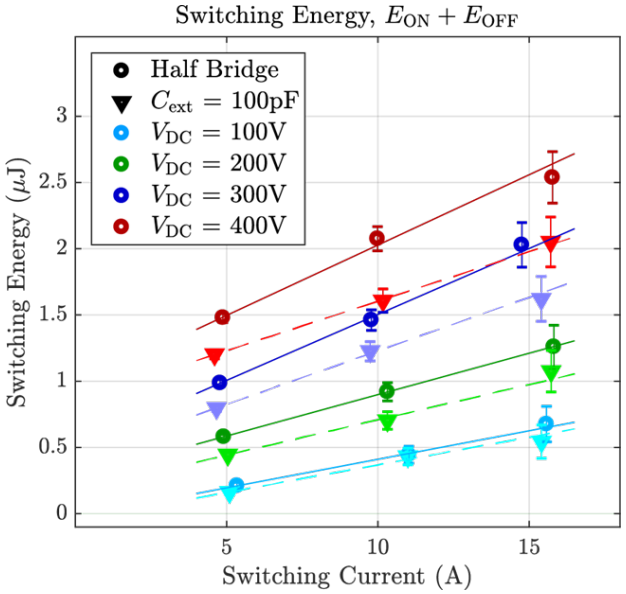


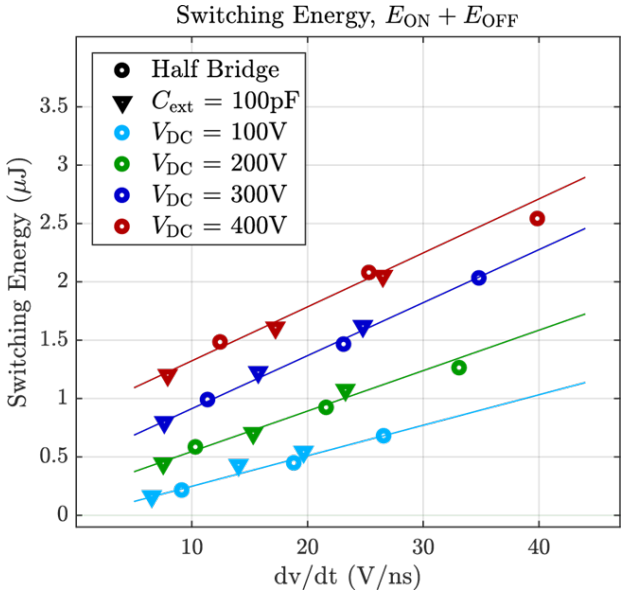
- Only 50ns Blanking Time – OVM Circuit Can also be Used for Dynamic $R_{DS,on}$ Measurement

ZVS Loss Measurement Results (1)

- Measurement of Energy Loss per Switch and Switching Period
- GaN Enhancement Mode Power Transistor (600V, 70mΩ@25°C)
- Antiparallel CREE SiC Schottky Freewheeling Diode (600V, 3.3A)



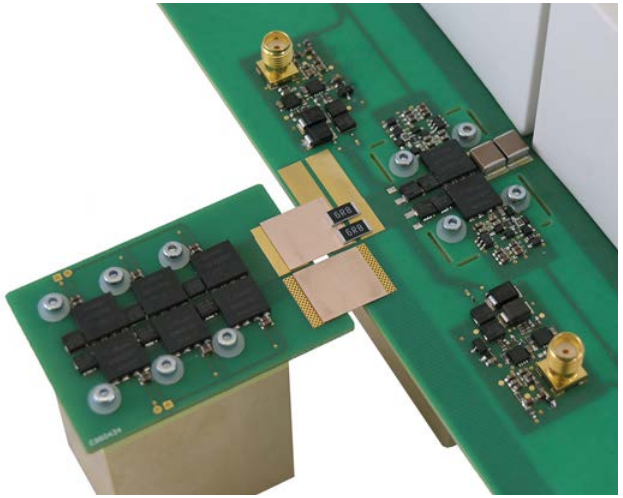


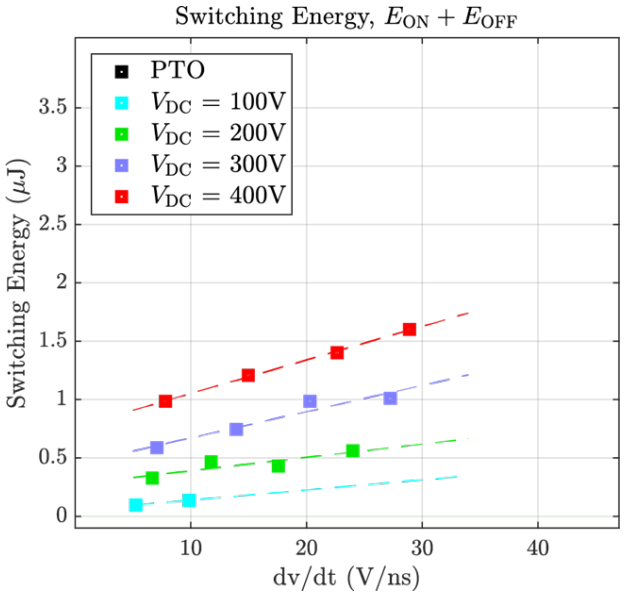


- Switching w/ and w/o 100pF Parallel Low-Loss SMD Multilayer Ceramic Chip Capacitor (450V)
- *dv/dt* Measured in 10%...90% of Turn-off Voltage, Behavior @ at Low *dv/dt* Still to be Clarified

ZVS Loss Measurement Results (2)

- Analysis of a *Permanently-Off Half-Bridge* Excited with Switch Node Voltage
- Measurement of Energy Loss per Switch and Switching Period





- Heating Indicates Losses in the Permanently-Off Devices
- Losses Comparable to the Losses of the Switching Half Bridge for Same d*v*/d*t*

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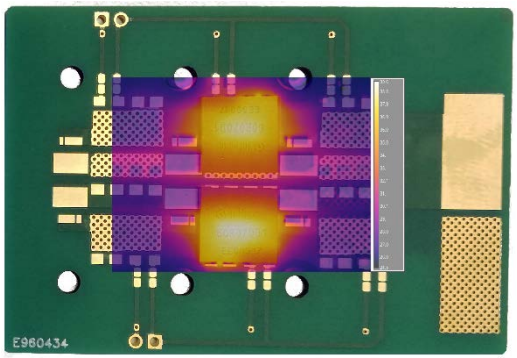

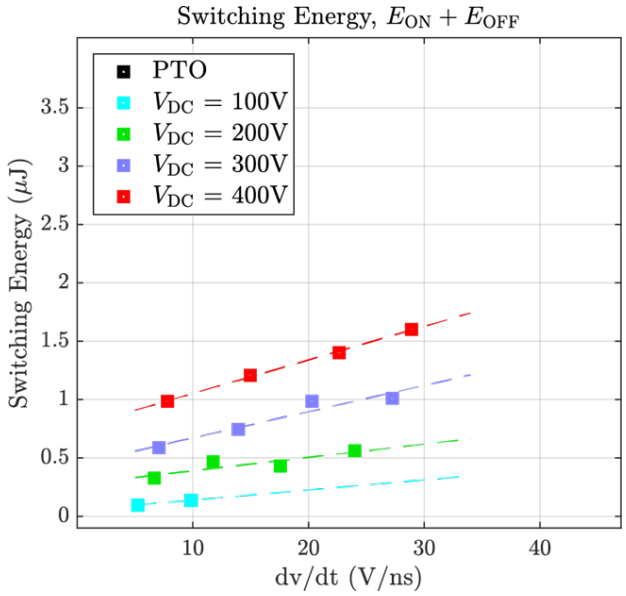

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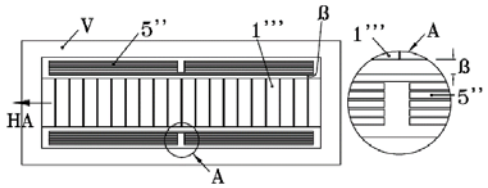
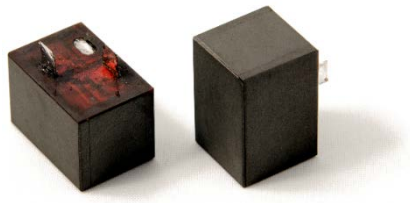
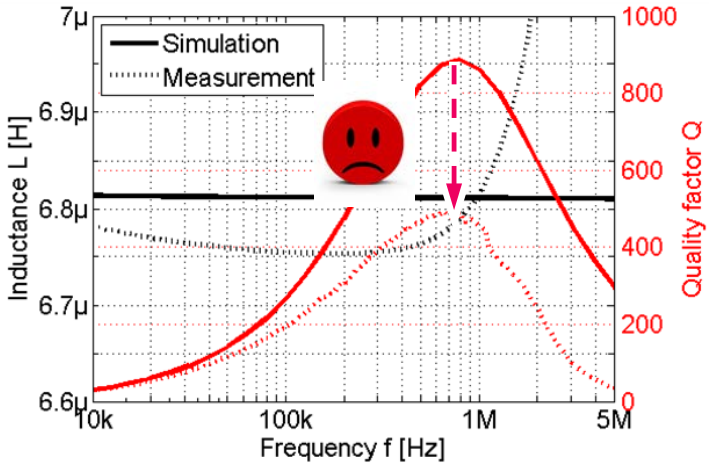
Measurement of Ferrite Multi-Airgap Core "Mystery" Losses

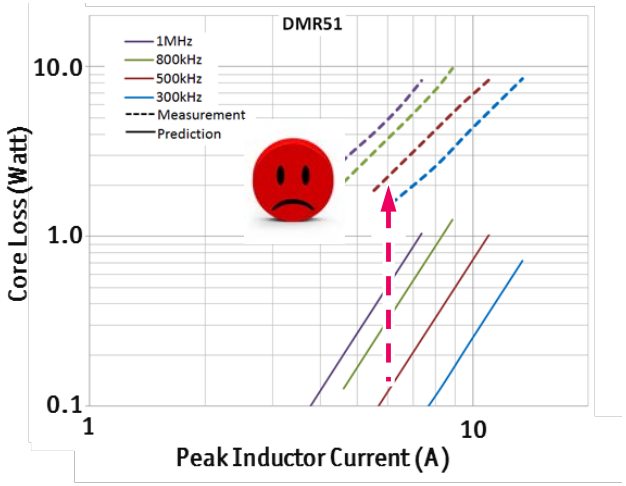


Multi-Airgap Inductor

- Ferrite E-Core with *50 x 0.3mm Thick Stacked Plates* as Center Post
- Power Loss of TCM Inductors Sign. Higher than Expected

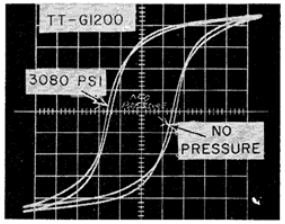




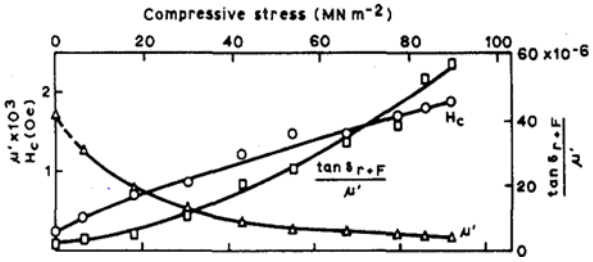


- Analysis by Fraunhofer IZM Shows *Up to Factor 10 High Core Losses (!)* → "Mystery" Losses

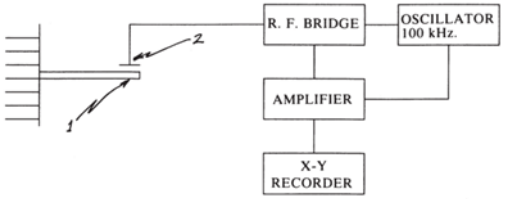
– Machining Increases Core Losses



- 1964 - E. Stern & D. Temme → Machining / Compressive Stress Changes BH-Loop of NiZn Ferrite



- 1974 - J. Knowles, E. Snelling → Compressive Stress Incr. Loss Fact., Reduces μ,



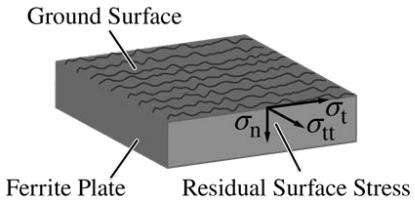
- 1984 - E. Klokholm & H. Wolfe → 40 μm Magn. Dead Surface Layer of MnZn Ferrite

- 1987 - S. Chandrasekar et al. → Lapping Causes Greater Residual Stress than Grinding

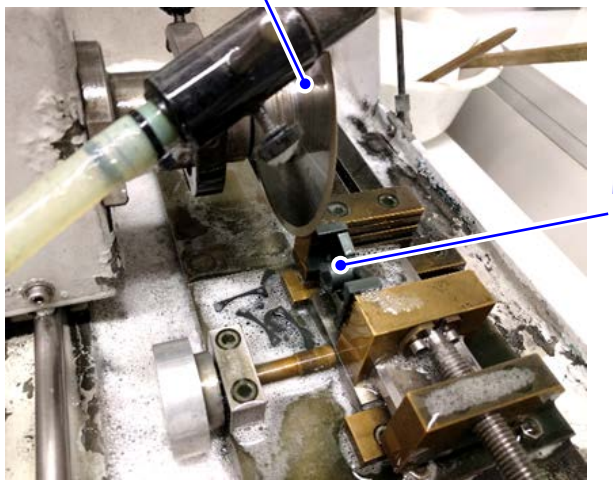
Ferrite Machining Process

laboratory for nanometallurgy

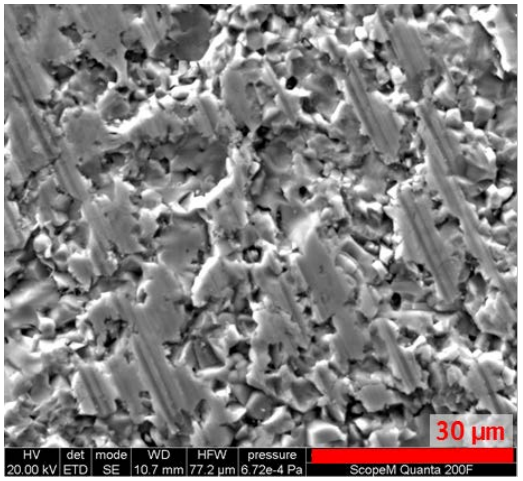
- Cutting of Thin Plates from Ferrite Rod with Diamond Saw
- Abrasive Machining Introduces Mech. Stress into Surface



Diamond Blade
5000rpm



Machined
Core



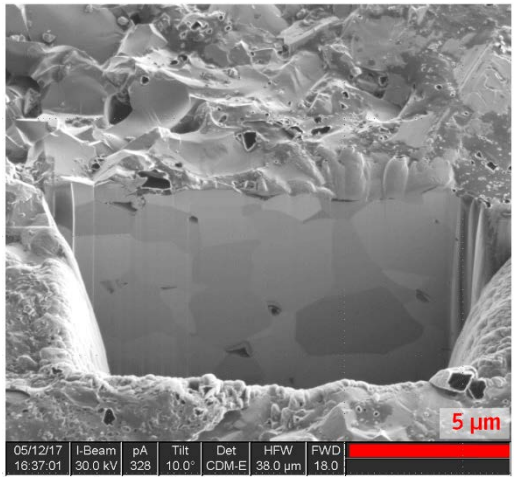
SEM Image of
Machined MnZn
Ferrite (3F4)

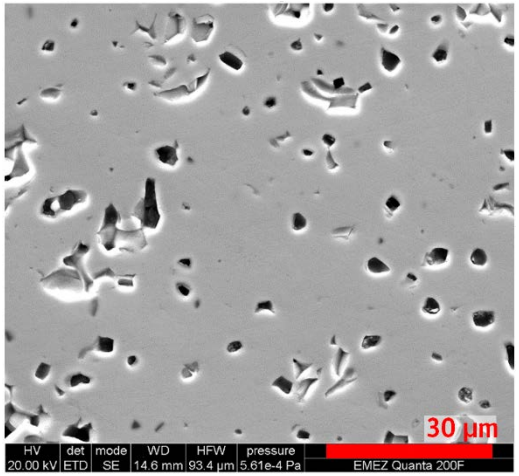
- Ferrite Properties in Surface Altered → Increase of Loss Factor

Subsurface Condition of Machined Ferrite

Empa
Materials Science and Technology

- Focused Ion Beam (FIB) Cut into Ferrite (3F4) Sample & Scanning Electron Microscopy (SEM)
- Polishing of Surface with Grain Sizes 2400 SiC → 4000 SiC → Colloidal Silica SiO_2

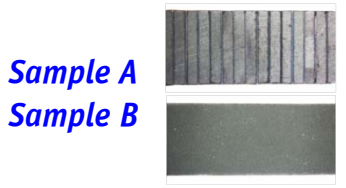


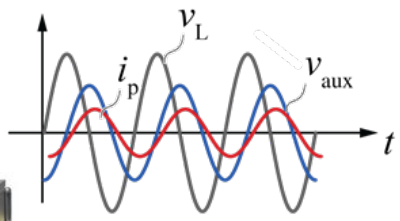


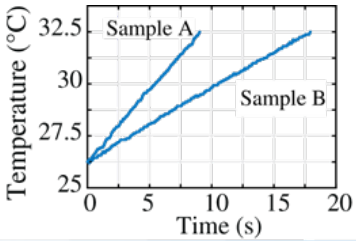
- Polishing Removes 500µm of Surface → Bulk Material Exposed
- Bulk Ferrite also Exhibits Cavities → Result of (Imperfect) Sintering Process

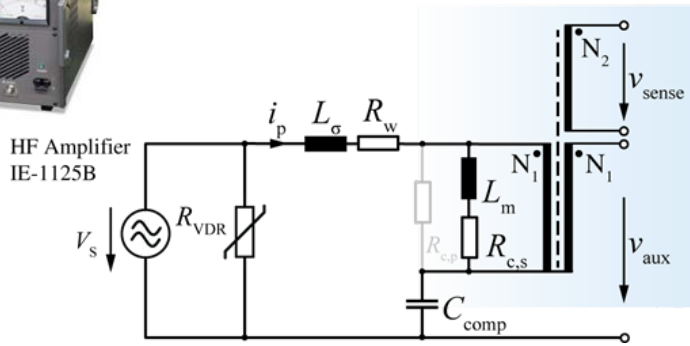
Thermometric Surface Loss Measurement

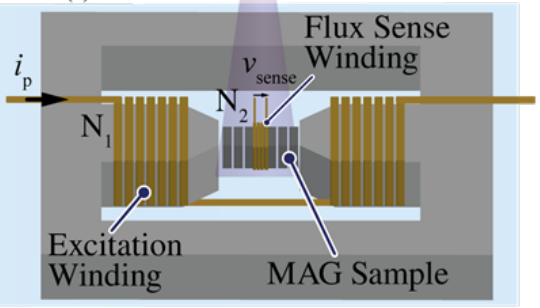
- Impression of Homogeneous Sin. Flux Density of Desired Ampl. / Frequ.
- Cap. Series Comp. for Lowering Impedance @ High Frequencies
- Measurement of *Transient* Temp. Change → Calcul. of Losses







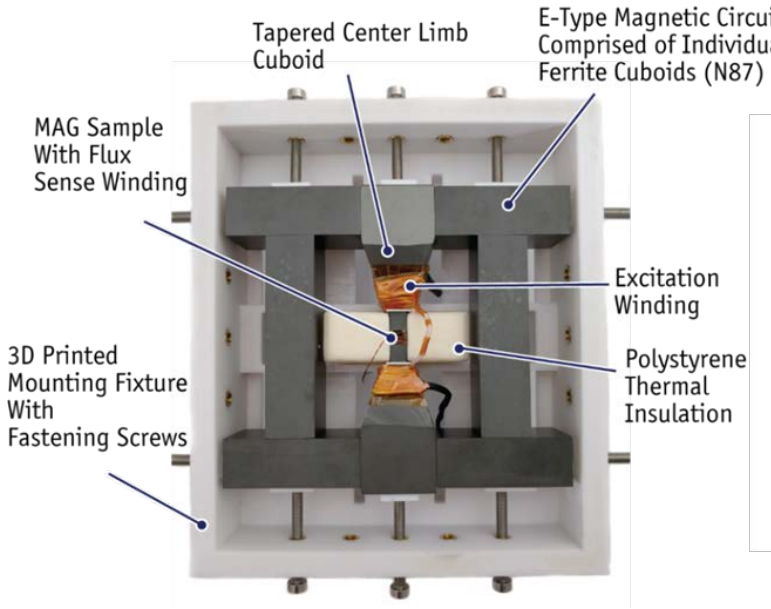


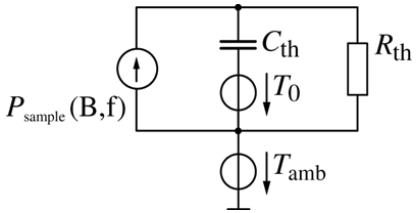


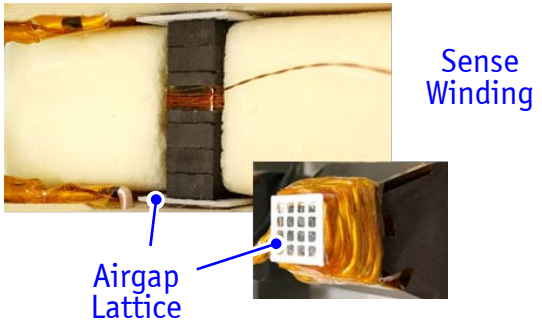
- Temperature Rise of ΔT= 1.5°...5°C Sufficient (Accuracy ±0.2°C), Fast Measurement (!)

Test Fixture / Magnetic Circuit

- E-Type Fixture for Swift Installation of Diff. Samples (7mm x 6.4mm x 21.6mm)
- FEM Optimiz. of Dimensions – Large Core Cross Section / Tapered Outer Limbs



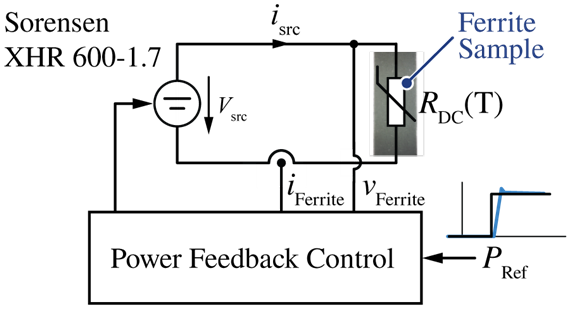


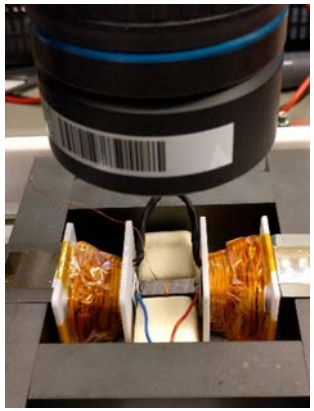


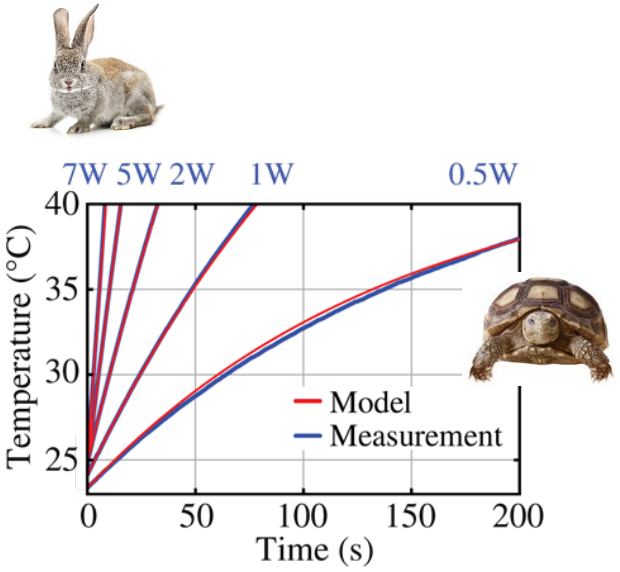
- Therm. Insul. & Airgap Lattice Ensure Low Heat Flux to Ambient
- Measurement of Temp. Increase Over Time Allows to Verify Homog. Flux Density in Sample

Identification of Therm. Parameters R_{th}, C_{th}

- DC Current Impressed in Ferrite, Voltage Control for Const. Power Dissipation as R_{DC}=R_{DC}(Temp.)
- Temperature Response of Sample Recorded (*FLIR A655sc W* with Close-Up Lens)
- Emissivity of Ferrite Determined Using Heat Plate (ε= 0.86)





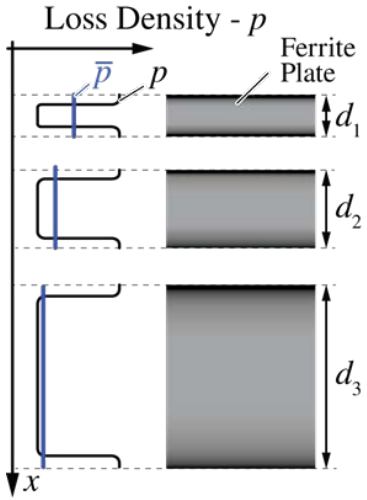


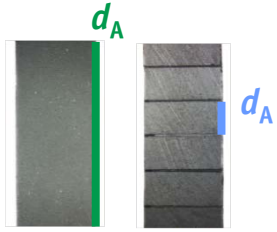
- R_{th} = 37.8 K/W Can be Neglected
- Obtained Parameter C_{th}=3.83J/K Close to C_{th} Calc. Based on Vendor Data (C_{th} = 3.6J/K)

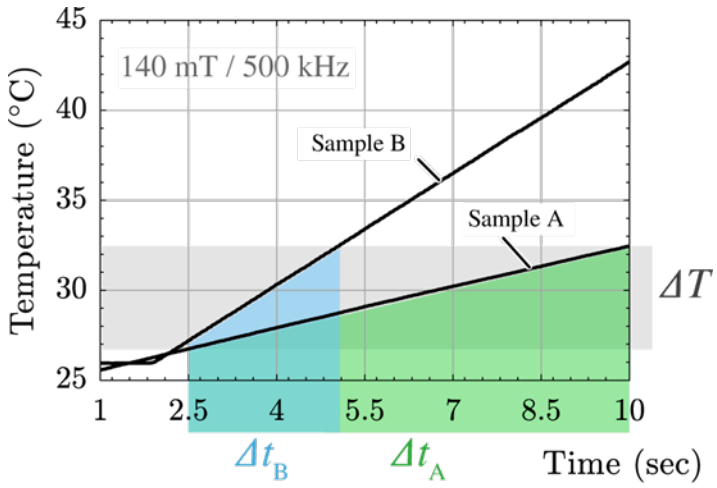
Surface Loss Measurement Principle

FERROXCUBE

- Hypothesis: Core Loss Density in Surface Layer Higher than in Bulk
- Thinner Plates → Higher Average Losses / Faster Temp. Rise
- Stacking of Plates Does NOT Affect Temperature Rise (!)



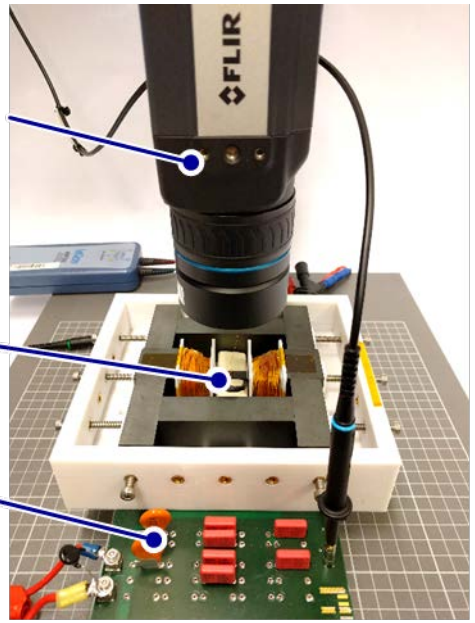




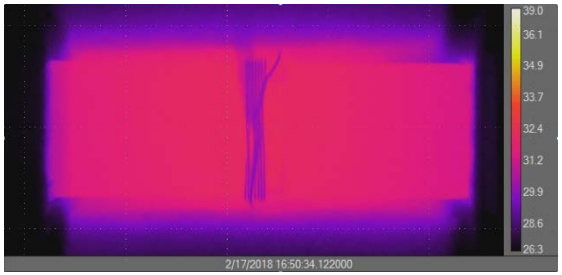
- Surface Loss Density Can be Directly Calc. from Mat. Parameters / Geometry & Δt_A and Δt_B

Temperature Rise Recording

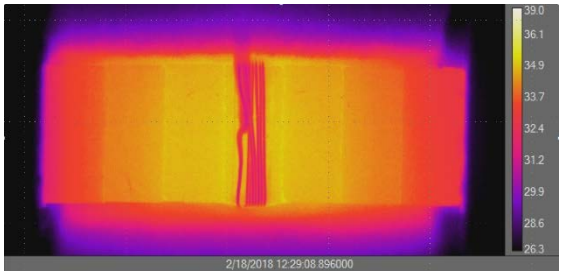
- Comparison of Solid 3F4 Sample (1 x 21.6mm) and Stacked Plates Sample (7 x 3mm)
- Sinusoidal Excitation *100mT / 400kHz*



3F4 Solid Sample / 21.6mm



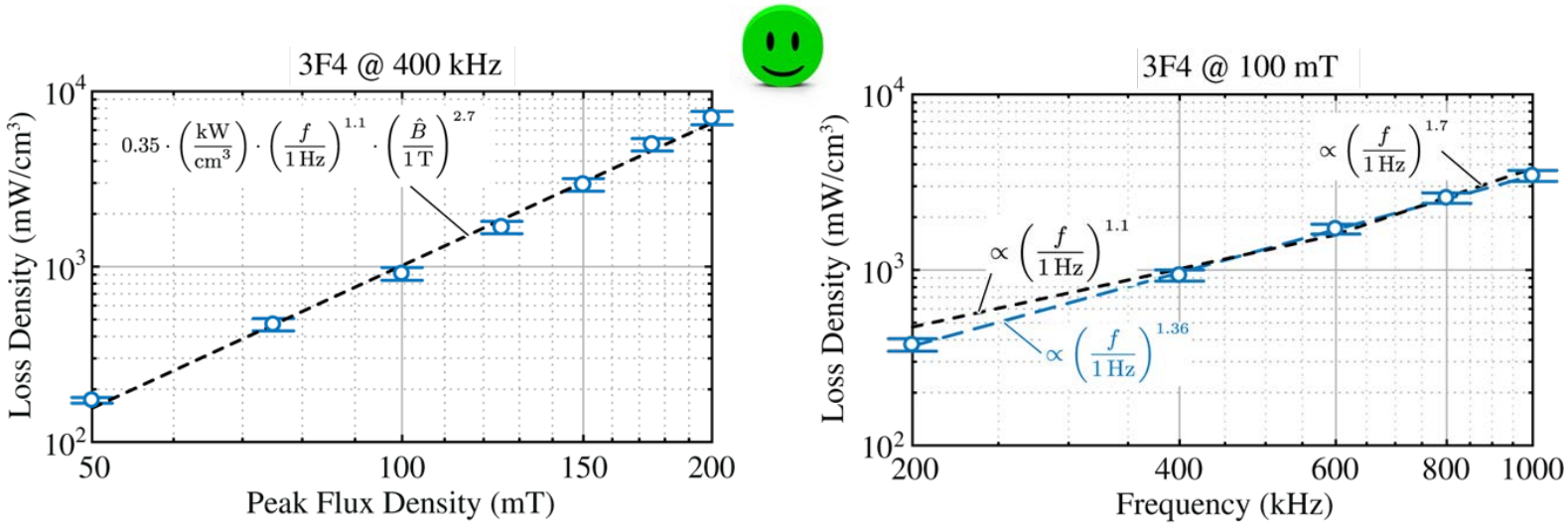
7 Plates 3F4 / 3mm



- Thermal Image shown *25 Seconds After Turn-On* of Magnetic Excitation

Measurement Results – *Bulk Losses*

- Comparison of Measurement Results and Datasheet Values, 3F4 @ 25°C
- Measurement Error Approx. ±10% (Worst Case)

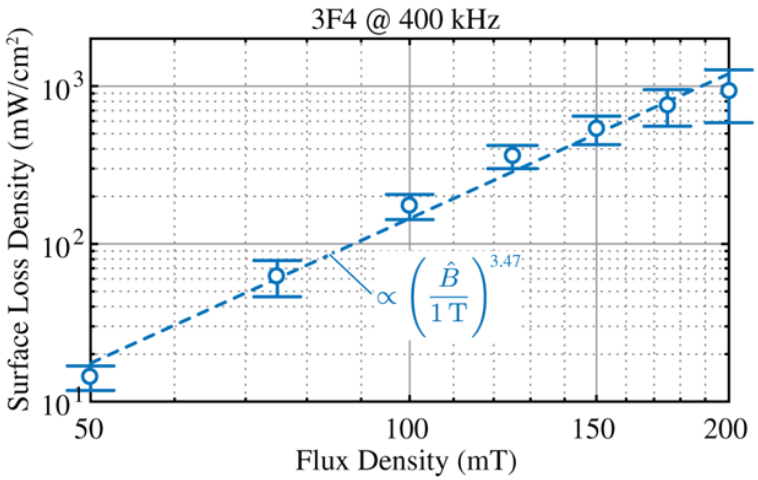


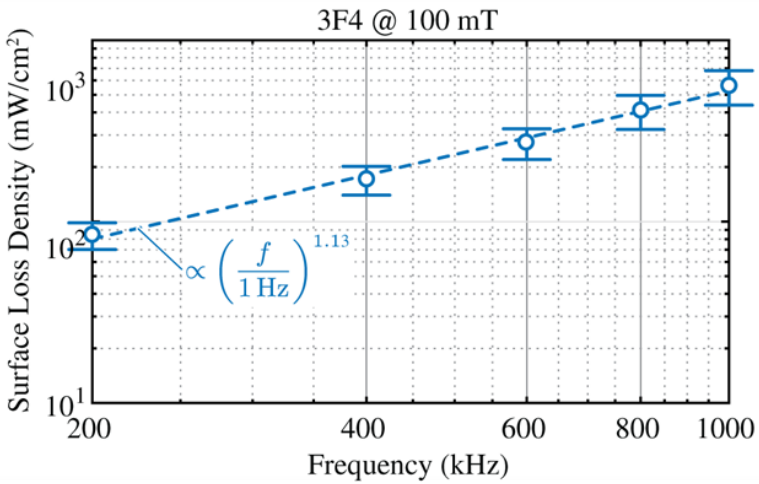
- Good Agreement with Datasheet Values / Vendor Steinmetz Parameters

Measurement Results – *Surface* Losses

- Measurement Error Approx. ±25% (Worst Case)
- Error Determined by Meas. Time & Temp. Reading Accuracy

$$p_{Surf} = 0.0615 \times \left(\frac{f}{1\text{Hz}}\right)^{1.13} \times \left(\frac{\hat{B}}{1\text{T}}\right)^{3.47} \left(\frac{\text{mW}}{\text{cm}^2}\right)$$

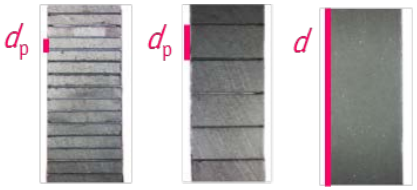




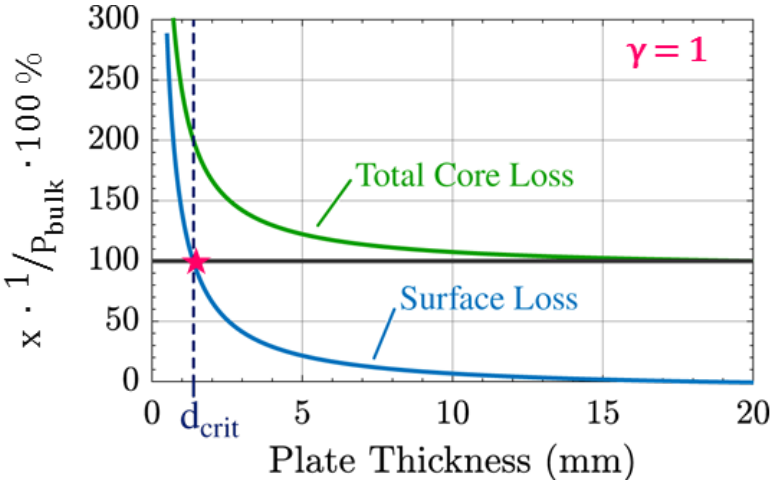
- Comp. of Steinmetz Parameters of Surface Losses & Bulk Losses BS > B, aS < a

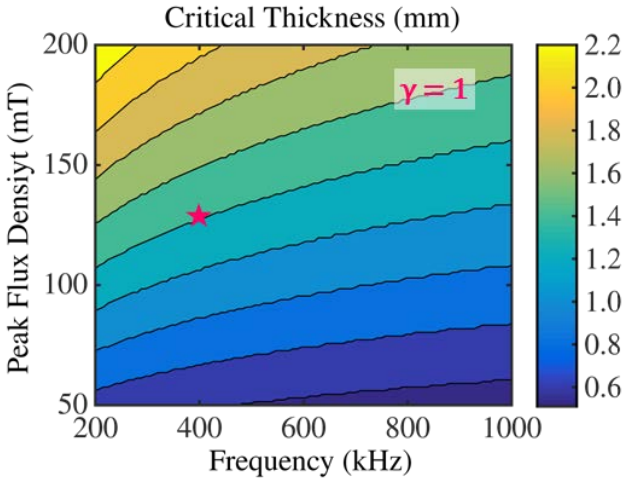
"Critical Thickness" of Ferrite Plates

- "Critical Thickness" Reached for Equal Losses in Bulk & Surface
- Critical Plate Thickness is INDEPENDENT of Cross Section (!)



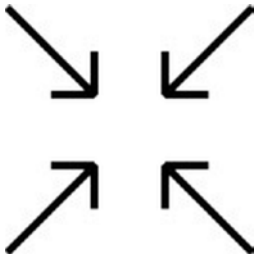
3F4 Critical Thickness
for 125mT / 400kHz





- Dependence on Flux Density Ampl. & Frequency !
- Dependence on Material / Machining Process / Power Processing Treatment

Little Box 2.0

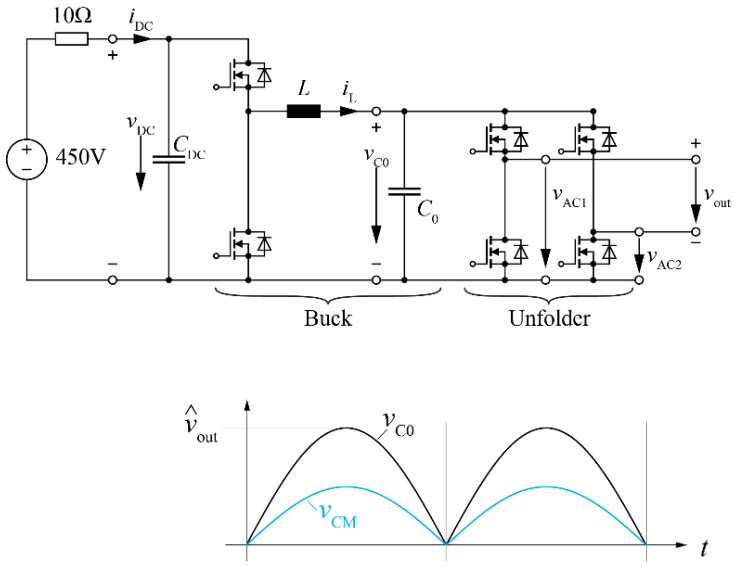


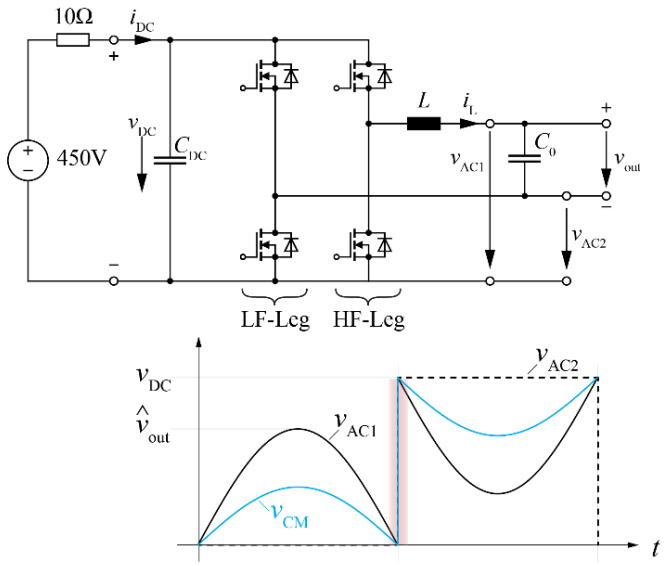
240 W/in³

DC/ | AC | Converter + Unfolder
PWM vs. TCM Optimization
ηρ-Pareto Limits
Hardware Prototype
Experimental Results

Little Box 2.0 – New Converter Topology (1)

- Alternative Converter Topology → Only Single HF Bridge Leg + 60Hz-Unfolder
- DC/ | AC | - Buck Converter + Full-Bridge Unfolder OR HF Half-Bridge & Half-Bridge Unfolder



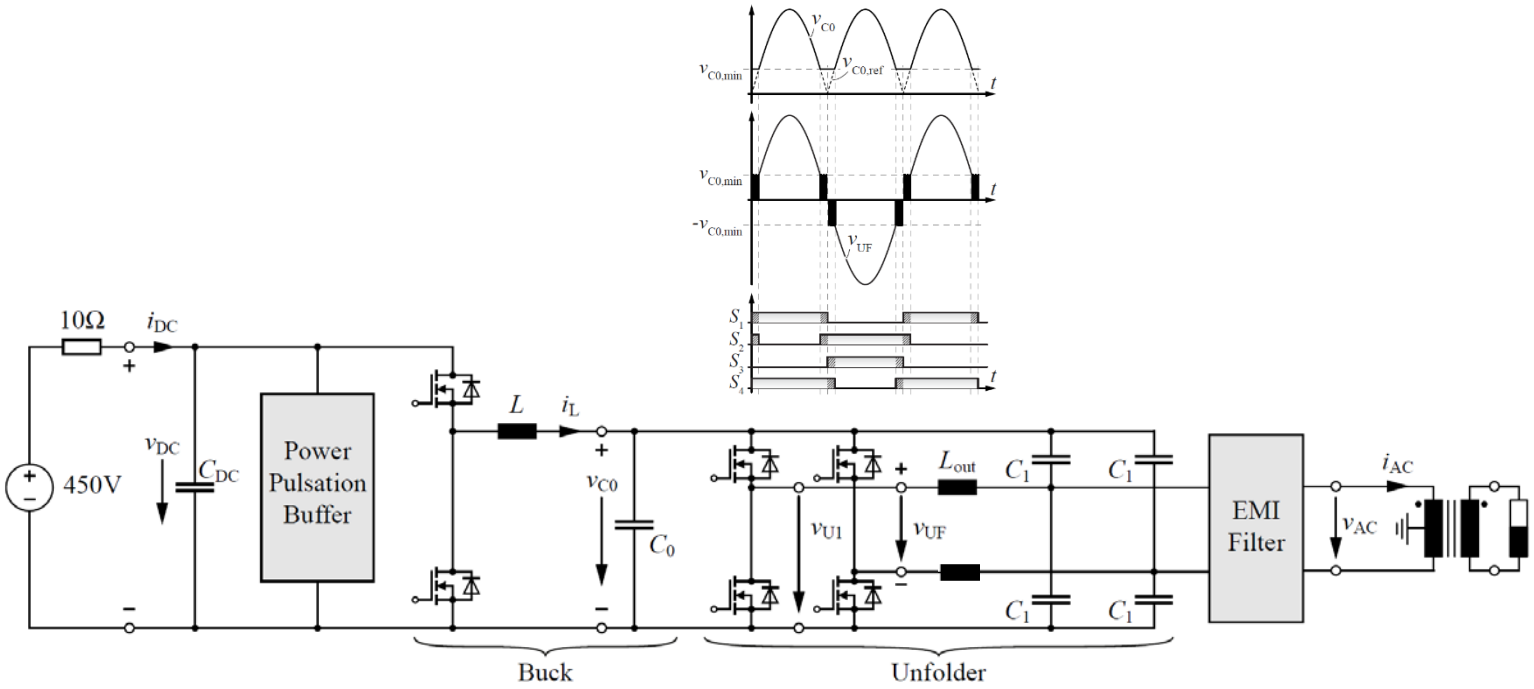


- v_{C0} Easy to Generate/Control
- Higher Conduction Losses Due to FB-Unfolder
- Lower CM-Noise (DC & n x 120Hz-Comp.)
- C_{CM}=700nF Allowed for 50mA Gnd Current

- v_{AC1} More Difficult to Generate/Control
- Lower Conduction Losses
- Higher CM-Noise (DC and n x 120Hz-Comp.)
- C_{CM}=150nF Allowed for 50mA Gnd Current

Little Box 2.0 – New Converter Topology (2)

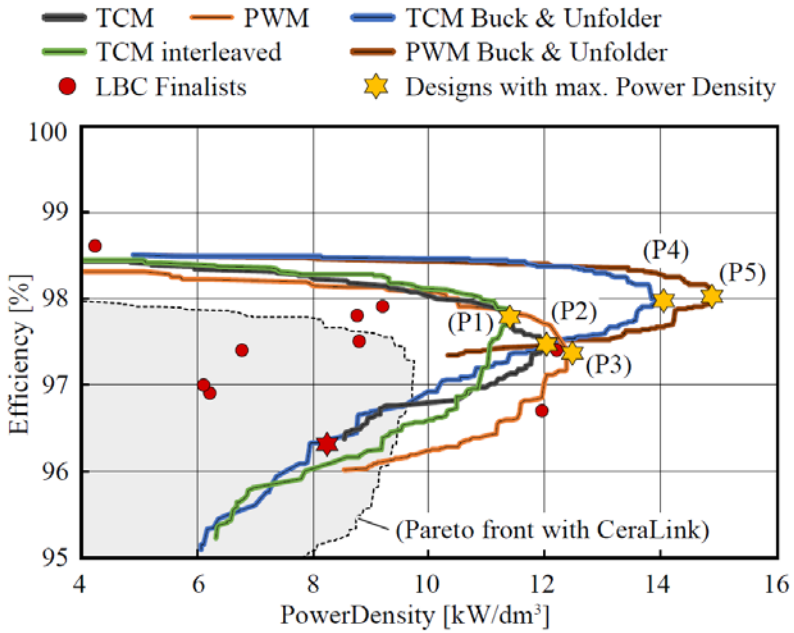
- Alternative Converter Topology - DC/ | AC | - Buck Converter + Unfolder
- 60Hz-Unfolder (Temporary PWM for Ensuring Continuous Current Control)
- TCM or PWM of DC/ | AC | - Buck-Converter

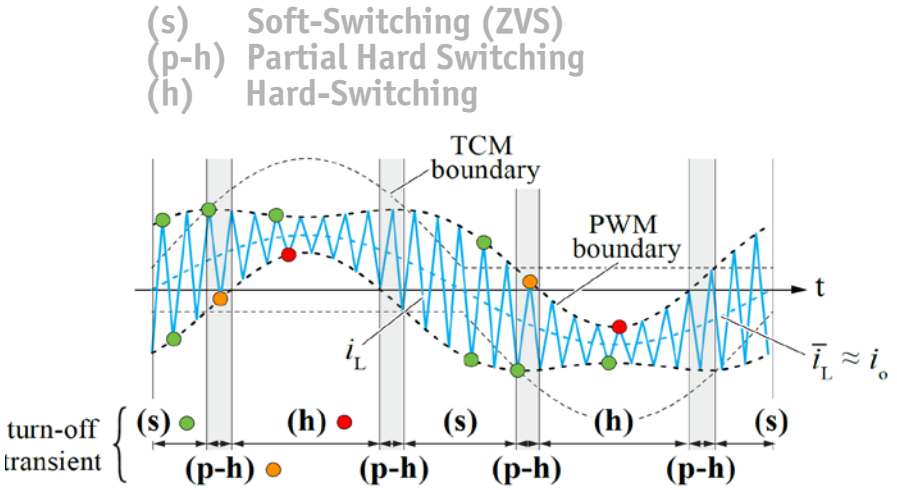


- **Full Optimization** of All Converter Options for **Real Switches** / X6S Power Pulsation Buffer

Little Box 2.0 – Multi-Objective Optimization

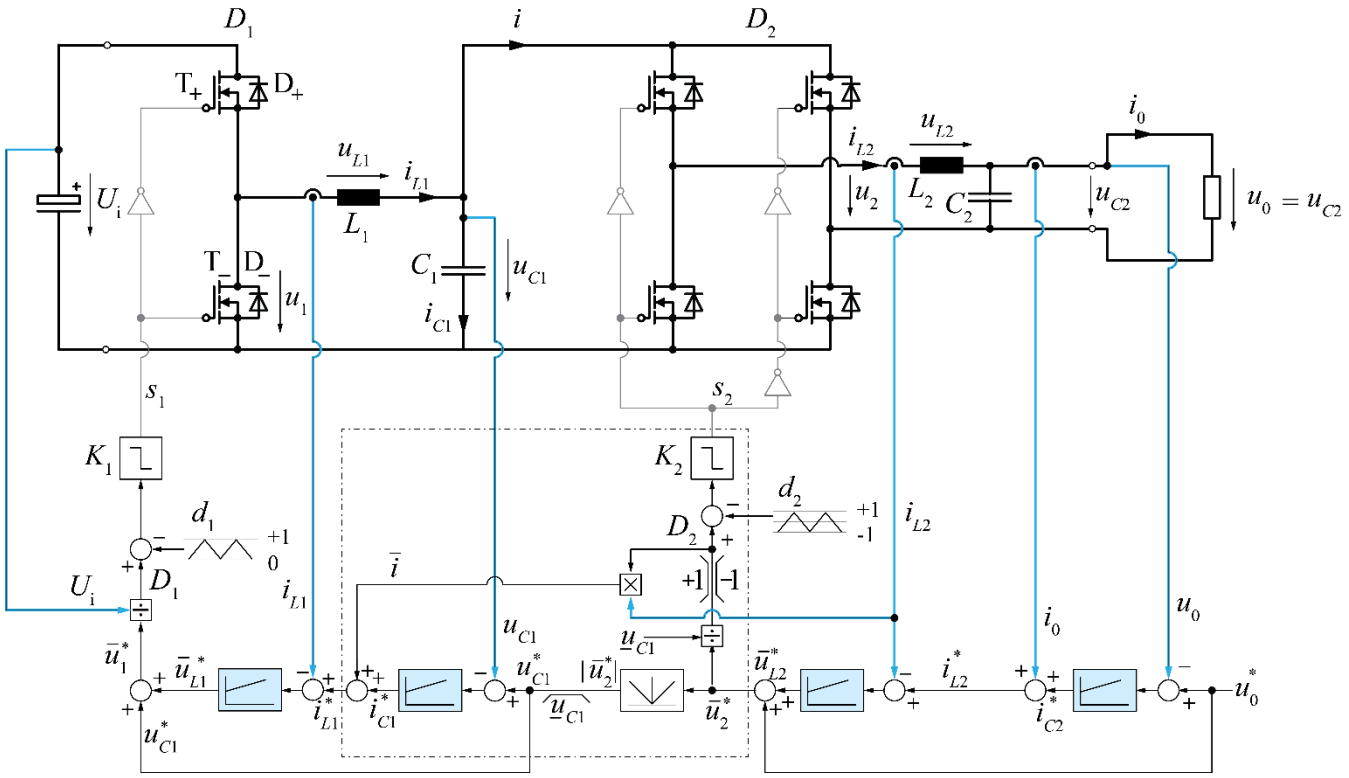
- DC/ | AC | - Buck Converter (Single Bridge Leg) + Unfolder & PWM Shows Best Performance
- Full-Bridge Would Employ 2 Switching Bridge Legs - Larger Volume & Losses
- Interleaving Not Advantageous – Lower Heatsink Vol. but Larger Total Vol. of Switches and Inductors





- ρ= 250W/in³ (15kW/dm³) @ η= 98% Efficiency Achievable for Full Optimization

Little Box 2.0 – Control Structure

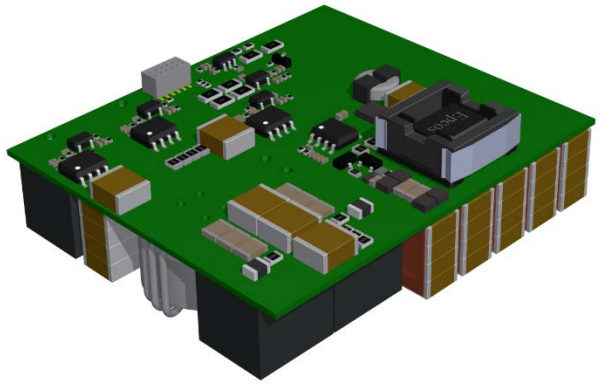


- Each Stage (Buck & Unfolder) Controlled with Cascaded Current and Voltage Loop
- Without Switching of Unfolder Control Like for Conventional Boost PFC Rectifier

3D-CAD Construction of the Final System

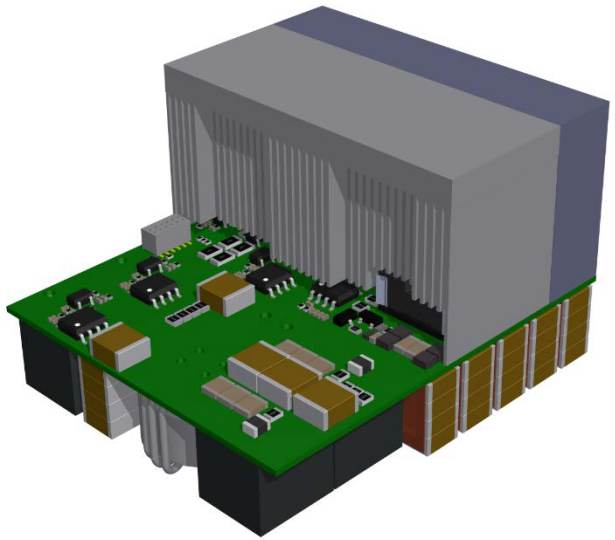
240 W/in³

Little Box 2.0 – Final Mechanical Construction (1)



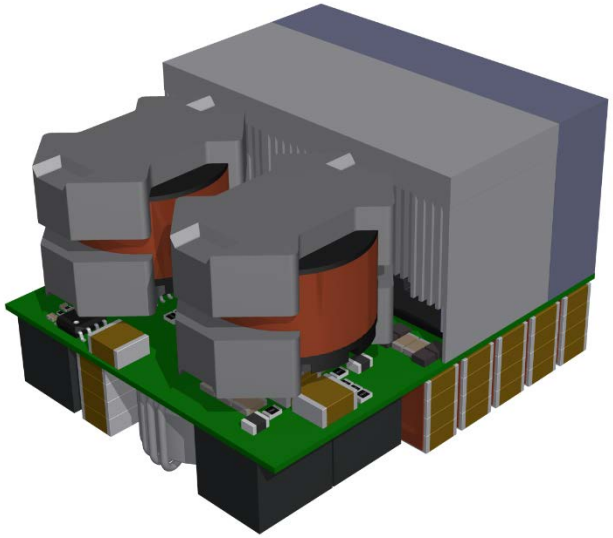
- 60 mm x 50 mm x 45 mm = 135 cm^3 (8.2in^3) → 14.8 kW/dm^3 (243 W/in^3)

Little Box 2.0 – Final Mechanical Construction (2)



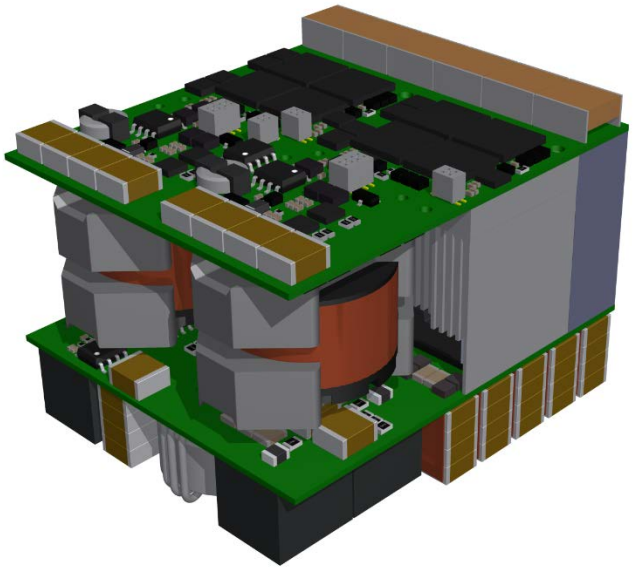
- 60 mm x 50 mm x 45 mm = 135 cm^3 (8.2in^3) → 14.8 kW/dm^3 (243 W/in^3)

Little Box 2.0 – Final Mechanical Construction (3)



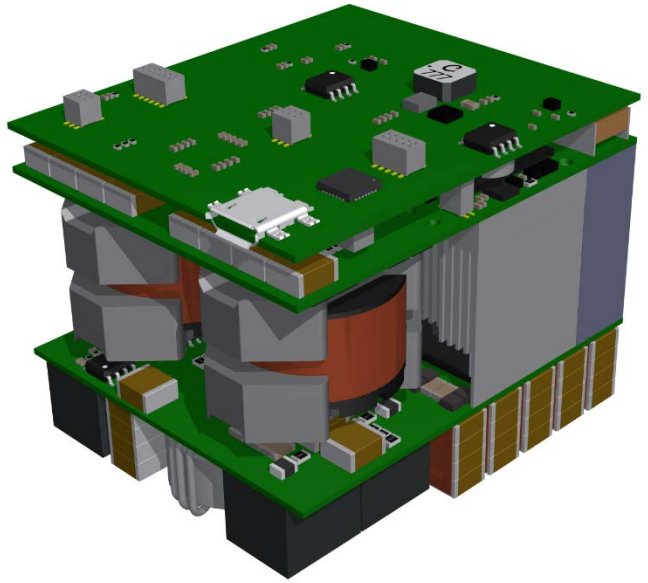
- 60 mm x 50 mm x 45 mm = 135 cm^3 (8.2in^3) → 14.8 kW/dm^3 (243 W/in^3)

Little Box 2.0 – Final Mechanical Construction (4)



- 60 mm x 50 mm x 45 mm = 135 cm^3 (8.2in^3) → 14.8 kW/dm^3 (243 W/in^3)

Little Box 2.0 – Final Mechanical Construction (5)



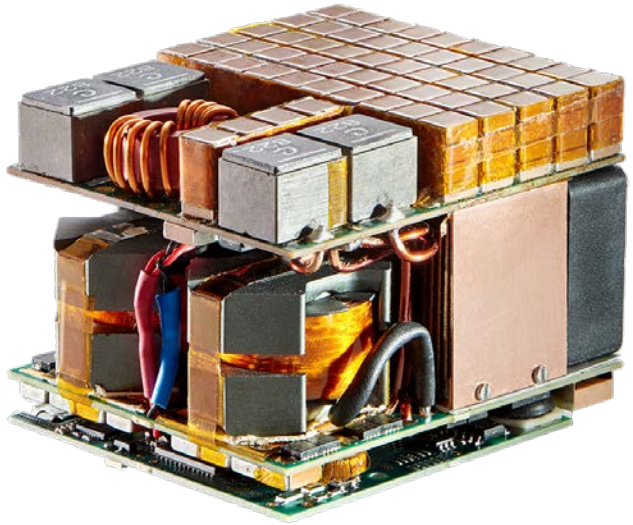
- 60 mm x 50 mm x 45 mm = 135 cm^3 (8.2in^3) → 14.8 kW/dm^3 (243 W/in^3)

Experimental Results

Hardware Prototype
Output Voltage/Input Current Quality
Steady-State / Step-Response Waveforms →
Efficiency
EMI Measurements
Operating Temperature

Little Box 2.0 -- Demonstrator

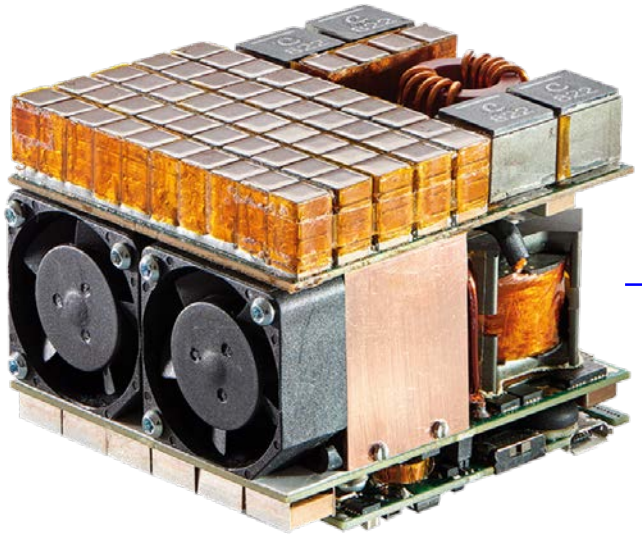
★ 240 W/in³



- 60 mm x 50 mm x 45 mm = 135 cm³ (8.2in³) → 14.8 kW/dm³ (243 W/in³)

Little Box 2.0 -- Demonstrator

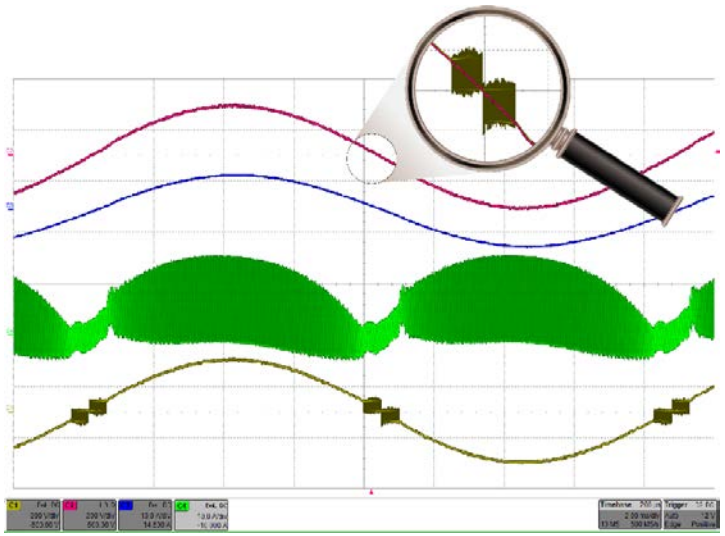
★ 240 W/in³

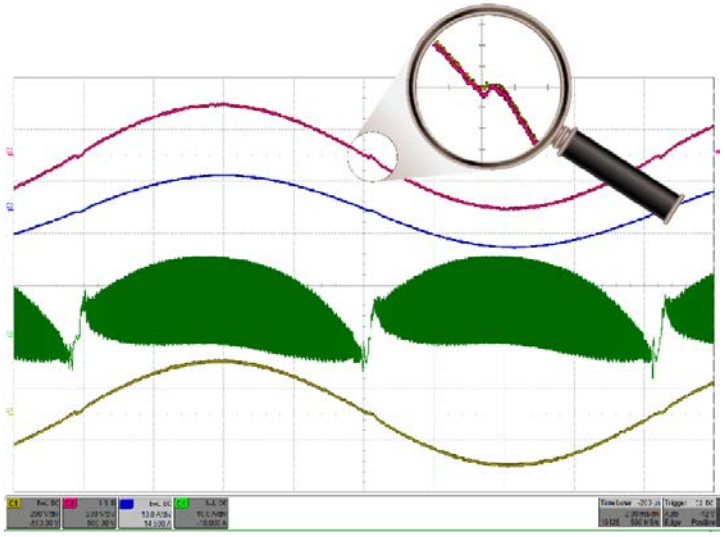


- 60 mm x 50 mm x 45 mm = 135 cm³ (8.2in³) → 14.8 kW/dm³ (243 W/in³)

Analysis of DC/|AC|-Buck Converter & Unfolder

- Voltage Zero Crossing Behavior With (Right) & Without (Left) Switching of Unfolder



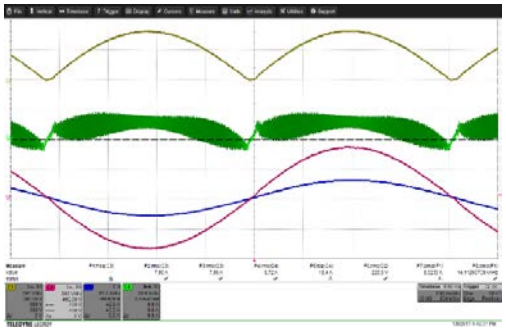


Output Voltage (200V/div)
Output Current (10A/div)
Buck Inductor Current (10A/div)
Unfolder Output Voltage (200V/div)

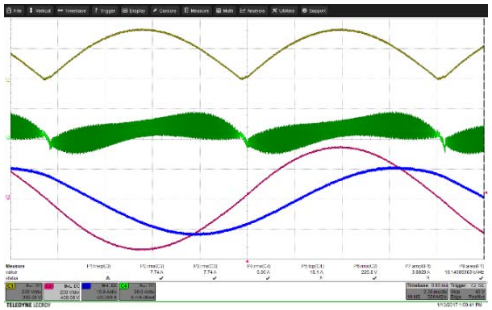
- Output Voltage & Current Fully Controlled Around Voltage Zero Crossings
- Slope of Buck Conv. Outp. Curr. can be Decreased – Adv. for React. Loads (No Step-Change of DC Curr.)

Little Box 2.0 – Measured Waveforms (1)

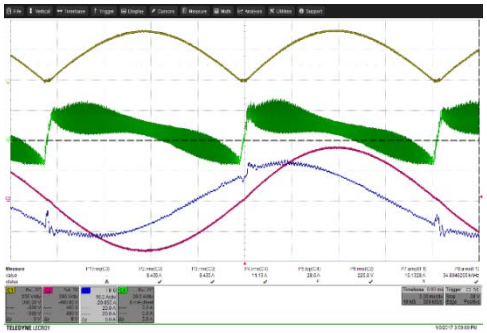
- DC/|AC| Buck-Stage Output Voltage & Inductor Current



■ Resistive Load



■ Inductive Load

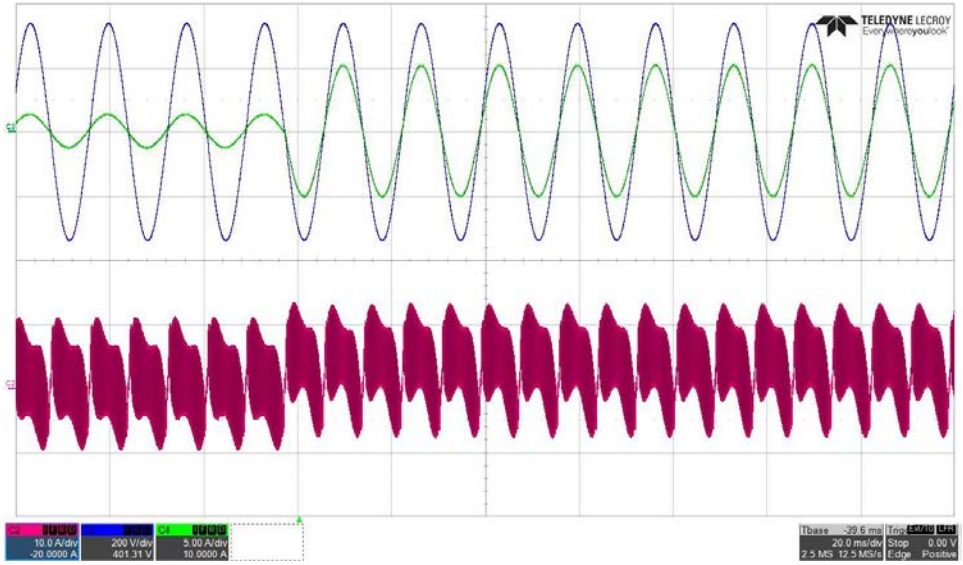


■ Capacitive Load

Little Box 2.0 – Measured Waveforms (2)

- Step-Response Waveforms for 600 W Load Step

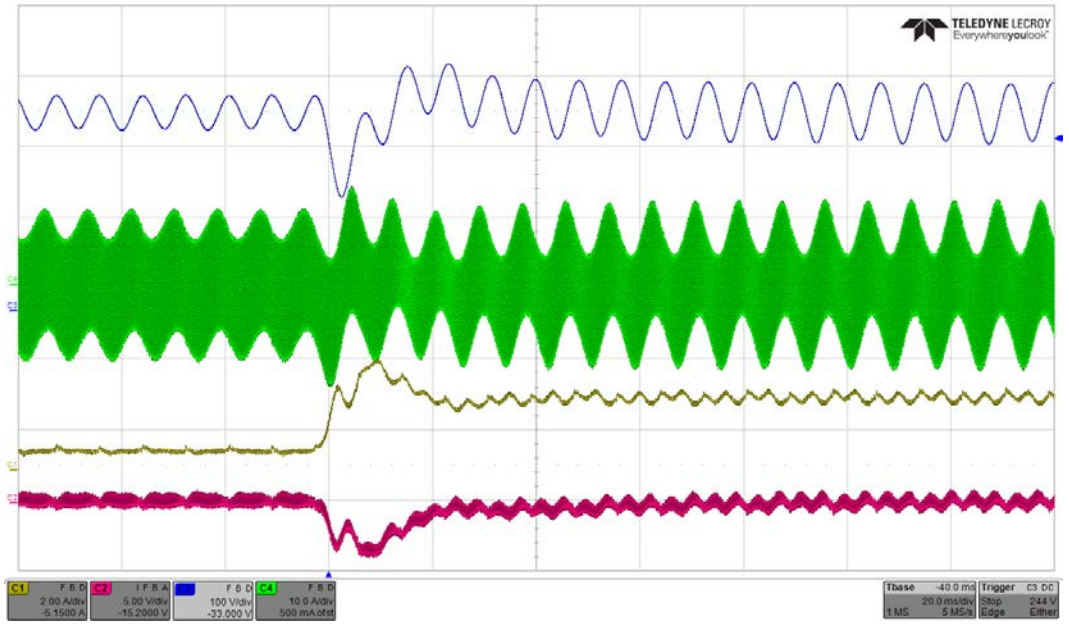
AC current (5 A/div)
AC voltage (200 V/div)
Buck Inductor Current (10 A/div)



- Good Performance of Output Voltage Controller

Little Box 2.0 – Measured Waveforms (3)

- Step-Response Waveforms for 600 W Load Step
- DC-Side and PPB Waveforms

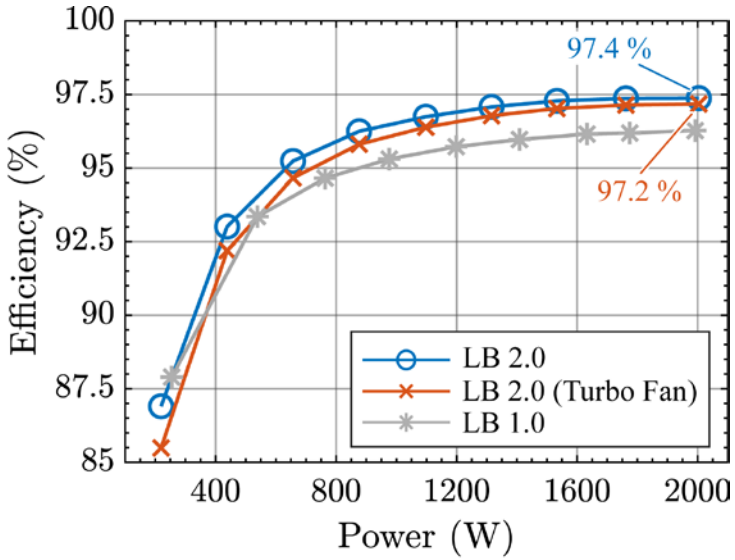


Buffer Voltage (100 V/div)
Buffer Inductor Current (10 A/div)
DC-Link Voltage (AC Coupl. 5 V/div)
Conv. Input Current (2 A/div)

- Transients Settle Within 50 ms

Little Box 2.0 – Efficiency Measurements (1)

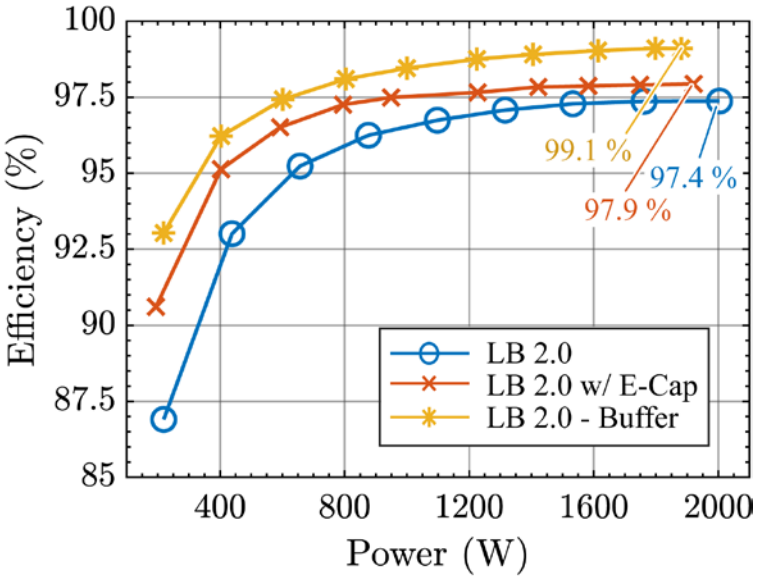
- Performance of LB 2.0 with X6S Power Pulsation Buffer
- 140 kHz PWM
- High Speed Fan for Improved Cooling



- 97.4 Peak Efficiency @ 2kW
- 96.12 % CEC Efficiency with Conv. Fans

Little Box 2.0 – Efficiency Measurements (2)

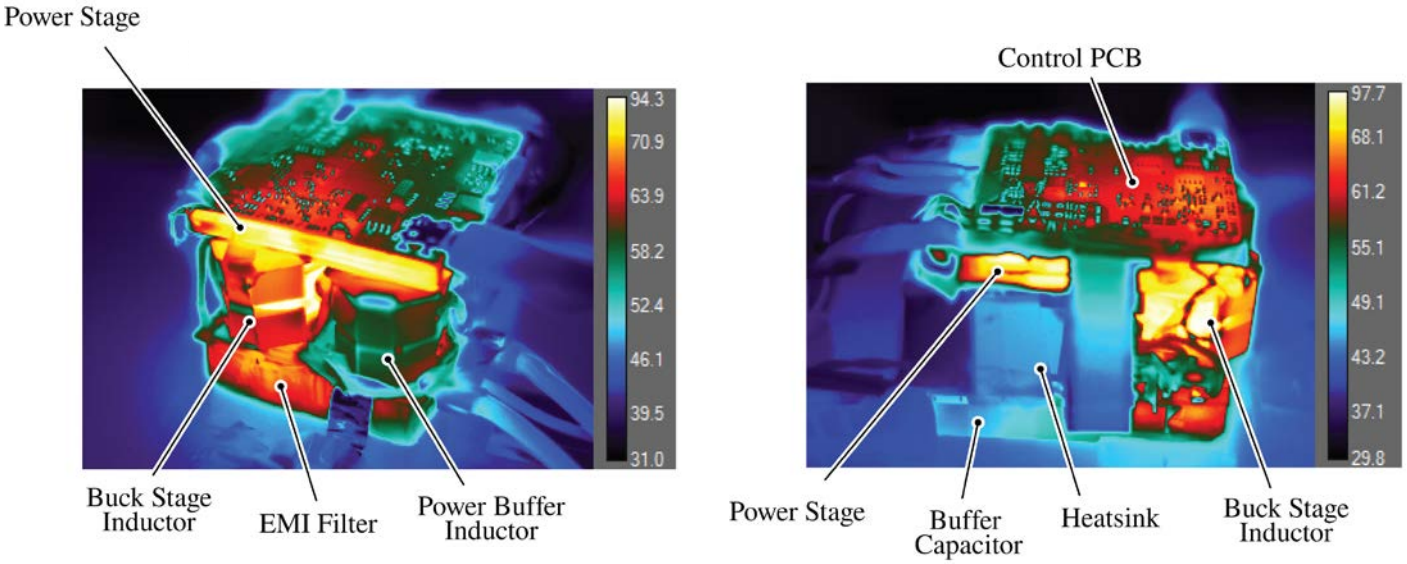
- Performance of X6S Power Pulsation Buffer
- Performance of Inverter with Electrolytic Capacitors



- 99.1% Peak Efficiency of PPB
- ≈98% Peak Efficiency of Inverter

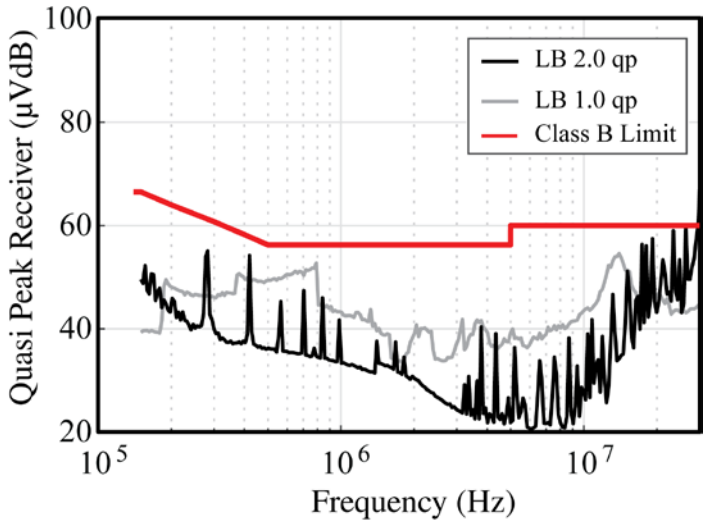
Little Box 2.0 – Thermal Management

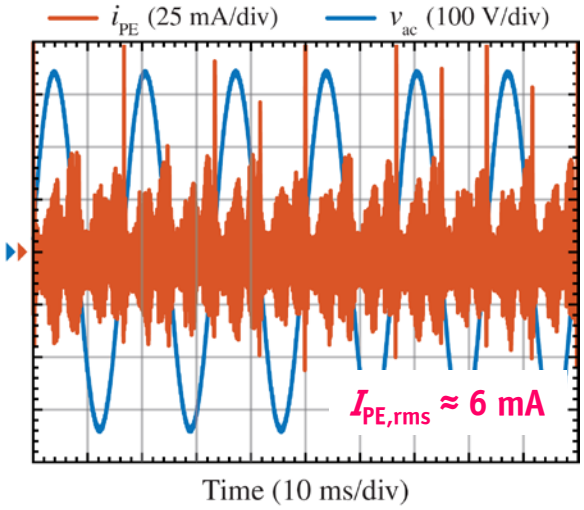
- Steady-State Operating Temperature @ 2 kW
- CSPI = 53 W/(dm^3.K)



- 60°C - 65°C of Exposed Surfaces
- 85°C Winding Temperature
- CSPI = 37.5 W/(dm3.K) Including Air Duct

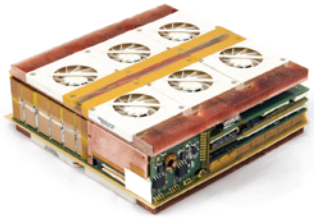
Little Box 2.0 – EMI Measurements

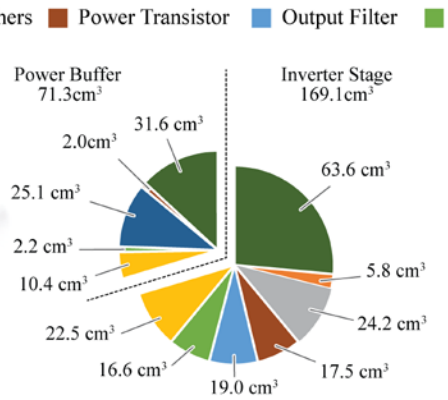




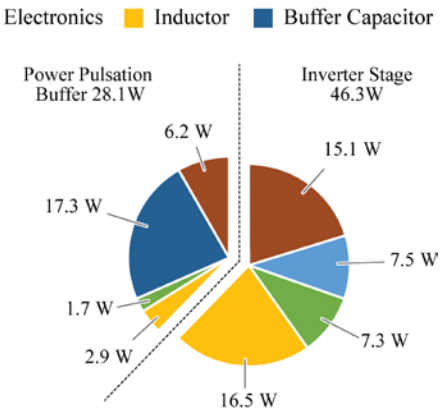
- Compliant to FCC Part 15 B EMI Limits
- Compliant to Revised 50 mA Ground Current Limit

Little Box Comparison - Volume and Loss Distribution

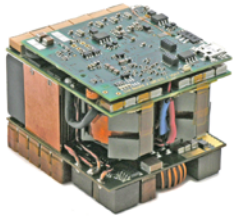


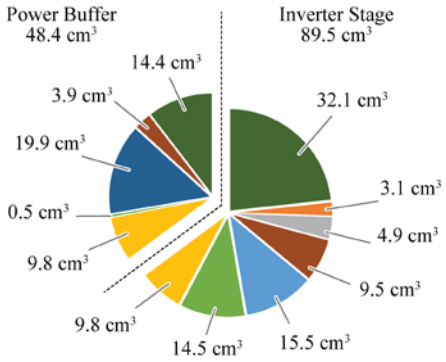


Tot. Volume: 240.5 cm³

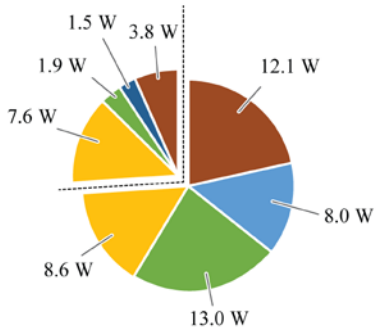


Tot. Losses: 74.4 W





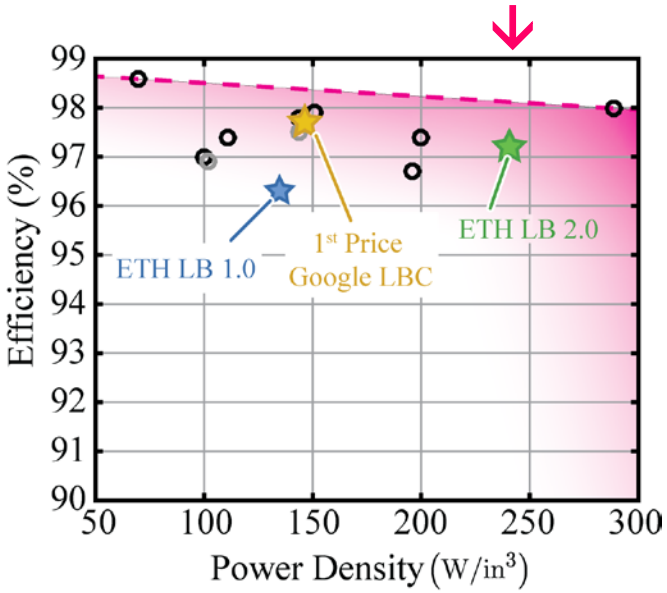
Tot. Volume: 137.9 cm³



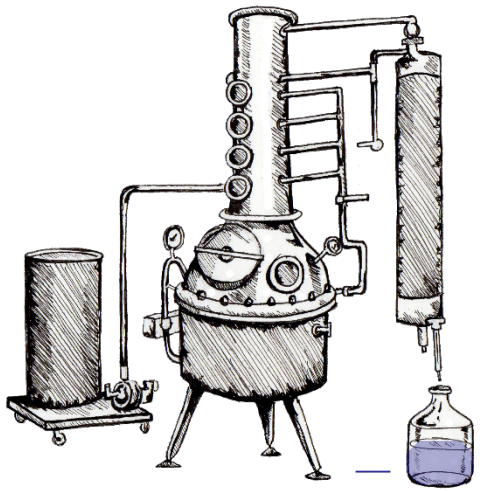
Tot. Losses: 56.4 W

Finalists - Performance Overview Revisited

- **18 Finalists (3 No-Shows)**
- 7 Groups of Consultants / 7 Companies / 4 Universities



- **70…300 W/in³**
- **35 kHz…500kHz…1 MHz** (up to 1MHz: 3 Teams)
- Full-Bridge or DC/|AC| Buck Converter + Unfolder
- Mostly Buck-Type Active Power Pulsation Filters (Ceramic Caps of Electrolytic Caps)
- **GaN (11 Teams)** / SiC (2 Teams) / Si (2 Teams)



Source: whiskeybehavior.info

Overall Summary

Performance Limits / Future Requirements

- 220...250W/in^3 for Two-Level Bridge Leg + Unfolder
- 250...300W/in^3 for Highly Integrated Multi-Level Approach
- Isol. Distance Requirements Difficult to Fulfill
- Fulfilling Industrial Inp. Overvoltage Requirem. would Signific. Reduce Power Density

- Low Frequency (20kHz...120kHz) SiC vs. HF (200kHz...1.2MHz) GaN
- Multi-Cell Concepts for LV Si (or GaN) vs. Two-Level SiC (or GaN)

- New Integr. Control Circuits and i=0 Detection for Sw. Frequency >1MHz
- Integrated Gate Drivers & Switching Cells
- High Frequency Low Loss Magnetic Materials
- High Bandwidth Low-Volume Current Sensors
- Low Loss Ceramic Capacitors Tolerating Large AC Ripple
- Passives w. Integr. Heat Management and Sensors
- 3D Packaging

- New U-I-Probes Required for Ultra-Compact Conv. R&D
- Specific Systems for Testing → Devices Equipped with Integr. Measurement Functions
- Convergence of Sim. & Measurem. Tools → Next Gen. Oscilloscope
- New Multi-Obj. Multi-Domain Simulation/Optim. Tools

References

ETH Zurich
Other Finalists
Non-Finalists
General

▶ Publications of ETH Zurich

D. Neumayr, D. Bortis, E. Hatipoglu, J. W. Kolar, G. Deboy, *New Efficiency Optimal Frequency Modulation (OFM) for High Power Density DC/AC Converter Systems*, to be published in Proc. of the International Future Energy Electronics Conference (IFEEC-ECCE Asia), Kaohsiung, Taiwan, June 3-7, 2017.

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D. Bortis, D. Neumayr, J. W. Kolar, *ηρ-Pareto Optimization and Comparative Evaluation of Inverter Concepts considered for the GOOGLE Little Box Challenge*, Proceedings of the 17th IEEE Workshop on Control and Modeling for Power Electronics (COMPEL), Trondheim, Norway, June 27-30, 2016.

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l. Zhang, R. Born, X. Zhao, J.S. Lai, *A High Efficiency Inverter Design for Google Little Box Challenge,* Proc. of the IEEE Workshop on Wide Bandgap Power Devices and Applications (WiPDA), 2015.

C. Zhao, B. Trento, L. Jiang, E. A. Jones, B. Liu, Z. Zhang, D. Costinett, F. Wang, L. M. Tolbert, J. F. Jansen, R. Kress, R. Langley, *Design and Implementation of GaN-Based 100-kHz 102-W/in^3 Single-Phase Inverter,* IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 4, no. 3, pp. 824–840.

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R. W. Erickson, A. P. Rogers, *A Microinverter for Building-Integrated Photovoltaics,* Proc. of the IEEE Applied Power Electronics Conference (APEC), 2009, pp. 911-917 .

M. Pahlevaninezhad, P. Jain, *Zero Voltage Switching Interleaved Boost AC/DC Converter,* US Patent US 8723487B2 (May 13, 2014), filed March 9, 2012.

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Johann W. Kolar (F´10) received his Ph.D. degree (summa cum laude) from the Vienna University of Technology, Austria. He is currently a Full Professor and the Head of the Power Electronic Systems Laboratory at the Swiss Federal Institute of Technology (ETH) Zurich. He has proposed numerous novel PWM converter topologies, and modulation and control concepts and has supervised over 60 Ph.D. students. He has published over 750 scientific papers in international journals and conference proceedings, 3 book chapters, and has filed more than 140 patents. He has presented over 20 educational seminars at leading international conferences, has served as IEEE PELS Distinguished Lecturer from 2012 through 2016, and has received 25 IEEE Transactions and Conference Prize Paper Awards, the 2014 IEEE Power Electronics Society R. David Middlebrook Achievement Award, the 2016 IEEE William E. Newell Power Electronics Award, the 2016 IEEE PEMC Council Award, and the ETH Zurich Golden Owl Award for excellence in teaching. He has initiated and/or is the founder of 4 ETH Spin-off companies. The focus of his current research is on ultra-compact and ultra-efficient SiC and GaN converter systems, wireless power transfer, Solid-State Transformers, Power Supplies on Chip, as well as ultra-high speed and ultra-light weight drives, bearingless motors, and energy harvesting.

Dominik Neumayr (SM10) started his academic education at the University of Applied Sciences (FH) for Automation Engineering in Wels and received the Dipl.-Ing. (FH) degree in 2008. He was with the Center for Advanced Power Systems (CAPS) in Tallahassee/Florida working on Power/Controller Hardware-in-the-Loop simulations and control systems design for AC/DC/AC PEBB based converter systems from ABB. He continued his academic education at the Swiss Federal Institute of Technology in Zurich (ETH Zurich) and received the M.Sc. degrees in electrical engineering and information technology in 2015. Since spring 2015 he is a PhD student at the Power Electronic Systems (PES) Laboratory, ETH Zurich. His current research focuses on ultra-high power density converter systems.

Dominik Bortis (M´08) received the M.Sc. degree in electrical engineering and the Ph.D. degree from the Swiss Federal Institute of Technology (ETH) Zurich, Switzerland, in 2005 and 2008, respectively. In May 2005, he joined the Power Electronic Systems Laboratory (PES), ETH Zurich, as a Ph.D. student. From 2008 to 2011, he has been a Postdoctoral Fellow and from 2011 to 2016 a Research Associate with PES, co-supervising Ph.D. students and leading industry research projects. Since January 2016 Dr. Bortis is heading the newly established research group Advanced Mechatronic Systems at PES.

Thank You !