3-Φ SiC/GaN Converter Systems

Johann W. Kolar et al.

Swiss Federal Institute of Technology (ETH) Zurich
Power Electronic Systems Laboratory
www.pes.ee.ethz.ch

Feb. 23, 2021

3-Φ SiC/GaN Converter Systems … There is No

Under the Bed

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ETH zürich

POWERAMERICA

3-Φ SiC/GaN Converter Systems

... BUT Lots of Opportunities & Some Challenges ;-)

Johann W. Kolar | Jonas E. Huber | David Menzi

Swiss Federal Institute of Technology (ETH) Zurich
Power Electronic Systems Laboratory
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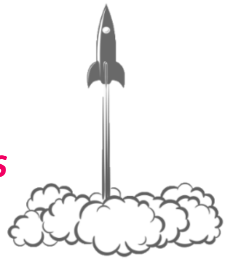
Outline

- ► *Introduction*
- ► *Performance Trends*
- ► *10x –Technologies / Concepts*
- ► *Research Results*
- ► *Conclusions*



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Adv. Mechatronic Systems
D. Bortis

AC-DC Converter	AC-AC Converter	DC-DC Converter	DC-AC Converter	Multi-Domain Modeling	Measurement Technology	Advanced Mechatronics	Magnetic Levitation
J. Huber		**F. Krismer**	**D. Bortis**	**F. Krismer**		**D. Bortis**	**D. Bortis**
		J. Schäfer					
N. Nain Y. Li D. Zhang	M. Heller J. Azurza M. Haider D. Menzi	P. Czyz P. Bezerra G. Knabben	J. Böhler G. Rohner	P. Papamanolis	P. Niklaus	R. Giuffrida S. Miric M. Röthlisberger	I. Bagaric R. Bonetti E. Hubmann

Secretariat
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Electronics Laboratory
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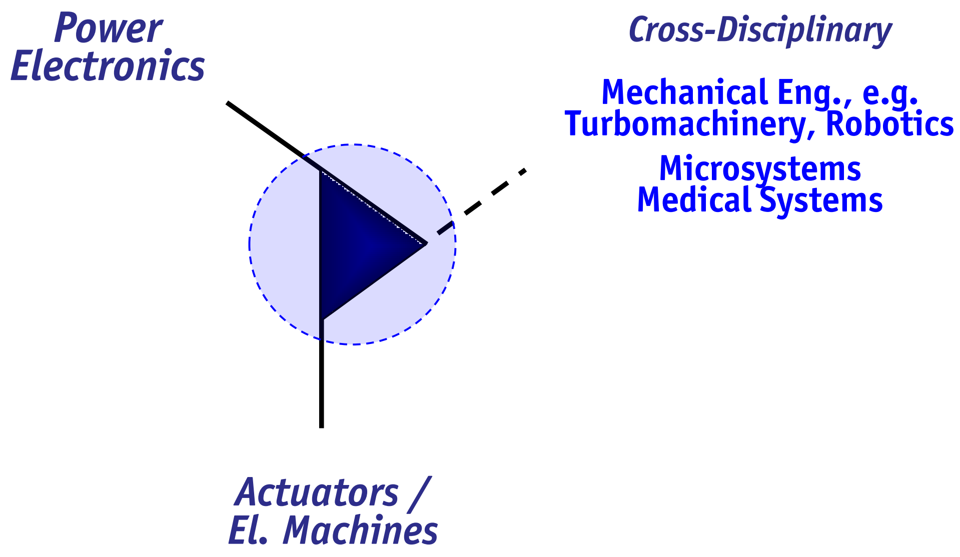
20 Ph.D. Students
1 PostDoc
3 Research Fellows

ECPE Competence Centre

EPSMA

Leading Univ. in Europe

Research Scope



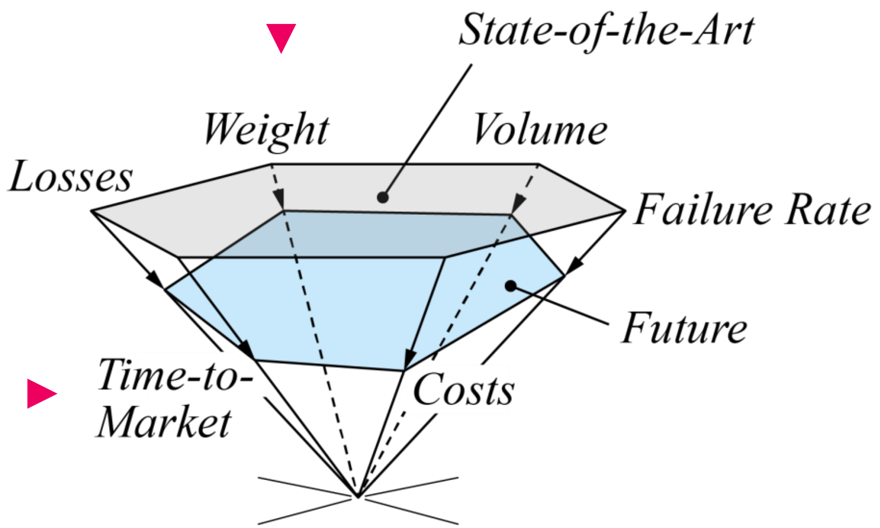
- *Explore the Limits / Create New Concepts / Push the Envelope*
- *Maximize Technology Utilization*
- *Enable New Applications*

Market Pull / Technology Push

Required Performance Improvements

Environmental Impact... [kg_{Fe} /kW]
[kg_{Cu} /kW]
[kg_{Al} /kW]
[cm^2_{Si} /kW]

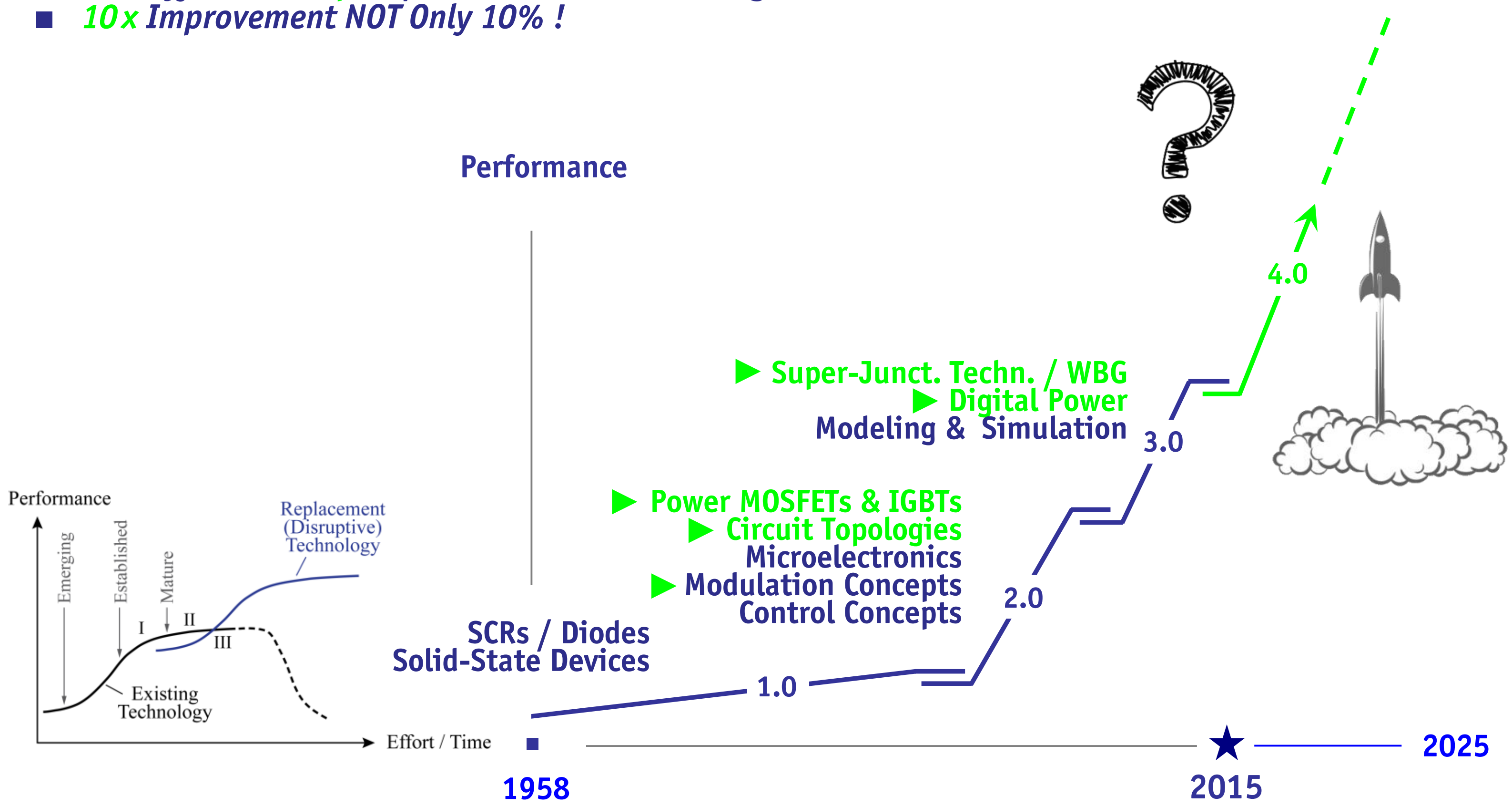
- Power Density [kW/dm³]
- Power per Unit Weight [kW/kg]
- Relative Costs [kW/$]
- Relative Losses [%]
- Failure Rate [h^{-1}]



- *Connected Cognitive Power Electronic Systems* → *Power Electronics 4.0*

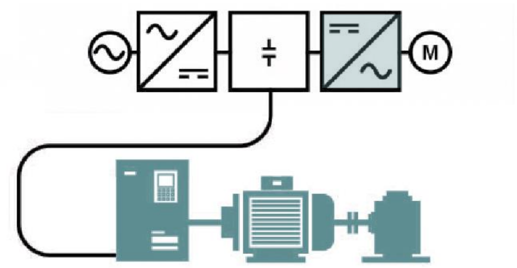
S-Curve of Power Electronics

- *Power Electronics 1.0 → Power Electronics 4.0*
- *Identify "X-Concepts" / "Moon-Shot" Technologies*
- *10x Improvement NOT Only 10% !*



3-Φ Variable Speed Drive Inverter Systems

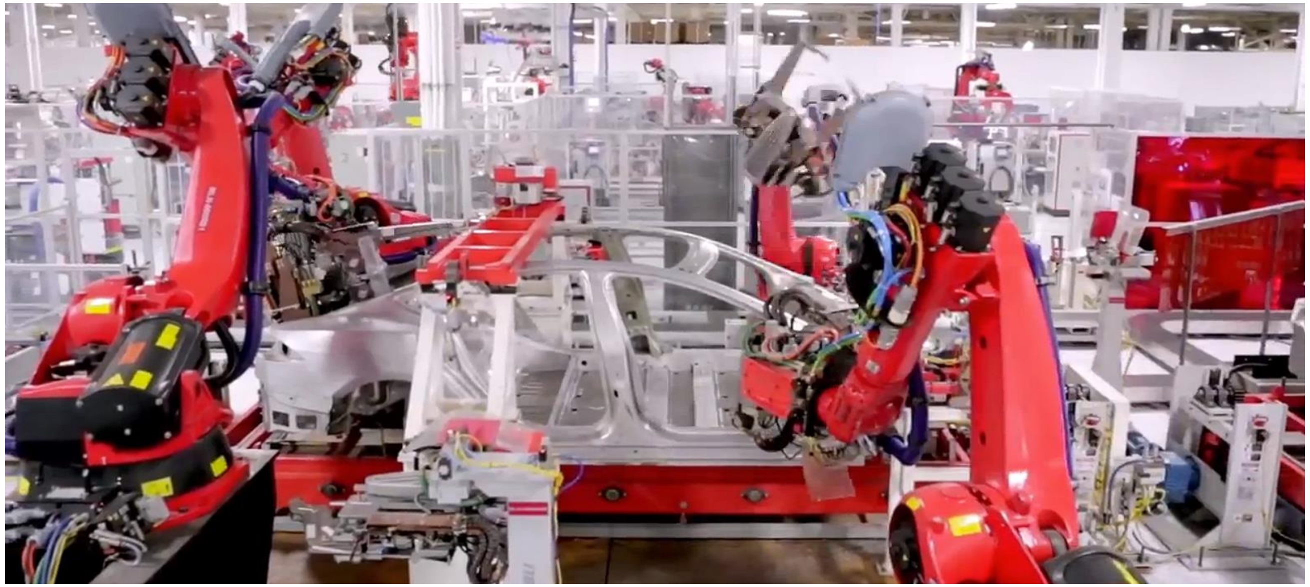
State-of-the-Art
Future Requirements



Source: PowerAmerica

Variable Speed Drive (VSD) Systems

- Industry Automation / Robotics
- Material Machining / Processing – Drilling, Milling, etc.
- Compressors / Pumps / Fans
- Transportation
- etc., etc. .... Everywhere !

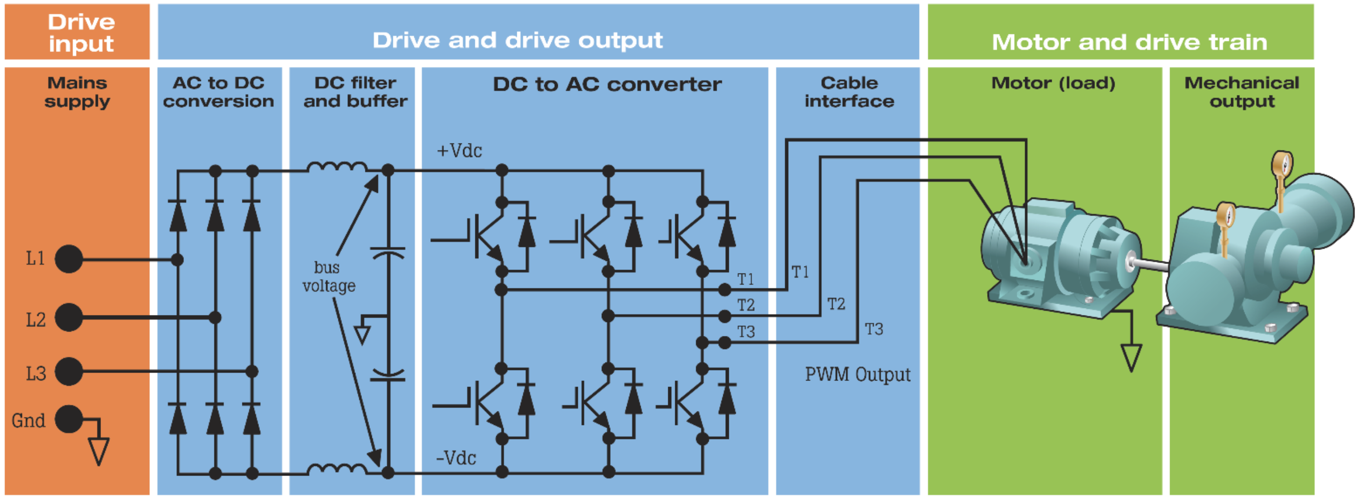


Source: TESLA MOTORS

- *60...70 % of All Electric Energy Used in Industry Consumed by VSDs*

State-of-the-Art

- *Mains Interface / 3-Φ PWM Inverter / Cable / Motor — Large Installation Space / Complicated*
- *Conducted EMI / Radiated EMI / Reflections on Long Motor Cables / Bearing Currents*



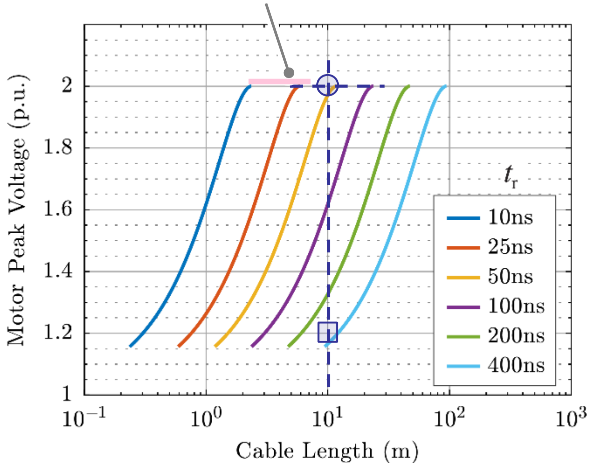
Source: FLUKE

- *High Performance @ High Level of Complexity / High Costs (!)*

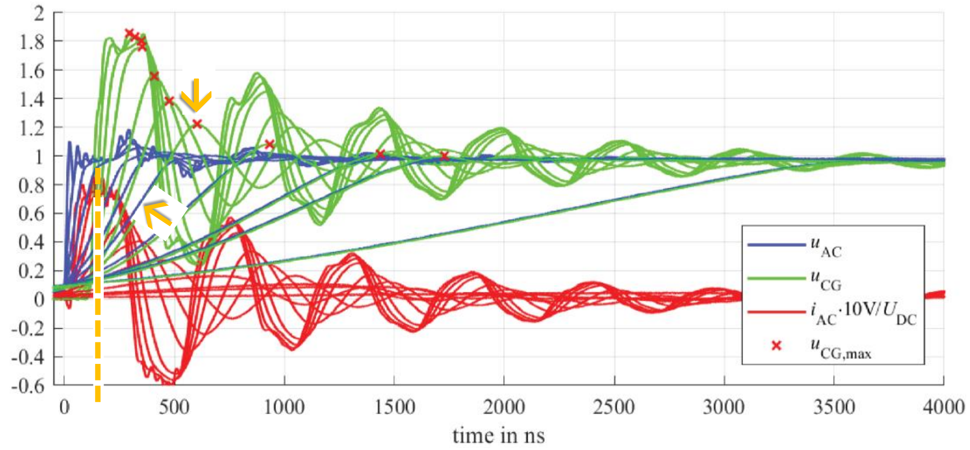
Surge Voltage Reflections

- *Long Motor Cable $l_c \geq ½\, t_r v$*
- *Short Rise Time of Inverter Output Voltage*
- *Impedance Mismatch of Cable & Motor → Reflect. @ Motor Terminals / High Insul. Stress*

SiC



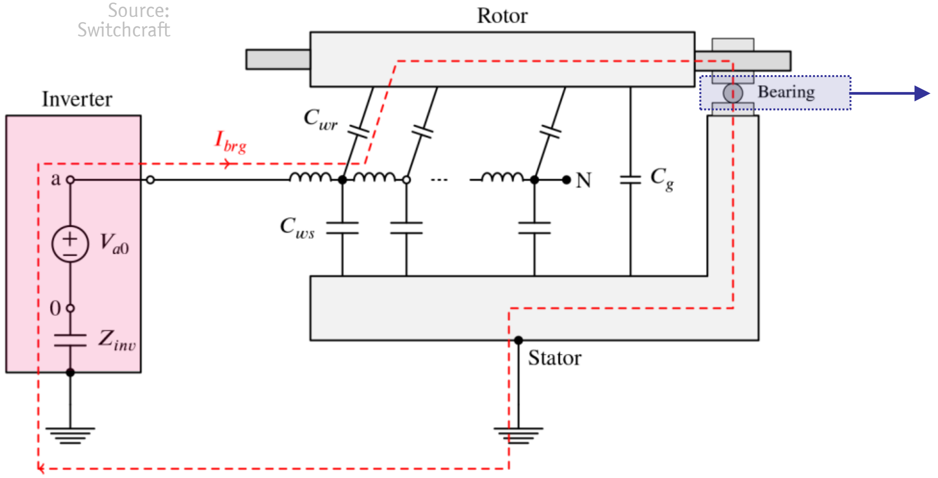
Source: Bakran / ECPE 2019

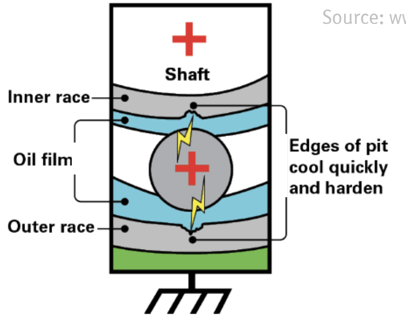


→ *dv/dt- OR Full-Sinewave Filtering / Termination & Matching Networks etc.*

Motor Bearing Currents

- *Switching Frequency CM Inverter Output Voltage → Motor Shaft Voltage*
- *Electrical Discharge in the Bearing ("EDM")*



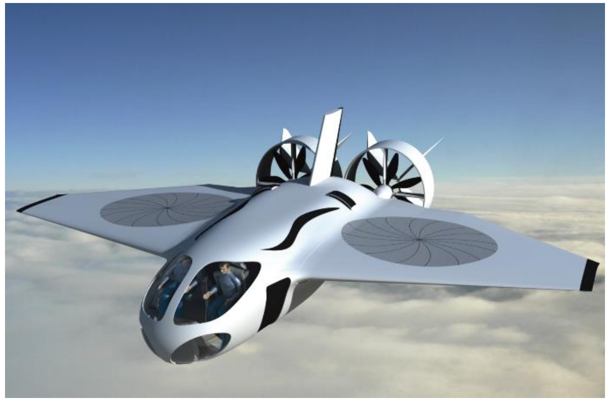


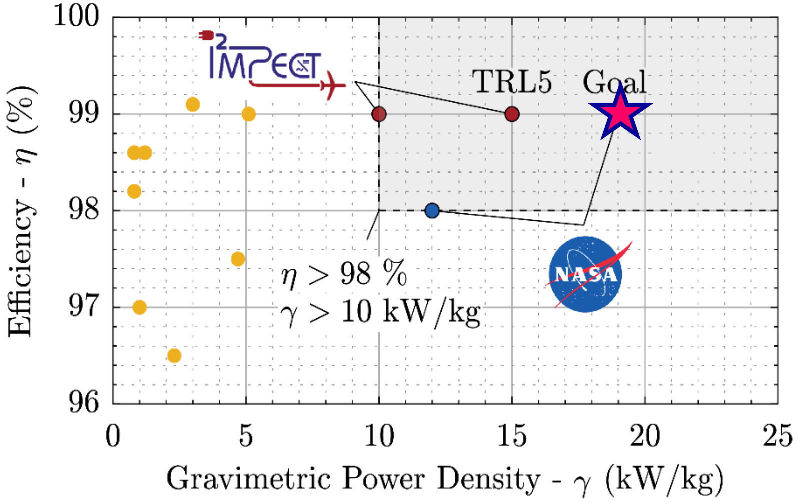
→ *Cond. Grease / Ceram. Bearings / Shaft Grndg Brushes / dv/dt- OR Full-Sinewave Filters*

VSD Inverter - Future Requirements

- *"Non-Expert" Installation / "Sinus-Inverter" OR Motor-Integrated Inverter*
- *Low Losses & Low HF Motor Losses*
- *Low Volume & Weight*
- *Wide Output Voltage Range*
- *High Output Frequencies*

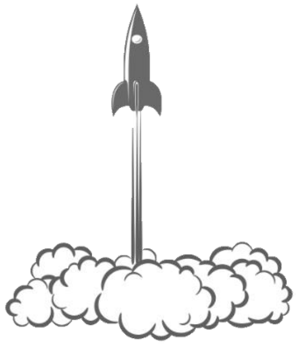
Source: Georgia Tech





- *Main "Enablers" → SiC/GaN Power Semiconductors & Adv. Inverter Topologies*

X-Technology #1

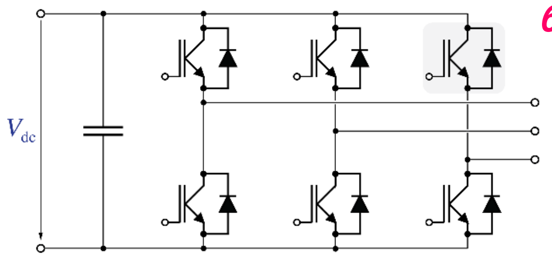


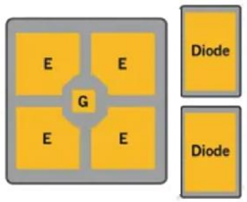
**Wide Bandgap
Power Semiconductors**

Si vs. SiC

- Si-IGBT / Diode → Const. On-State Voltage, Turn-Off Tail Current & Diode Reverse Recovery Current
- SiC-MOSFET → Massive Loss Reduction @ Part Load BUT Higher R_{th}

6x Si-IGBT
6x Si-Diode

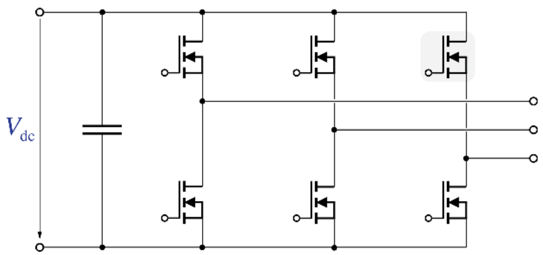




Source: ATZ elektronik 2018

1200V 100A
Die Size: 98.8 mm² + 39.4 mm²

6x SiC-MOSFET



1200V 100A
Die Size: 25.6 mm²

Source: Cree

- Space Saving of >30% on Module Level (!)

Low $R_{DS(on)}$ High-Voltage Devices

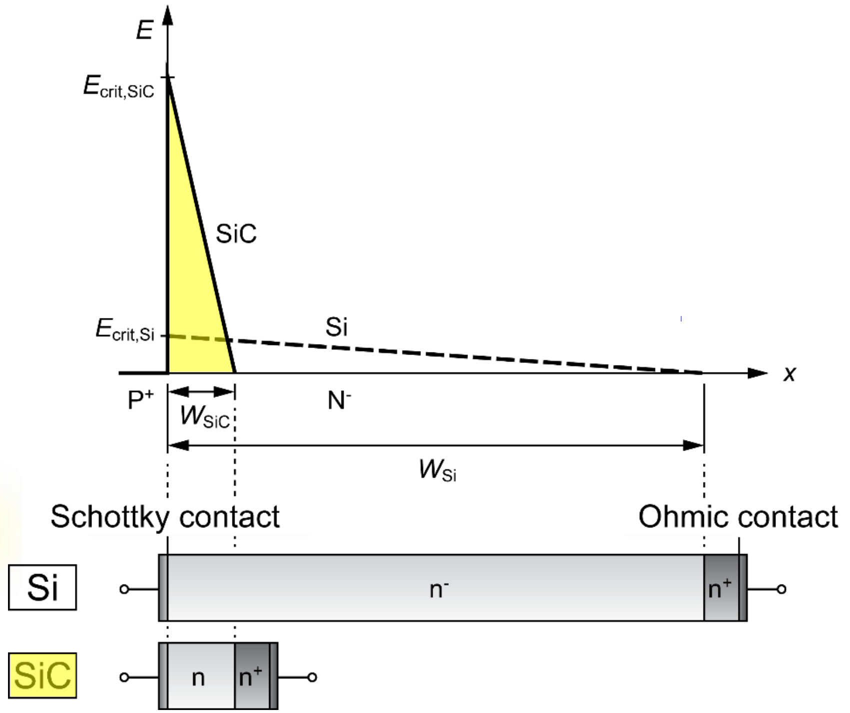
- *Higher Critical E-Field of SiC → Thinner Drift Layer*
- *Higher Maximum Junction Temperature $T_{j,max}$*

at 300 K	Si	GaAs	4H/6H-SiC	GaN
Eg (eV)	1.12	1.4	3.0-3.2	3.4
Ec (MV/cm)	0.25	0.3	2.2-2.5	3
μ_n (cm²/Vs)	1350	8500	100-1000	1000
ε_r	11.9	13	10	9.5
Vsat (cm/s)	1×10^7	1×10^7	2×10^7	3×10^7
λ (W/cmK)	1.5	0.5	3 - 5	1.3

$$R^*_{on} = \frac{4V_B^2}{\varepsilon\mu_n E_C^3} \leftarrow$$

For 1kV:	Si	SiC
W (µm)	100	10
N_D (cm^{-3})	10^{14}	10^{16}

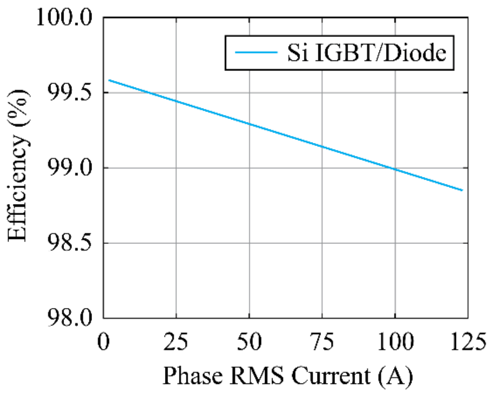
$$R^*_{on,SiC} \approx \frac{1}{300} R^*_{on,Si}$$

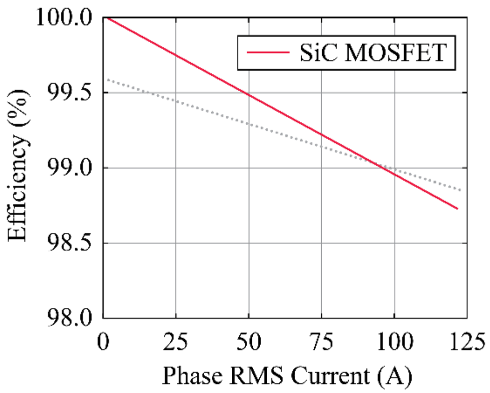


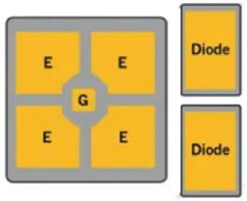
- *Massive Reduction of Relative On-Resistance → High Blocking Voltage Unipolar Devices*

Si vs. SiC Conduction Behavior

- ***Si-IGBT*** → ***Const. On-State Voltage Drop / Rel. Low Switching Speed,***
- ***SiC-MOSFETs*** → ***Resistive On-State Behavior / Factor 10 Higher Sw. Speed***







1200V 100A
Die Size: 98.8 mm² + 39.4 mm²

Source: Infineon

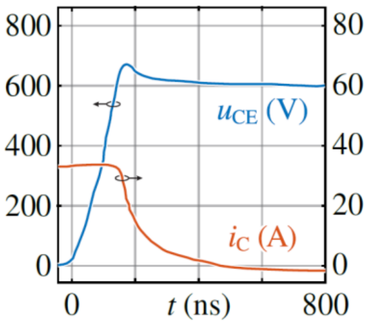
1200V 100A
Die Size: 25.6 mm²

Source: Cree

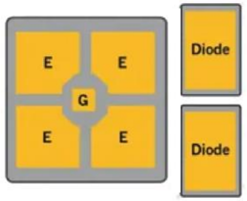
- ***Efficiency Characteristic Considering Only Conduction Losses***

Si vs. SiC Switching Behavior

- *Si-IGBT* → *Const. On-State Voltage Drop / Rel. Low Switching Speed,*
- *SiC-MOSFETs* → *Resistive On-State Behavior / Factor 10 Higher Sw. Speed*

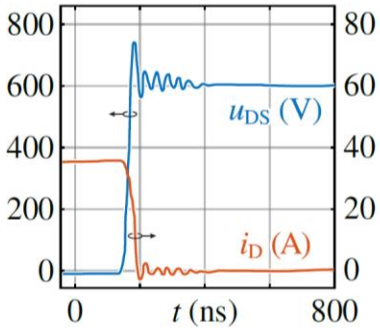


Source: Fuji Electric



1200V 100A
Die Size: 98.8mm² + 39.4mm²

Source: Infineon

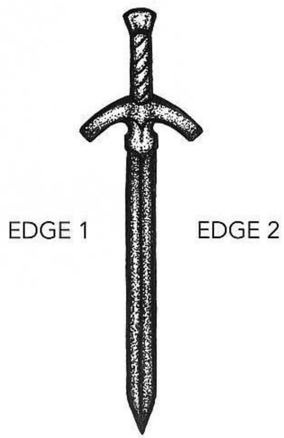


1200V 100A
Die Size: 25.6mm²

Source: Cree

- *Extremely High di/dt & dv/dt* → *Challenges in Packaging / EMI / Motor Insulation / Bearing Currents*

Challenges

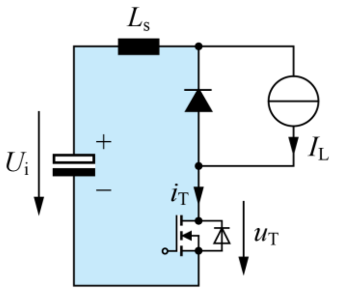


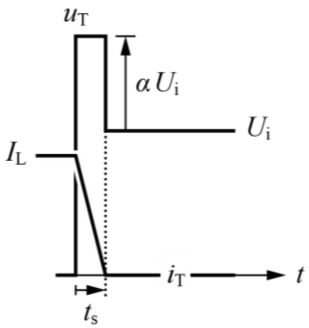
Circuit Parasitics

$$L\frac{di}{dt} = u$$

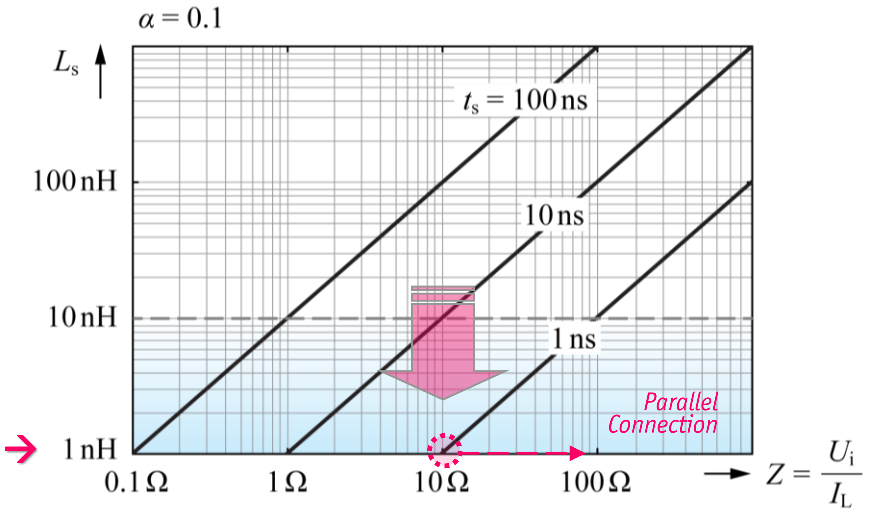
- *Extremely High di/dt*
- *Commutation Loop Inductance L_s*
- Allowed L_s Directly Related to Switching Time t_s →

$$L_s \leq \frac{\alpha U_i}{\frac{I_L}{t_s}} = \alpha t_s \underbrace{\frac{U_i}{I_L}}_{Z}$$





→

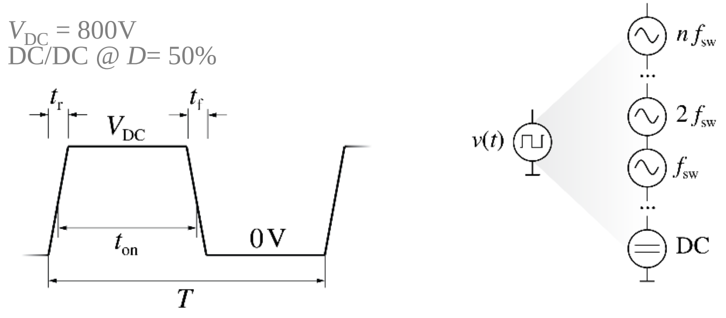


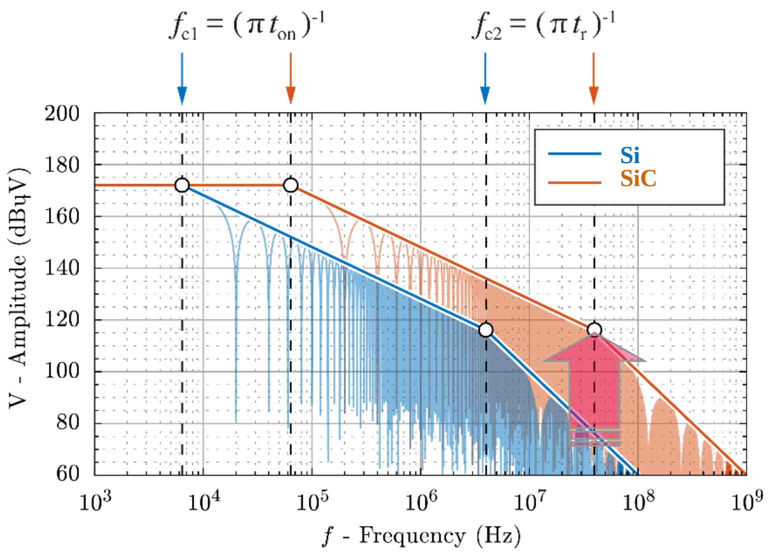
- *Advanced Packaging & Parallel Interleaving for Partitioning of Large Currents*

Si vs. SiC EMI Emissions

- *Higher dv/dt* → *Factor 10*
- *Higher Switching Frequencies* → *Factor 10*
- *EMI Envelope Shifted to Higher Frequencies*

f_S= 10kHz & 5 kV/us for (Si IGBT)
f_S= 100kHz & 50 kV/us for (SiC MOSFET)





- *Higher Influence of Filter Component Parasitics & Couplings* → *Advanced Design*

Power Electronic Systems Laboratory

Inverter Output Filters

dv/dt-Filters
Full-Sinewave Filters

ETH zürich

PowerAmerica

Power Electronic Systems Laboratory

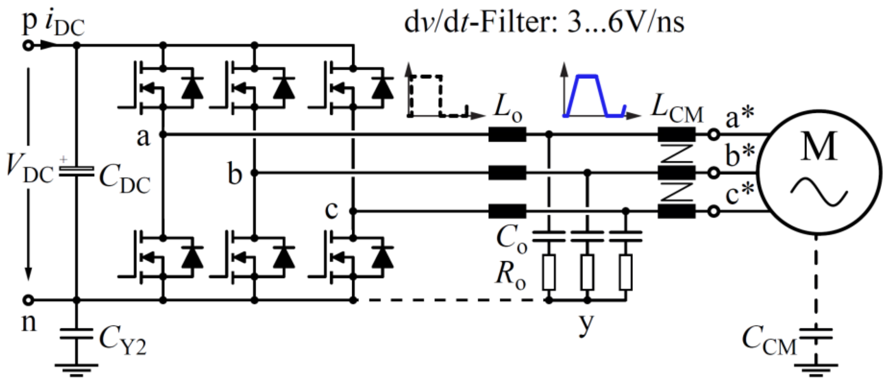
dv/dt-Control

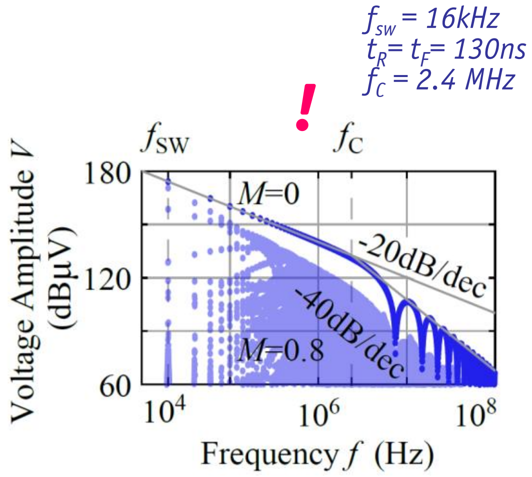
ETH zürich

POWERAMERICA

Passive | Hybrid | Active dv/dt-Limitation

- *Passive* – *Damped LC-Filter $f_C > f_S$*
- *Hybrid* – *Undamped LC-Filter & Multi-Step Sw. Transition*
- *Active* – *Gate-Drive Based Shaping of Sw. Transients*

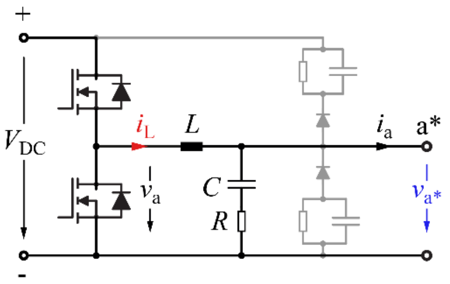


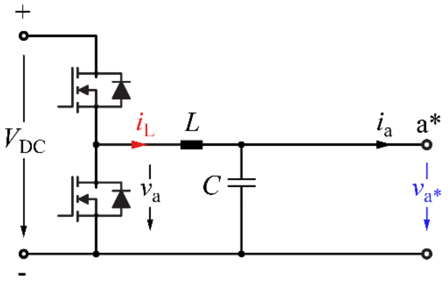


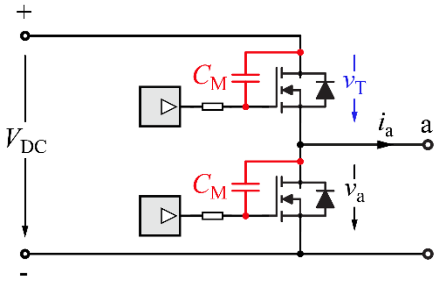
- *Connection to DC-Minus & CM Inductor* → *Limit CM Curr. Spikes / EMI / Bearing Currents*

Comparison of dv/dt-Filtering Techniques (1)

- *Passive Concept*
  1. *LCR-Filter*
  2. *Clamped LC-Filter*
- *Hybrid Concept ($3f_S$)*
  1. *LC-Filter*
  2. *Multi-Step Switching*
- *Active Concept*
  1. *Miller Capacitor*
  2. *Gate Curr. Control*

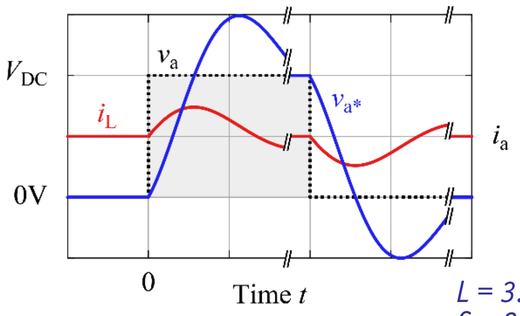




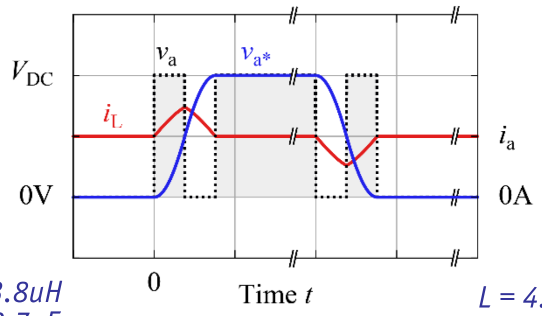


- *Output Voltage Waveforms — V_{DC} = 800V, P_{out} = 10kW, 6kV/us*

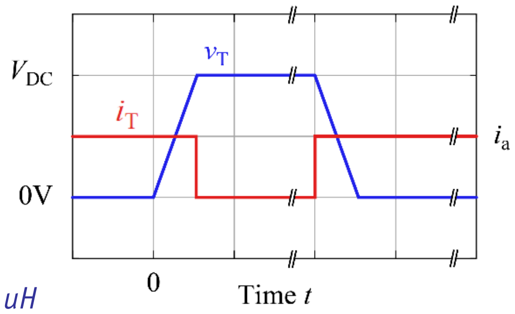
1200V SiC / 16mΩ
C_M = 120pF



L = 3.8uH
C = 2.7nF
R = 19Ω

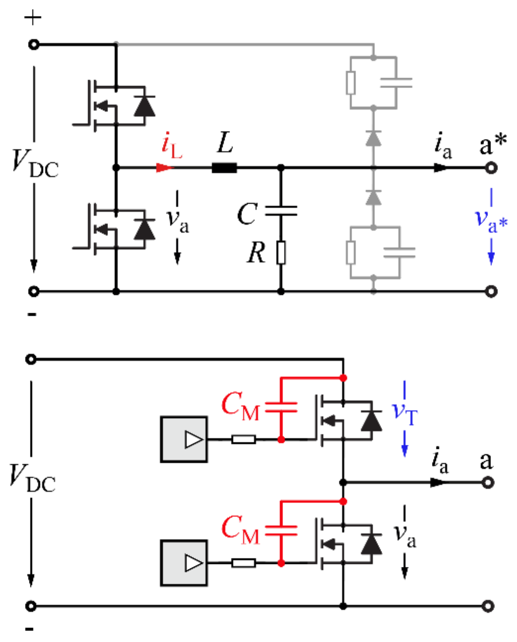


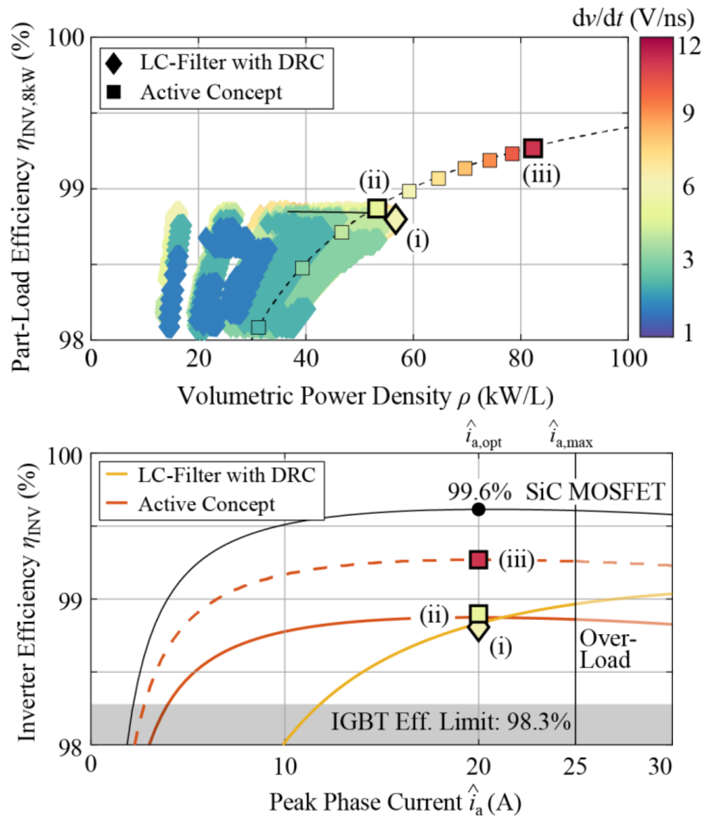
L = 4.1uH
C = 1.3nF



Comparison of dv/dt-Filtering Techniques (2)

- *Comparative Evaluation of Passive & Active Concept*



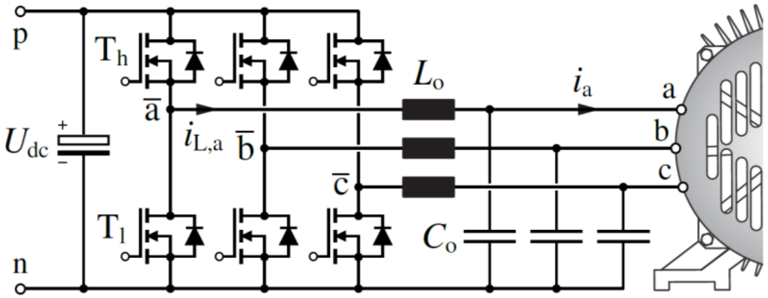


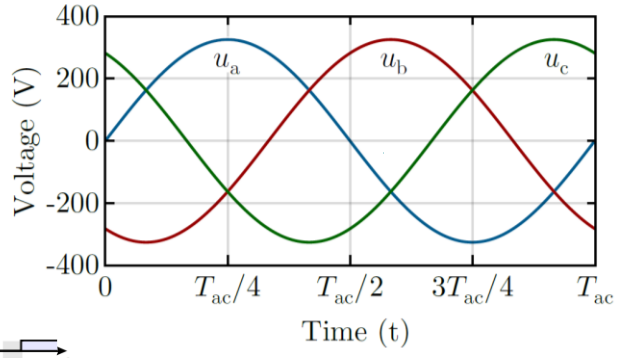
- ***Losses / Power Density*** – V_{DC} = 800V, P_{out} = 10kW, f_{sw} = 16kHz, 1200V SiC-MOSFETs (16mΩ)

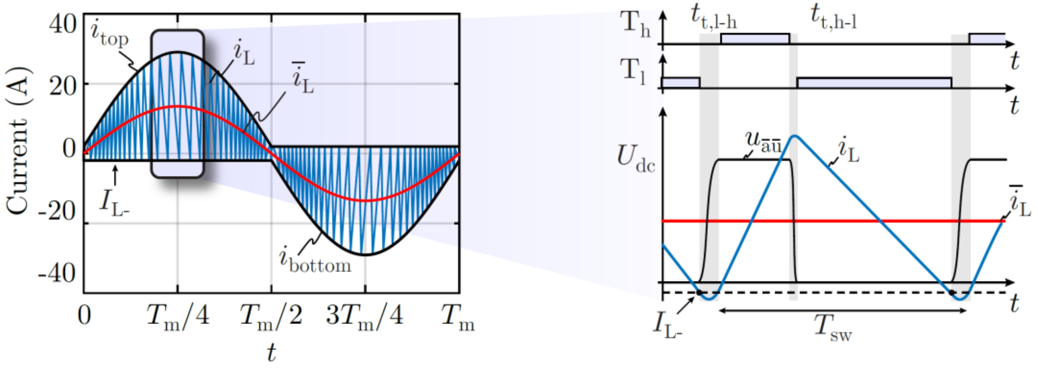
Inverter Systems w/ Sinusoidal Output Voltages

ZVS/TCM Operation

- *Sinusoidal Output Voltage*
- *ZVS of Inverter Bridge-Legs*
- *High Sw. Frequency & TCM → Low Filter Inductor Volume*





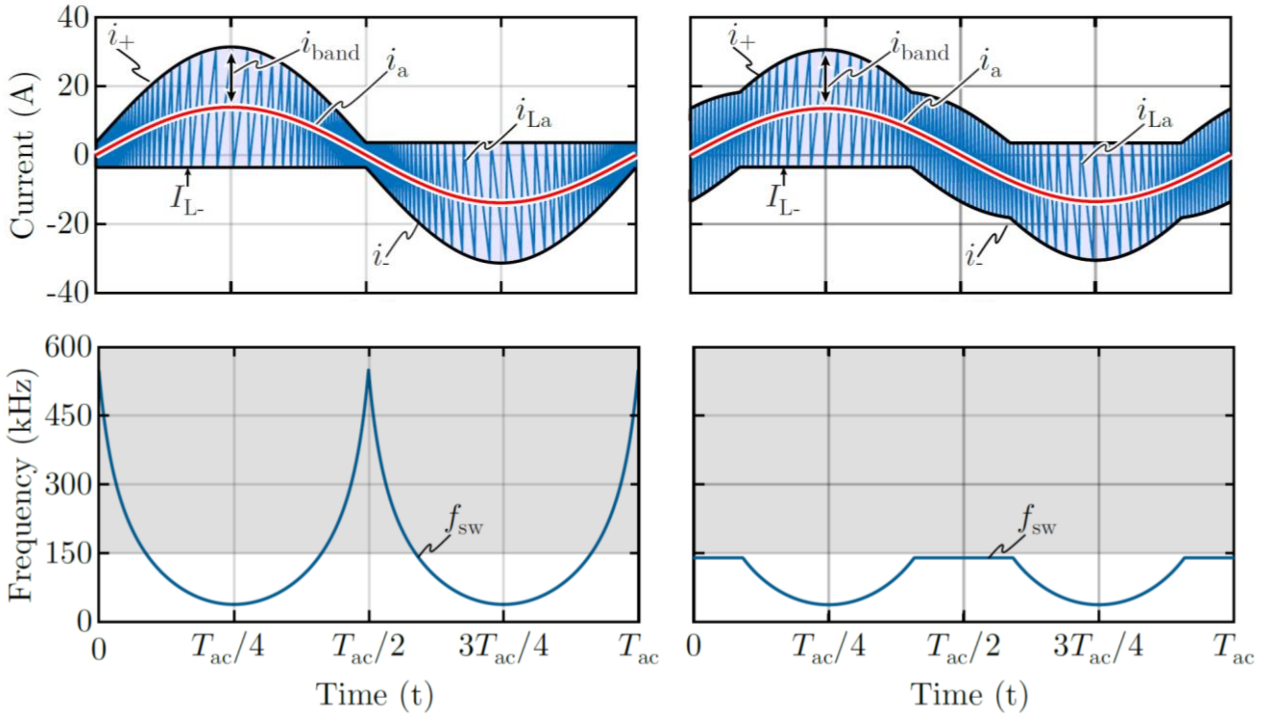


NFO Sinus

- *Only 33% Increase of Transistor Conduction Losses Compared to CCM (!)*
- *Very Wide Switching Frequency Variation*

TCM → B-TCM

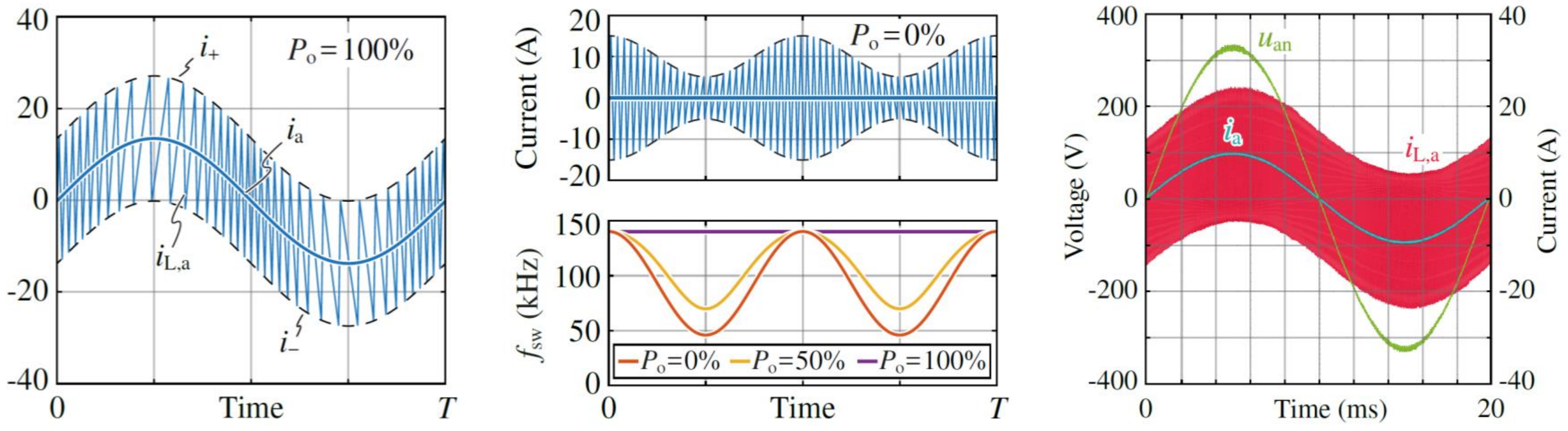
- *Very Wide Switching Frequency Variation of TCM → B-TCM*



- *TCM → B-TCM — 10% Further Increase of Transistor Conduction Losses*

B-TCM → S-TCM

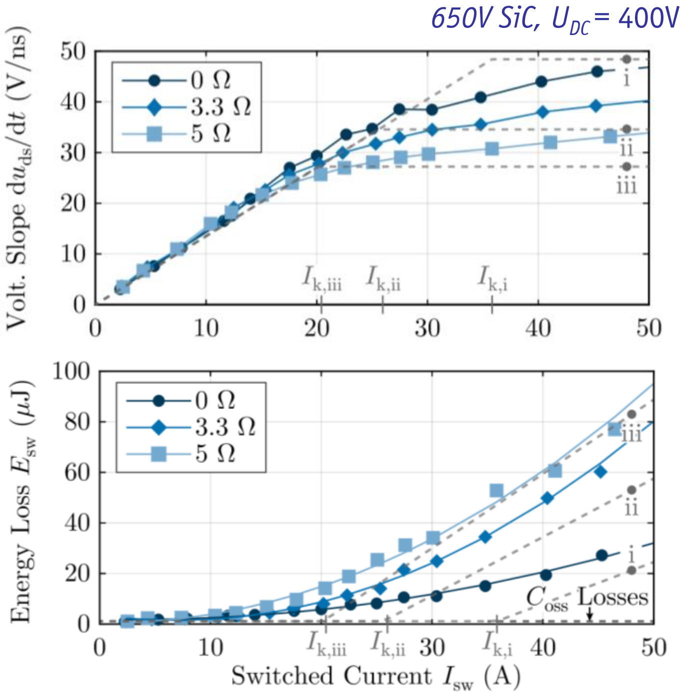
- *Sinusoidal Switching Boundaries → S-TCM*
- *Adaption for Low Output Power Considering $f_{sw,max}$= 140kHz*



- *TCM → S-TCM ≈ 10% Further Increase of Transistor Conduction Losses*

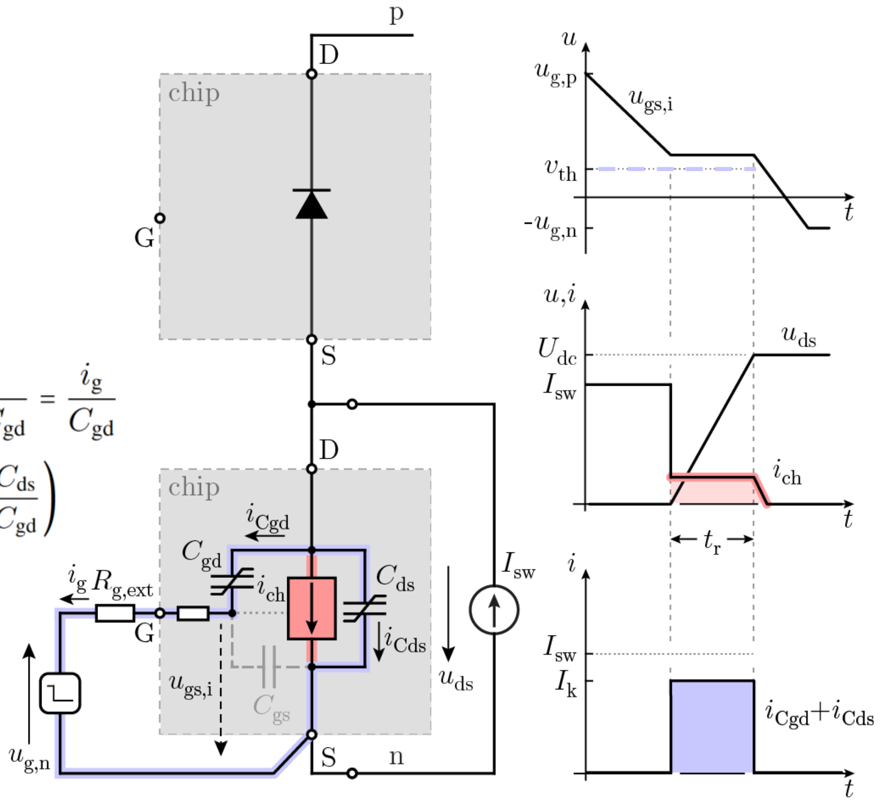
Remark Residual ZVS Losses

- *Overlap of u_{DS} & Channel Current i_{ch} @ High $I_{sw} > I_k$*
- *Temporary Turn-on Due to $u_{GS,i} > u_{th}$*



$$\left.\frac{du_{ds}}{dt}\right|_{max} = \frac{I_k}{C_{ds}+C_{gd}} = \frac{i_g}{C_{gd}}$$

$$I_k = \frac{u_{th}+u_{g,n}}{R_g}\left(1+\frac{C_{ds}}{C_{gd}}\right)$$

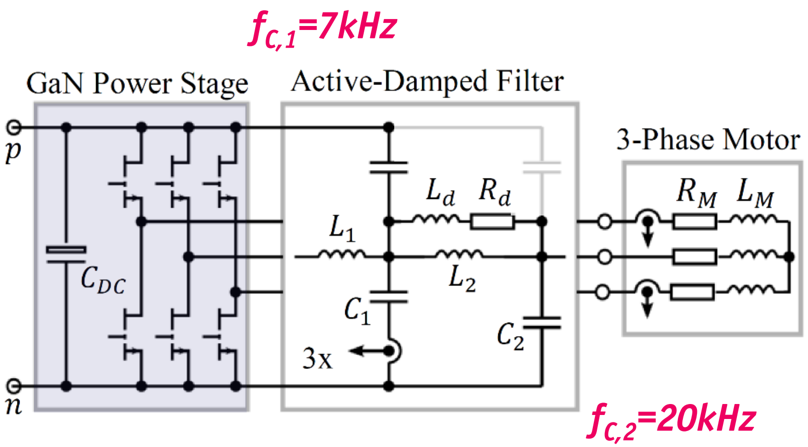


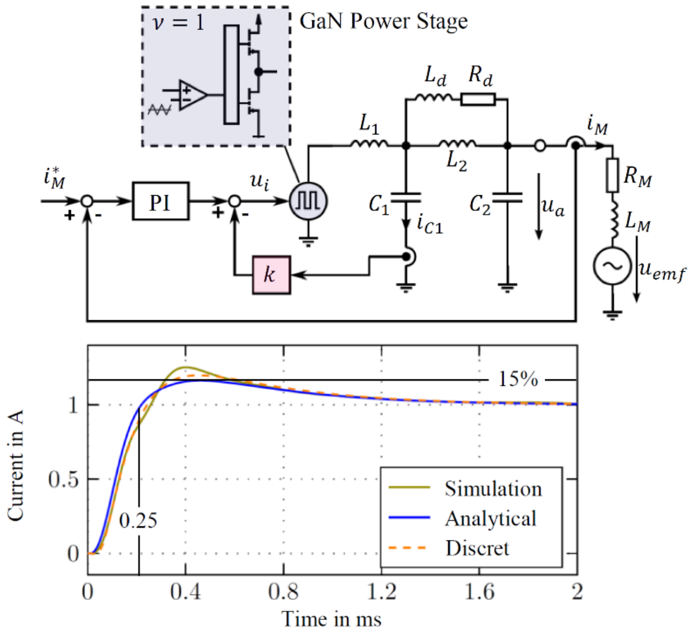
- *"Kink" Current I_K Dependent on Inner & Outer Gate Resistance & $u_{g,n}$*

CCM & 2-Stage Full-Sinewave Output Filter (1)

PERFECTION IN AUTOMATION
A MEMBER OF THE ABB GROUP
TECHNISCHE UNIVERSITÄT WIEN
Vienna | Austria

- Sinewave Output & IEC/EN 55011 Class-A
- Low-Loss Active Damping of 1st Filter Stage — Neg. Cap. Current Feedback
- 2kW / 400V DC-Link 3-Φ 650V GaN Inverter (I_M=5A), $f_{out,max}$ = 500Hz
- Sw. Frequency f_S= 100kHz

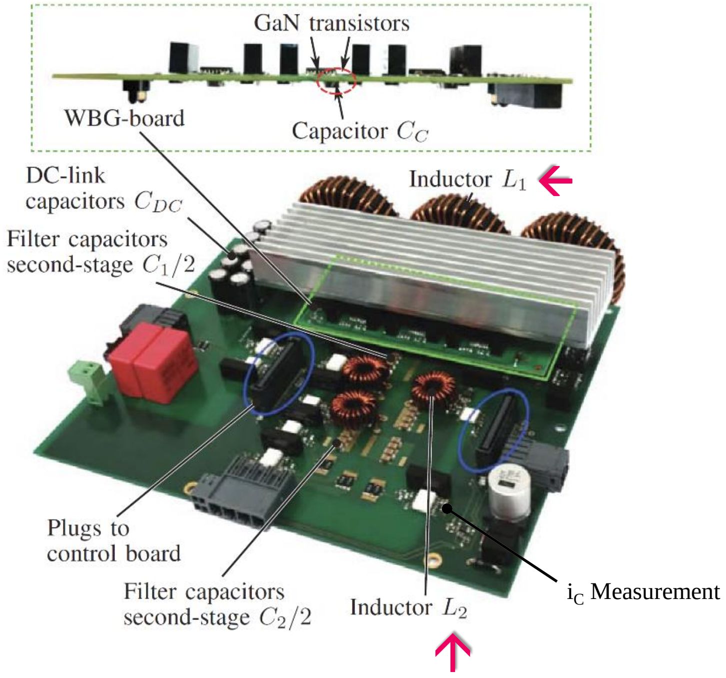


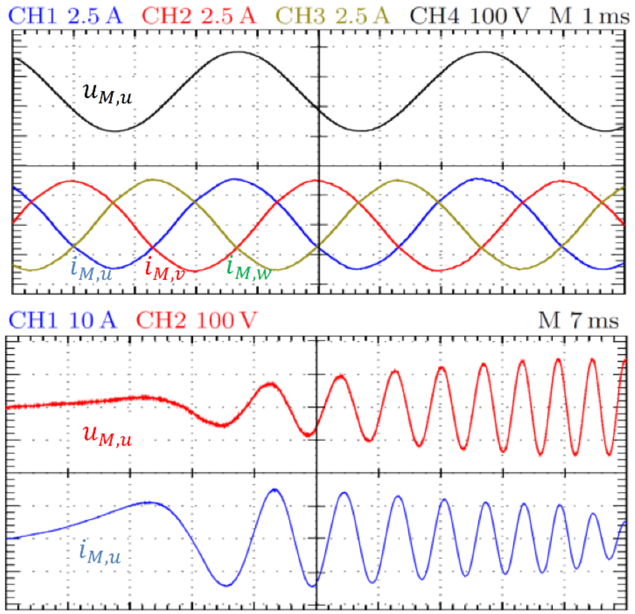


→ Evaluation of Optimized Inductors — Soft Sat. Toroidal Iron Powder Cores
→ L_1=200uH (0D57S) / C_1=2.5uF / L_2=25uH (0D20S) / C_2=2.5uF / L_d=33uH / R_d=5.6Ω

CCM & 2-Stage Full-Sinewave Output Filter (2)

- *Exp. Verification — 650V E-Mode GaN Systems Transistors (50mΩ)*
- *Sw. Frequency f_S= 100kHz, Efficiency ≈98%*
- *200mm x 250mm*

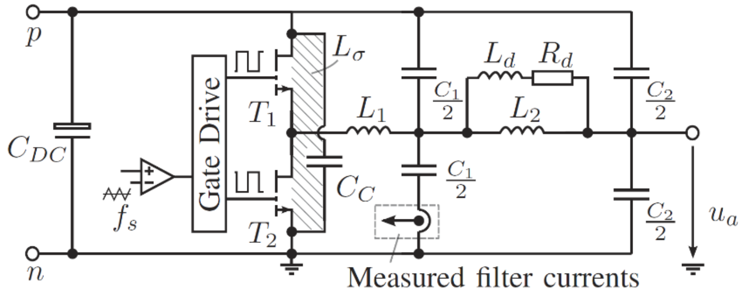


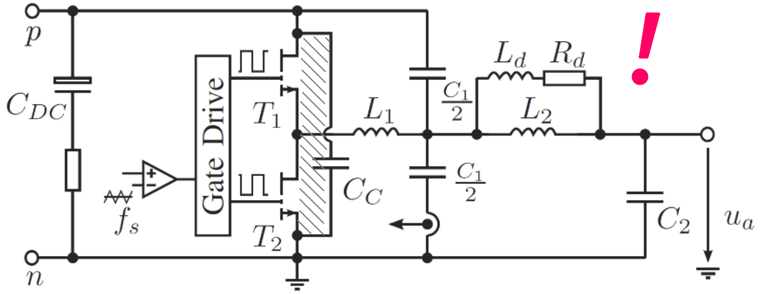


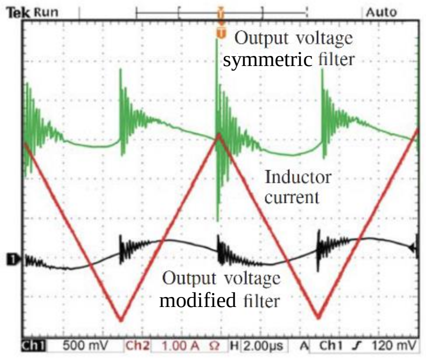
- *Stationary Motor Phase Curr. /Voltage @ 2.5Nm & f_{out}=250Hz*
- *Speed Increase from Standstill to n = 3000rpm in 60ms*

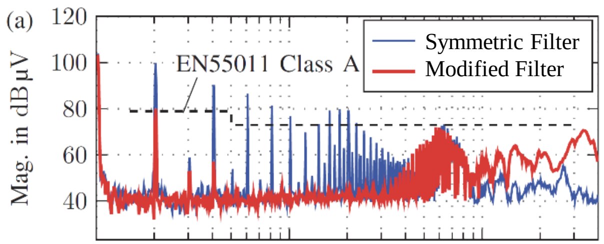
CCM & 2-Stage Full-Sinewave Output Filter (3)

- *Modification of Output Filter Structure*
- *Elimination of Direct Cap. Coupling Between Output and Noisy (!) DC+ (Due to R_{DC})*
- *For Opt. i_C-Feedback C_1 Realized Using ≈Linear Kemet KC-Link*



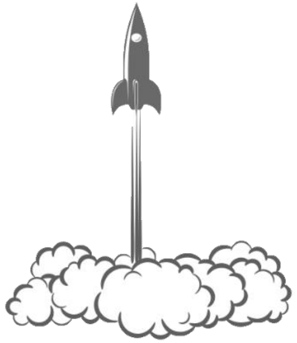






- *Modified Filter → Compliance to EMI Standard EN55011 Class-A*

X-Technology **#2**

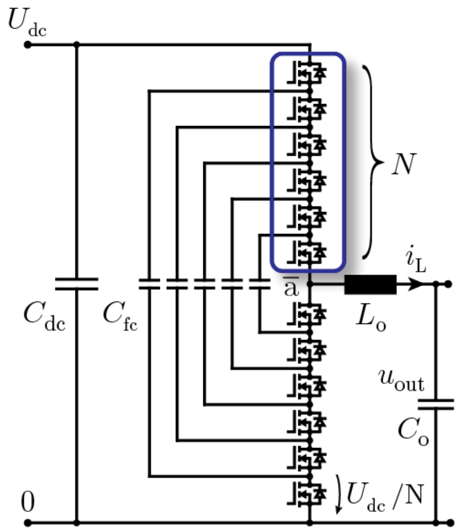


Multi-Level / -Cell
Converters & Modularity

Multi-Level (ML) Converter Scaling

- *1/N Reduction of Blocking Voltage → Lower $R_{DS,(on)}$ Semiconductors (R_{on}' ~ U_B^2)*
- *Eff. Increase of Sw. Frequency → $f_{sw,eff}$ = N f_{sw} (f_{sw} ... Individual Device)*
- *Larger Chip Area and/or Smaller L_0*

N= # of Levels -1

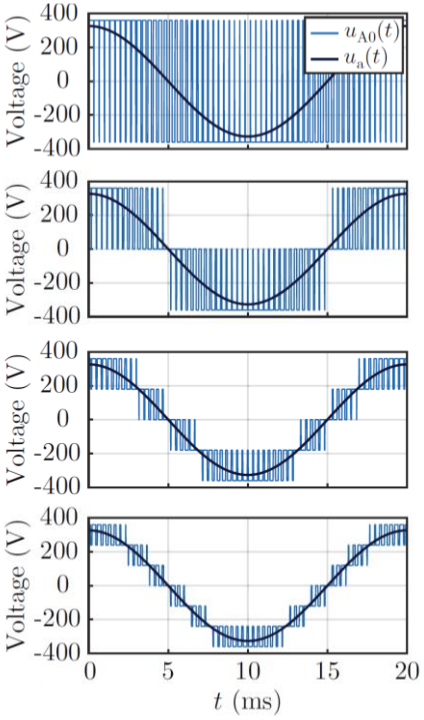


# of Levels= 2

 # = 3

 # =5

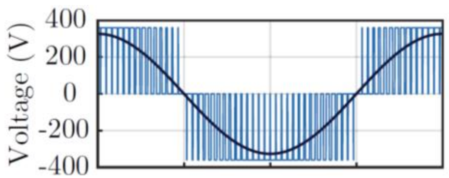
 # =7

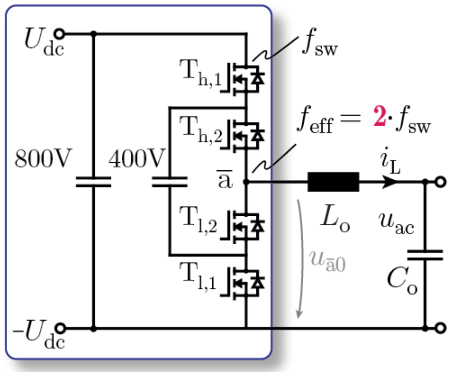


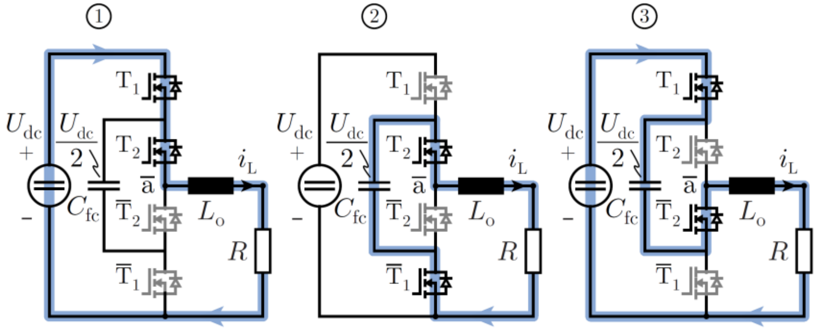
- *D-FOM = D-FOM(U_{dc}/N) → Results in ML-Performance (X-FOM) Dependent on N*

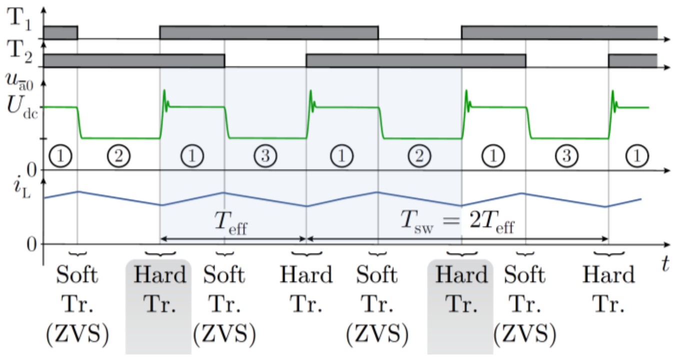
Functional Principle of ML-Converters

- *3-Level Flying Cap. (FC) Converter Requires No Connection to DC-Midpoint*
- *Involves All Switches in Voltage Generation → Eff. Doubles Device Sw. Frequency*
- *FC Voltage Balancing Possible also for DC Output*





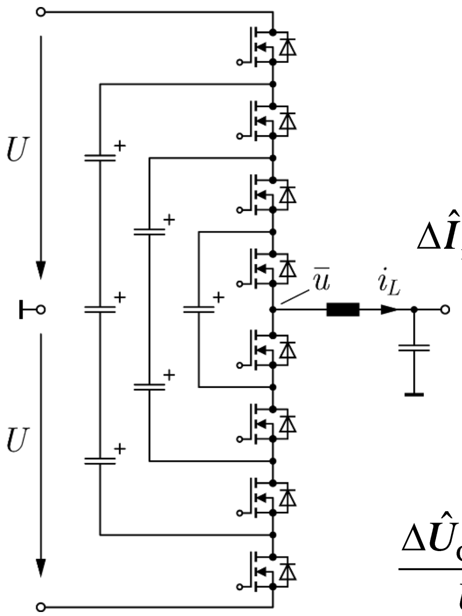




- *Risk of Transistor Overvoltage for Steep U_{dc} Changes*

Scaling of ML Bridge-Leg Concepts

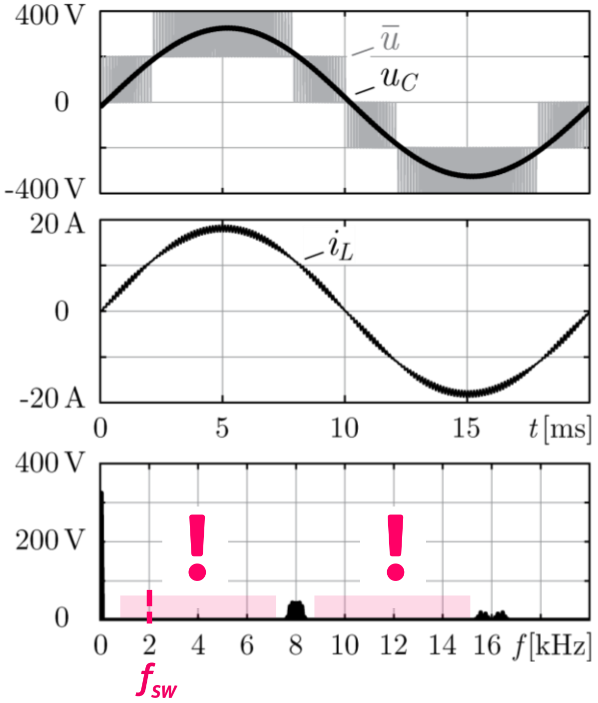
- *Reduced Ripple @ Same (!) Switching Losses*
- *Lower Overall On-Resistance @ Given Blocking Voltage → 1+1=2 NOT $2^2 = 4$ (!)*
- *Application of LV Technology to HV*



$$\frac{U}{8 f_s L}$$

$$\Delta\hat{I}_{max,N} = \frac{1}{N^2}\Delta\hat{I}_{max,N=1}$$

$$\frac{\Delta\hat{U}_{C,max,N}}{U} = \frac{\pi^2}{32}\left(\frac{f_O}{f_S}\right)^2\frac{1}{N^3}$$

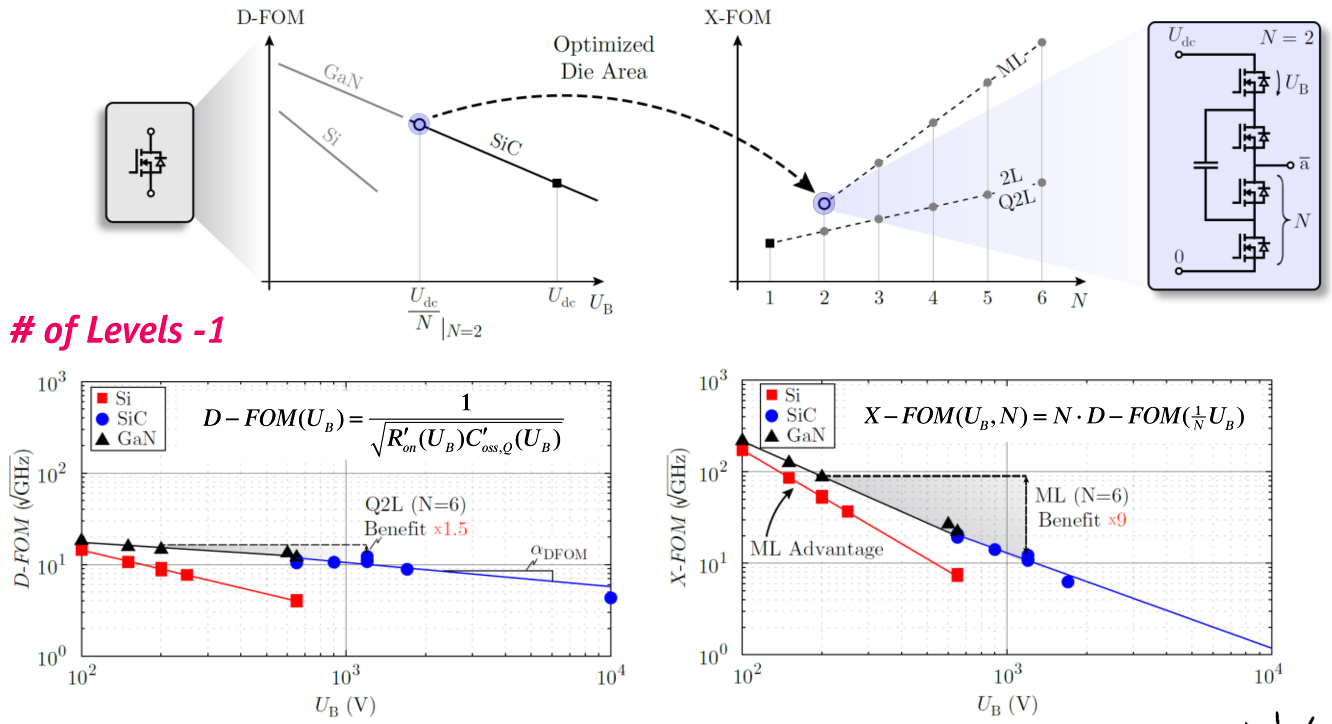


- *Scalability / Manufacturability / Standardization / Impedance Matching / Redundancy*

X-FOM of ML-Bridge-Legs

- *Quantifies Bridge-Leg Performance of N-Level FC Converters*
- *Identifies Max. Achievable Efficiency & Loss Opt. Chip Area @ Given Sw. Frequ.*

N= # of Levels -1

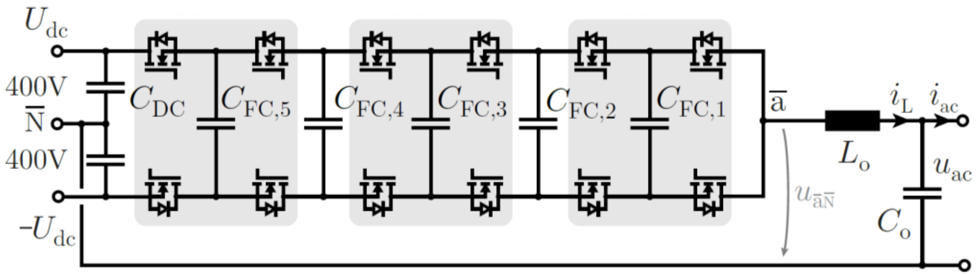


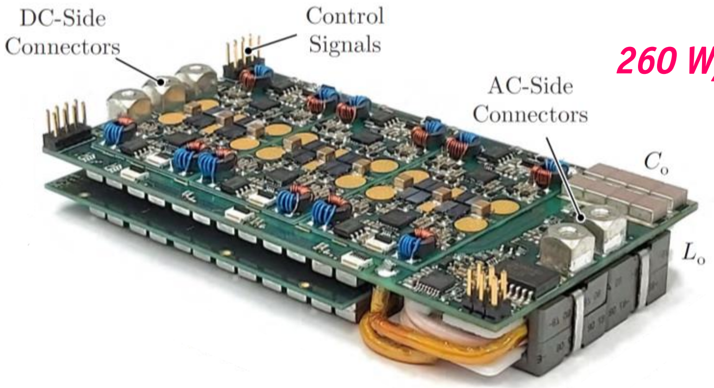
- *Compared to 2-Level Benchmark @ Same Filter Ind. Volt-Seconds* →

$P_{semi,min,ML} \approx 1/N^{1.2}\, P_{semi,min,2L}$
$A_{chip,ML} \approx N^{1.2} A_{chip,2L}$

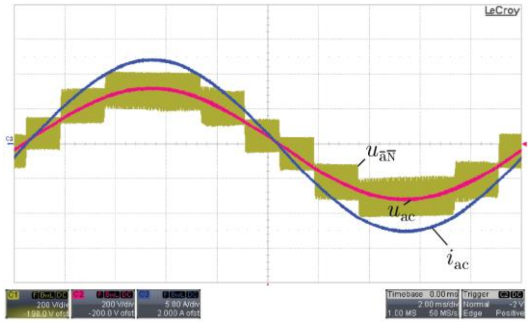
7-Level Flying Cap. 200V GaN Inverter (1)

- DC-Link Voltage 800V
- Rated Power 2.2 kW / Phase
- 99% Efficiency → Natural Convection Cooling (!)





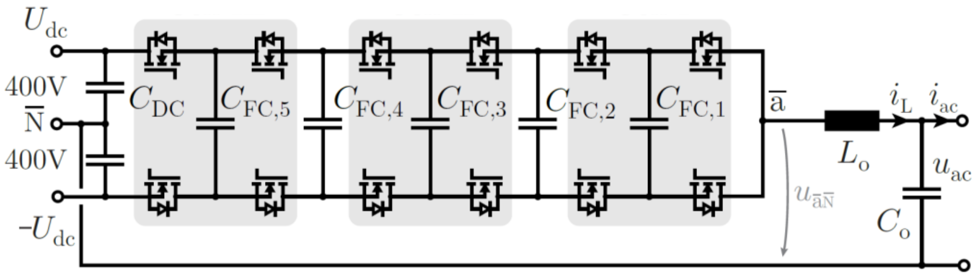
260 W/in^3



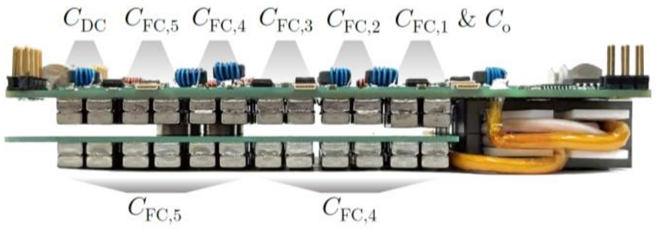
- High Effective Sw. Frequency (6 x 30kHz = 180kHz) → Small Filter Inductor L_0

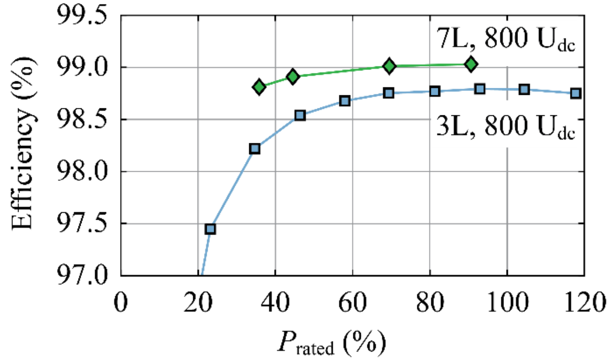
7-Level Flying Cap. 200V GaN Inverter (2)

- DC-Link Voltage 800V
- Rated Power 2.2 kW / Phase
- 99% Efficiency → Natural Convection Cooling (!)



260 W/in³

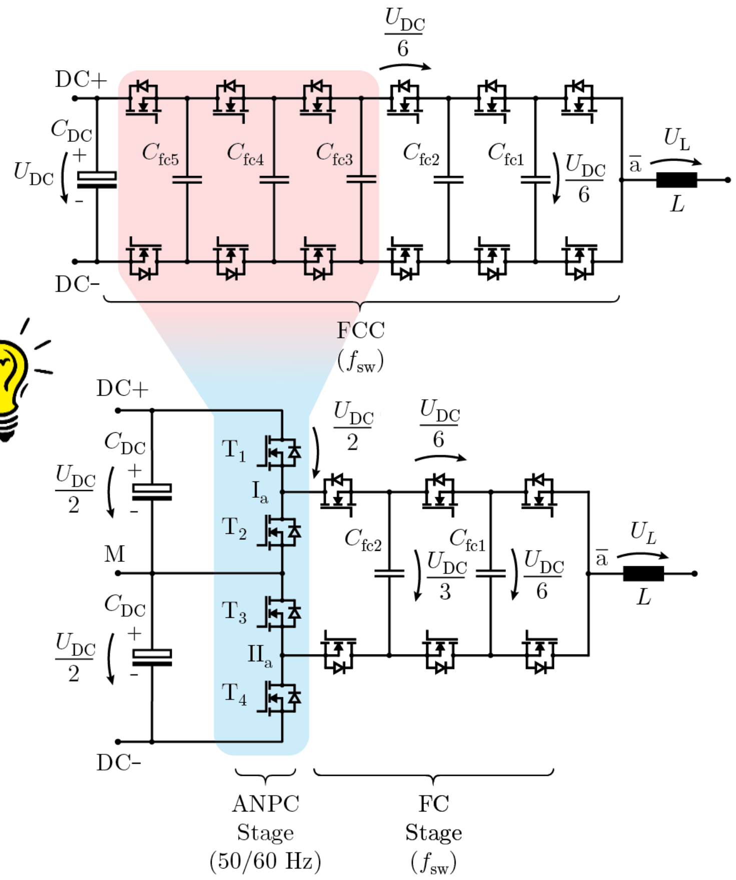


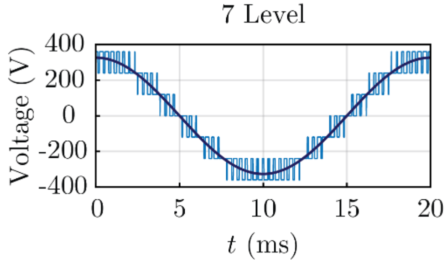


- High Effective Sw. Frequency (6 x 30kHz = 180kHz) → Small Filter Inductor L_o

3-Φ Hybrid Multi-Level Inverter Demonstrator

- *Realization of a 99%++ Efficient 10kW 3-Φ 400V$_{rms,ll}$ Inverter System*
- *7-Level Hybrid Active NPC Topology / LV Si-Technology*





99.35%
2.6kW/kg
56 W/in^3

- *200V Si → 200V GaN Technology Results in 99.5% Efficiency*

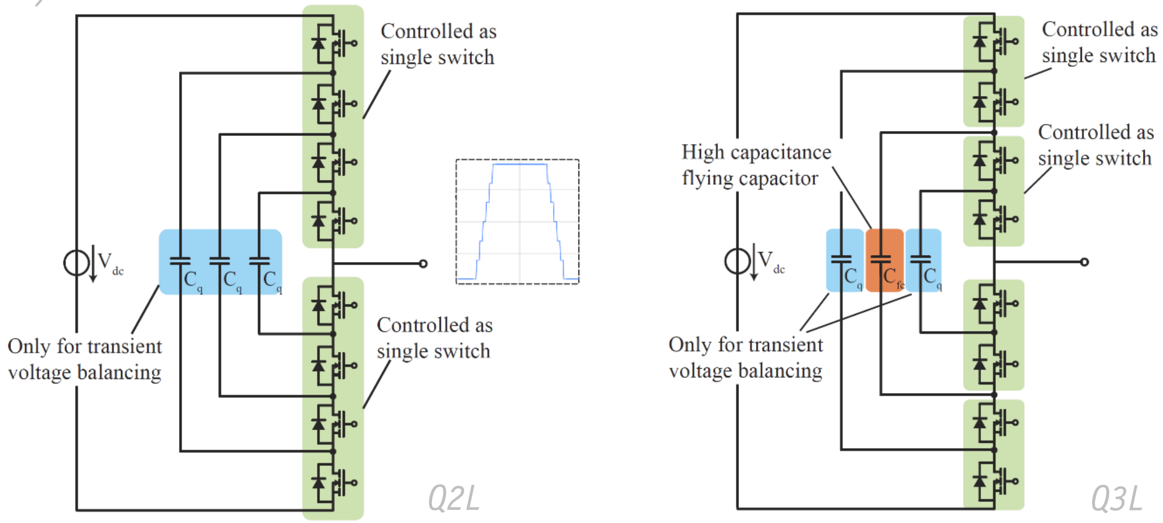
Quasi-2L/3L
Flying Capacitor Inverter

Quasi-2L & Quasi-3L Inverters (1)

- *Operation of N-Level Topology in 2-Level or 3-Level Mode*
- *Intermediate Voltage Levels Only Used During Sw. Transients*
- *Applicability to All Types of Multi-Level Converters*

- Schweizer (2017)

ABB



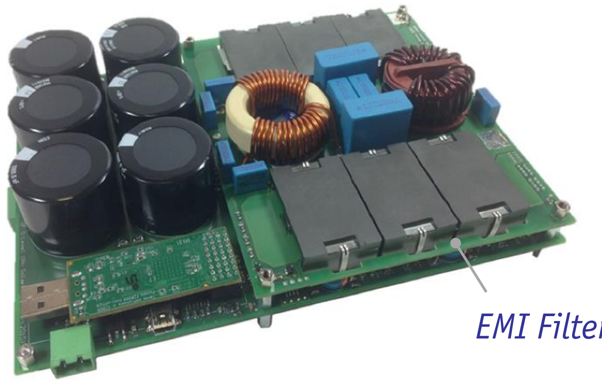
- *Reduced Average dv/dt → Lower EMI / Lower Reflection Overvoltages*
- *Clear Partitioning of Overall Blocking Voltage & Small Flying Capacitors*
- *Low Voltage/Low $R_{DS(on)}$/Low $ MOSFETs → High Efficiency / No Heatsinks / SMD Packages*

Quasi-2L & Quasi-3L Inverters (2)

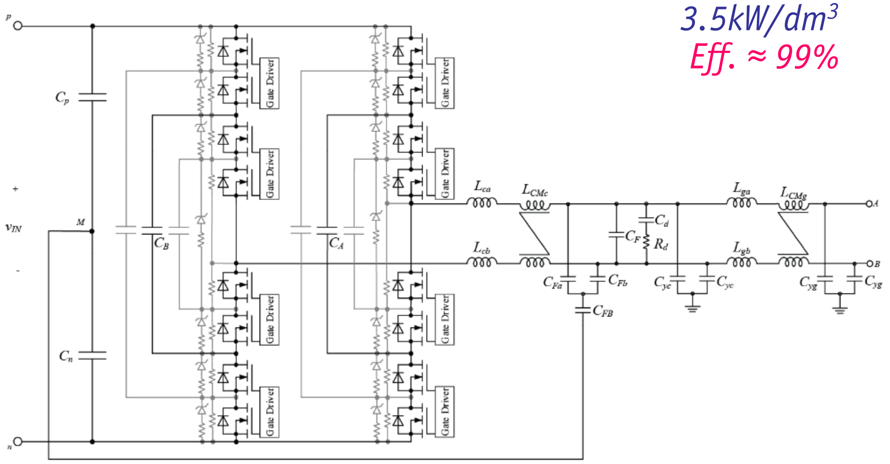
- Operation of 5L Bridge-Leg Topology in Quasi-3L Mode
- Intermediate Voltage Levels Only Used During Sw. Transients
- Applicability to All Types of Multi-Level Converters

\- Schweizer (2017)

ABB



EMI Filter



3.3kW @ 230V_{rms}/50Hz
Equiv. f_S= 48kHz

3.5kW/dm^3
Eff. ≈ 99%

- Reduced Average dv/dt → Lower EMI / Lower Reflection Overvoltages
- Clear Partitioning of Overall Blocking Voltage & Small Flying Capacitors
- Low Voltage/Low $R_{DS(on)}$/Low $ MOSFETs → High Efficiency / No Heatsinks / SMD Packages

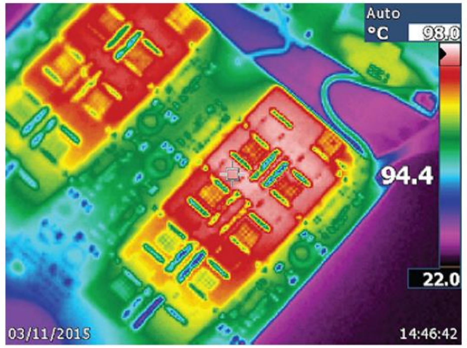
Quasi-2L & Quasi-3L Inverters (3)

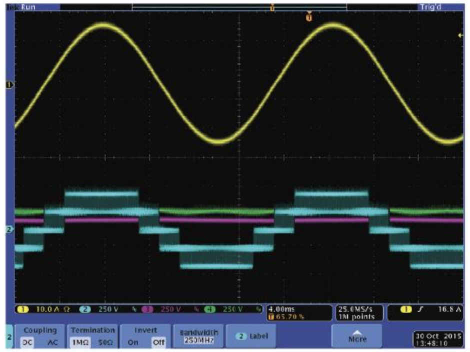
- Schweizer (2017)

ABB

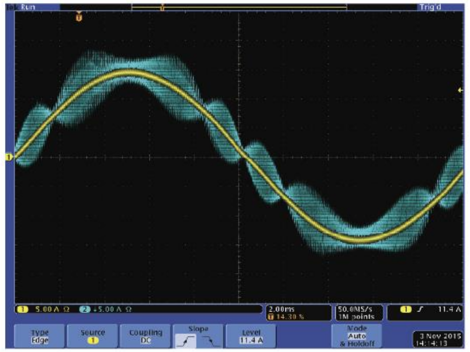
- Operation of 5L Bridge-Leg Topology in Quasi-3L Mode
- Intermediate Voltage Levels Only Used During Sw. Transients
- Applicability to All Types of Multi-Level Converters

Operation @ 3.2kW





— Conv. Output Voltage
— Sw. Stage Output Voltage
— Flying Cap. (FC) Voltage
— Q-FC Voltage (Uncntrl.)



— Output Current
— Conv. Side Current

- Reduced Average dv/dt → Lower EMI / Lower Reflection Overvoltages
- Clear Partitioning of Overall Blocking Voltage & Small Flying Capacitors
- Low Voltage/Low $R_{DS(on)}$/Low $ MOSFETs → High Efficiency / No Heatsinks / SMD Packages

Ultra-Compact
Power Module with
Integrated Filter

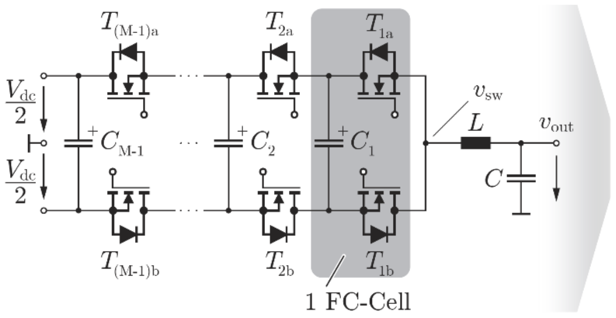
650V GaN E-HEMT Technology

$f_{S,eff} = 4.8MHz$

$f_{out} = 100kHz$

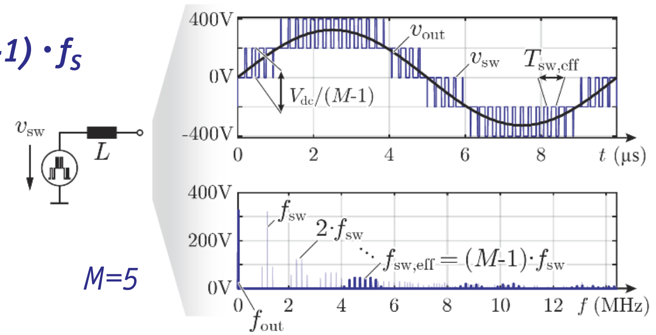
Integrated Filter GaN Half-Bridge Module

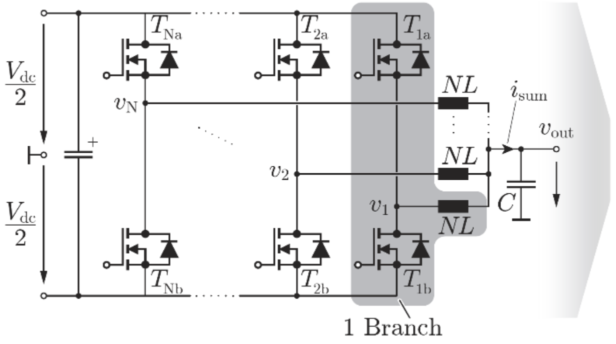
- *Minimization of Filter Volume by Series & Parallel Interleaving & Extreme Sw. Frequency*
- *Handling of DC Output Requires Flying Capacitor Approach for Series Interleaving*



$f_{S,eff} = (M-1) \cdot f_S$

$M=5$

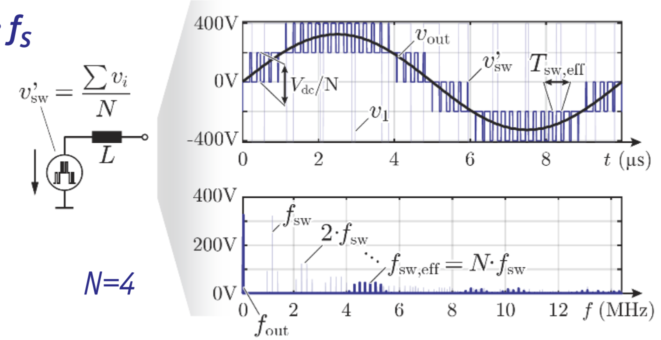




$f_{S,eff} = N \cdot f_S$

$v'_{sw} = \frac{\sum v_i}{N}$

$N=4$

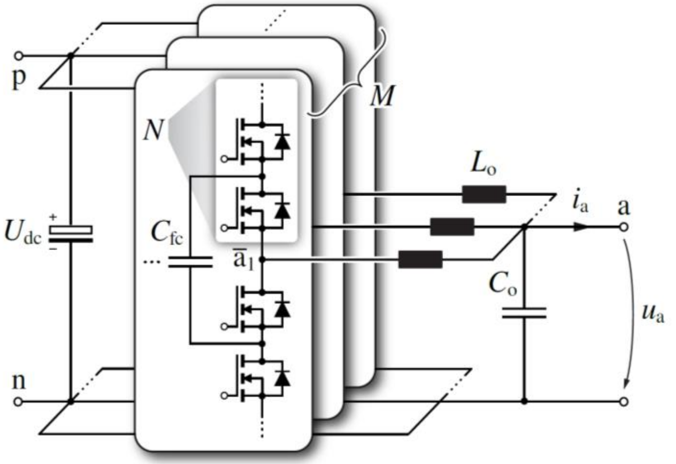


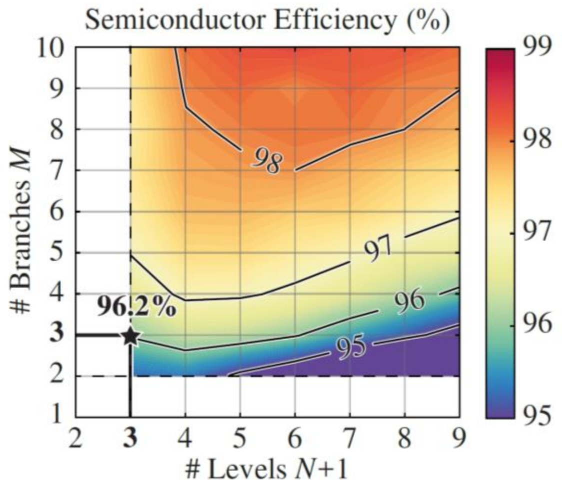
→ *Target: Best Combination of Multiple Levels (M) & Parallel Branches (N)*

4.8MHz GaN Half-Bridge Phase Module

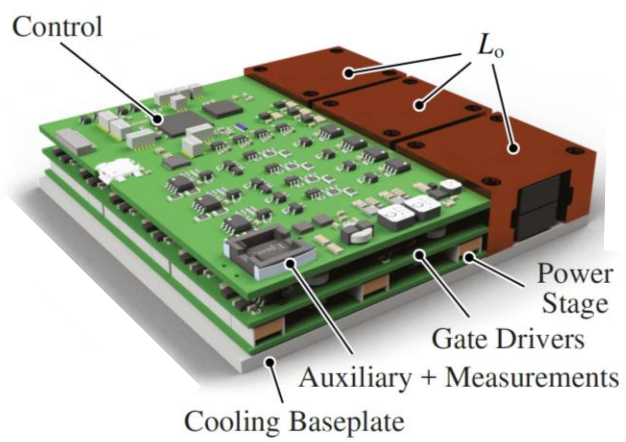
- *Combination of Series & Parallel Interleaving*

— *600V GaN Power Semiconductors, f_{sw}= 800kHz*
— *Volume of ≈180cm³ (incl. Control etc.)*
— *H_2O Cooling Through Baseplate*





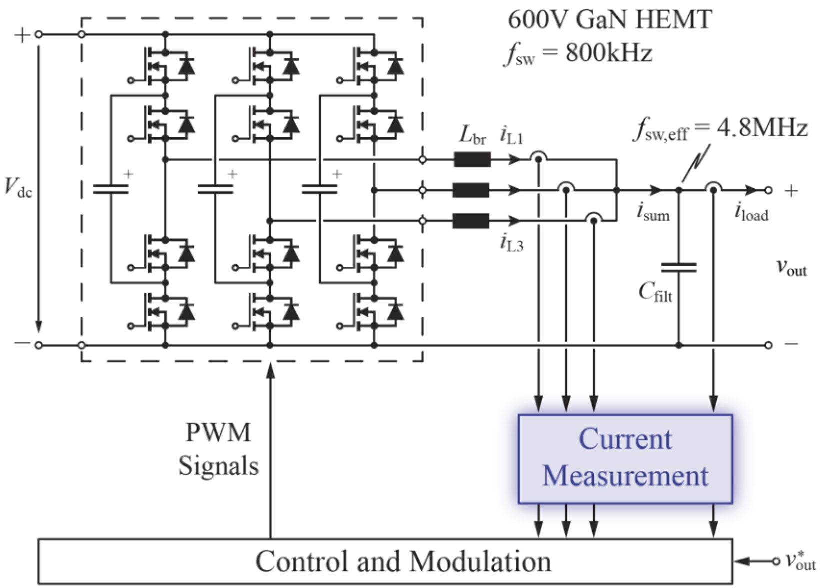
≈ 820 W/in³

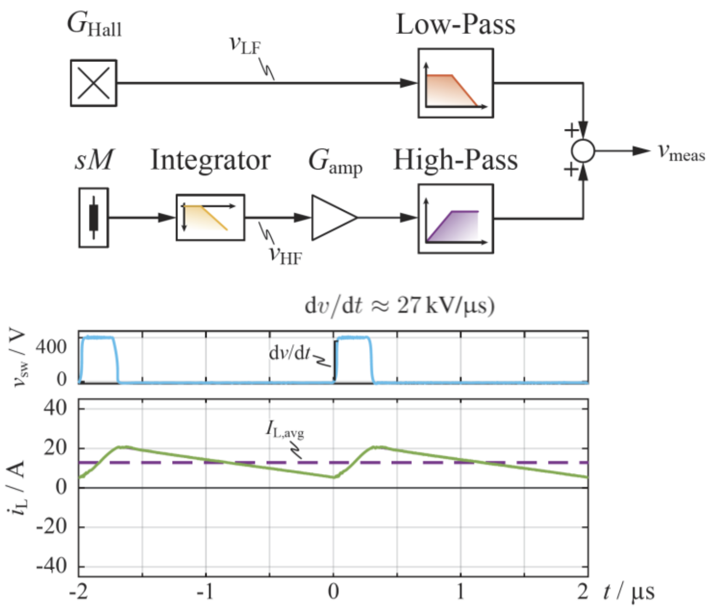


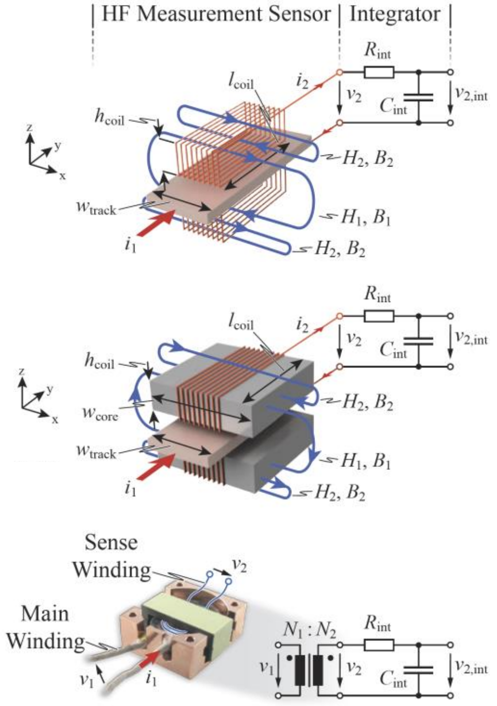
- *Operation @ f_{out}=100kHz / $f_{S,eff}$= 4.8MHz, 10kW, U_{dc}=800V*

Remark High-BW High-CMRR Current Measurement

- Extension of Commercial Hall Sensor DC… f_{Hall}≈ 500kHz → DC…20MHz
- Low-Pass & High-Pass Filter Network Combining HF-Sensor & LF Hall-Sensor







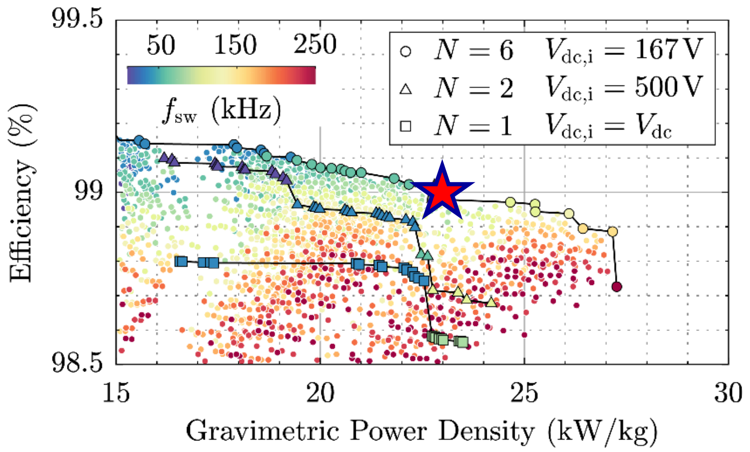
- Hall Sensor Bandwidth f_{Hall} = 1.6MHz
- Rogowski Coil High-Pass Corner Frequency f_{int}=1kHz
- Low/High-Pass Filter Cross-Over Network f_{filter} = 24kHz

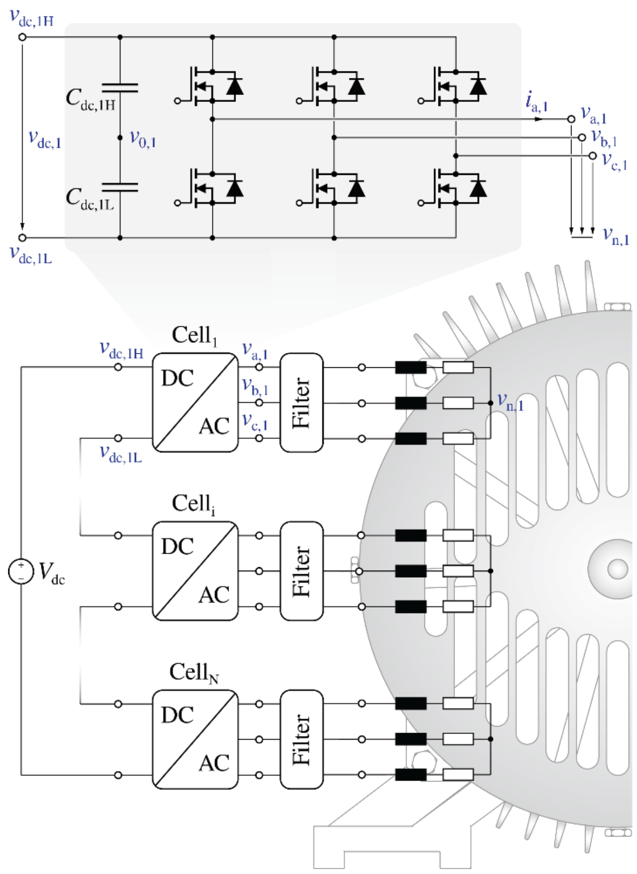
Motor-Integrated Inverter Systems

Stacked-Multi-Cell (SMC) Inverter

- *Fault-Tolerant VSD*
- *Low-Voltage Inverter Modules*
- *Very-High Efficiency / Power Density*
- *Automated Manufacturing*

- *Rated Power* *45kW / f_{out} = 2kHz*
- *DC-Link Voltage* *1 kV*

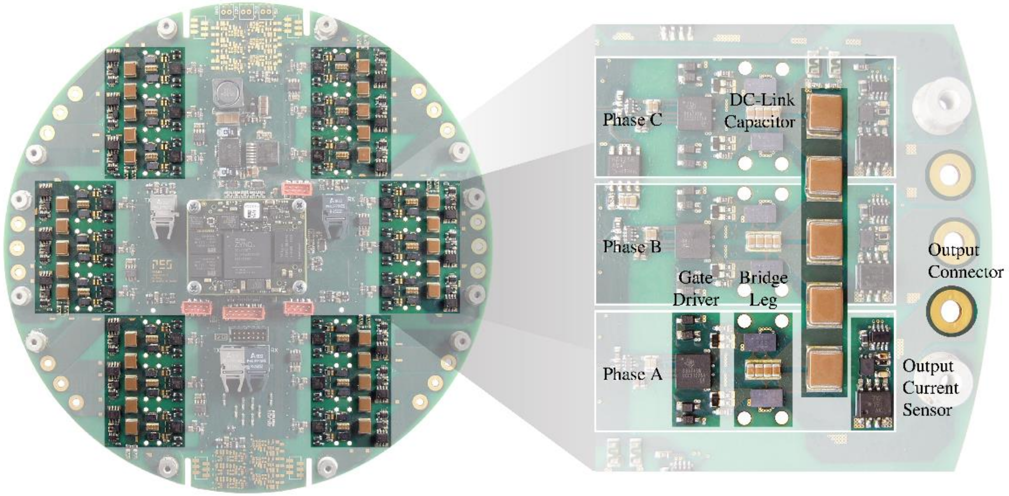




- *Smart Motor / Plug & Play* | *Connected / Intelligent VSD 4.0*

Motor-Integrated SMC 200V GaN-Inverter

- *Rated Power* *9kW @ 3700rpm*
- *DC-Link Voltage* *650V...720V*
- *3-Φ Power Cells* *5+1*
- *Outer Diameter* *220mm*

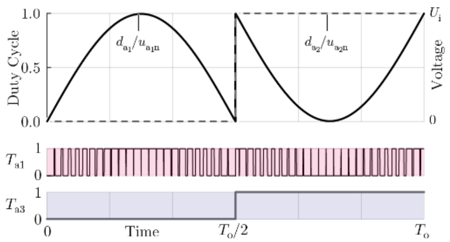


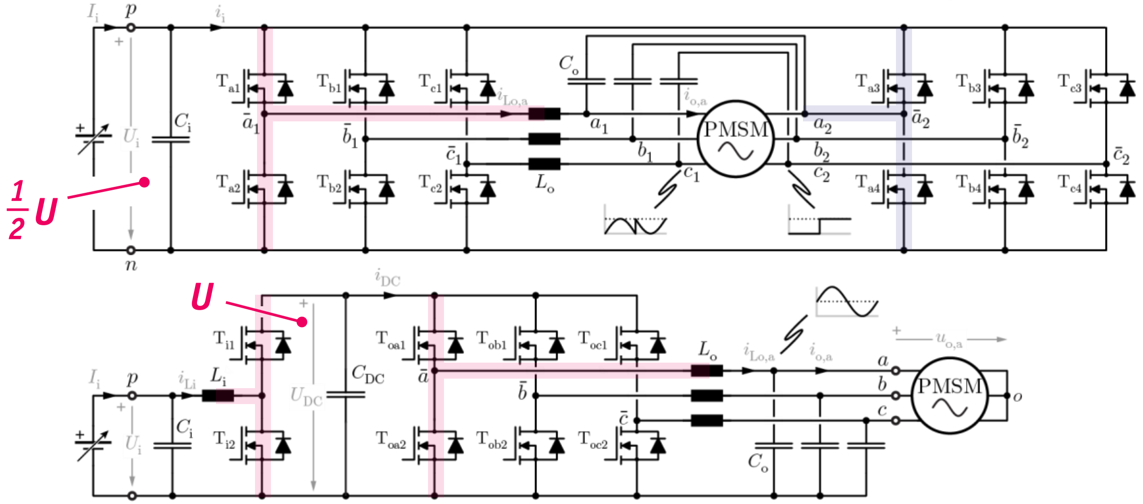
— *Axial Stator Mount*
— *200V GaN e-FETs*
— *Low-Capacitance DC-Links*
— *45mm x 58mm / Cell*

- *Main Challenge — Thermal Coupling/Decoupling of Motor & Inverter*

Double-Bridge (DB) Inverter

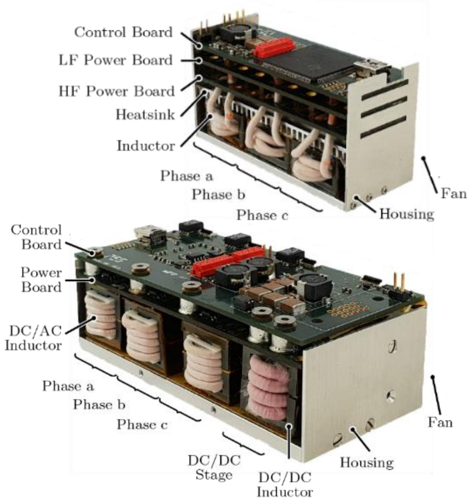
- *Comparison to Conv. 2-Level Inverter + Front-End DC/DC Boost-Stage*





U_b = 40V...120V
P = 1.0kW
f_s = 300kHz (200V EPC GaN)
f_o = 5kHz

210 W/in³

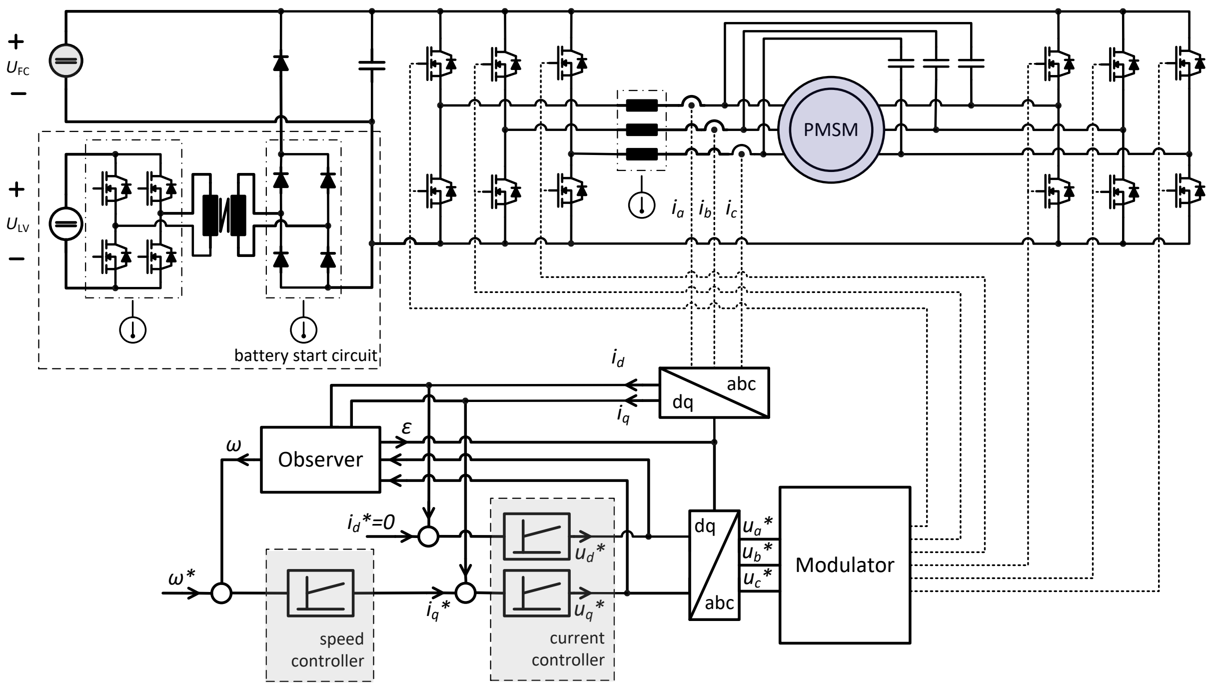


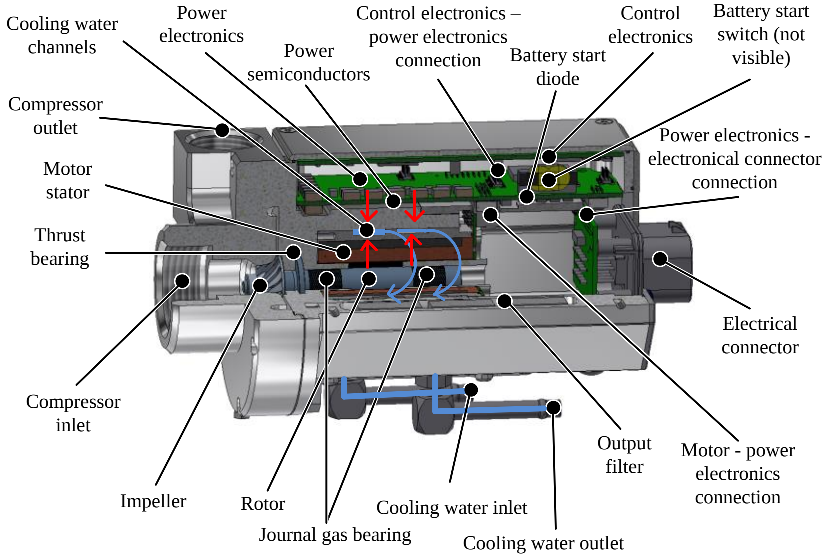
98 W/in³

- *Advantages — Lower Sw. Losses & Lower # of Filter Inductors*

Turbo-Compressor-Integrated DB GaN-Inverter

- *E-Mobility 5...15kW Fuel Cell Pressurized Air Supply*
- *1kW Rated Power, f_{sw}=300kHz | n= 280‘000rpm / f_{out}= 4.6kHz*
- *Low EMI / Low Cabling Effort*



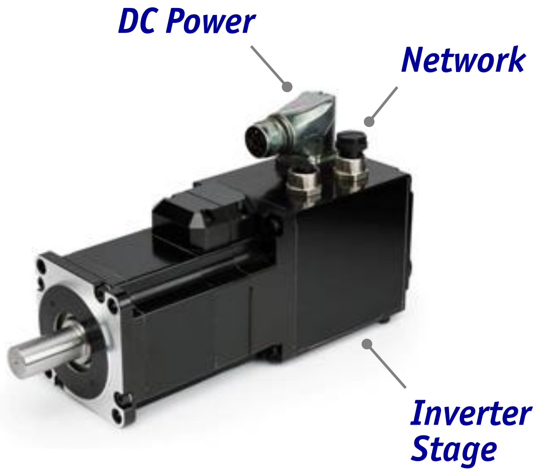


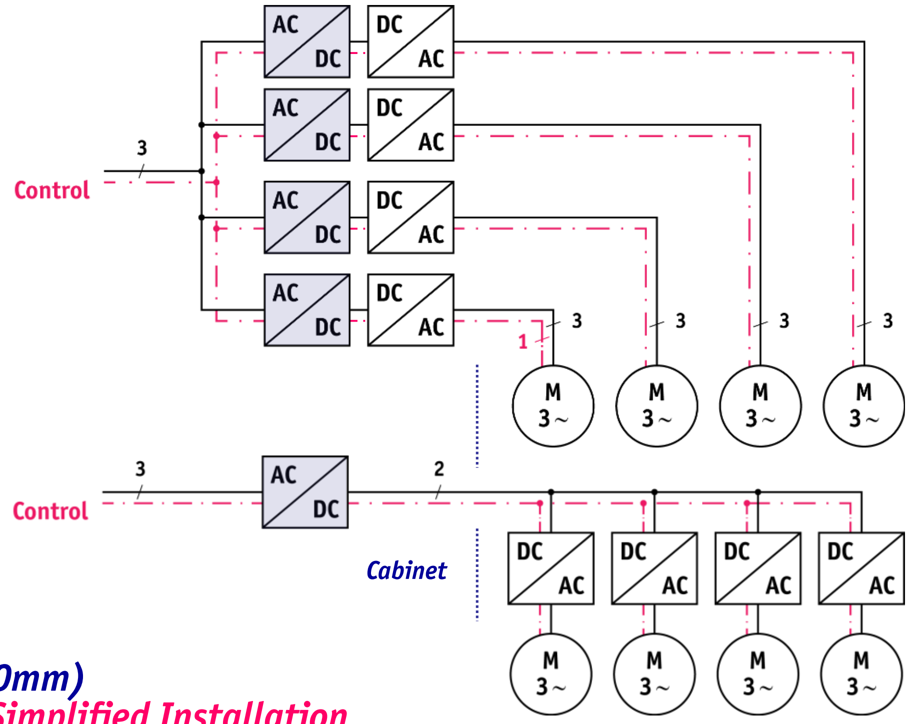
- *Integration → 2x System Power Density | 97% → 98.5% Inverter Efficiency*

3-Φ 650V GaN Motor-Integrated Inverter

Source: YASKAWA

- *Sigma-7F Servo Drive — Motor Integration of DC/AC Stage (TO-220 GaN)*
- *Distributed DC-Link System — Single AC/DC Converter / Smaller Cabinet*
- *0.1 – 0.4kW / 270...324V Nominal DC-Link Voltage*



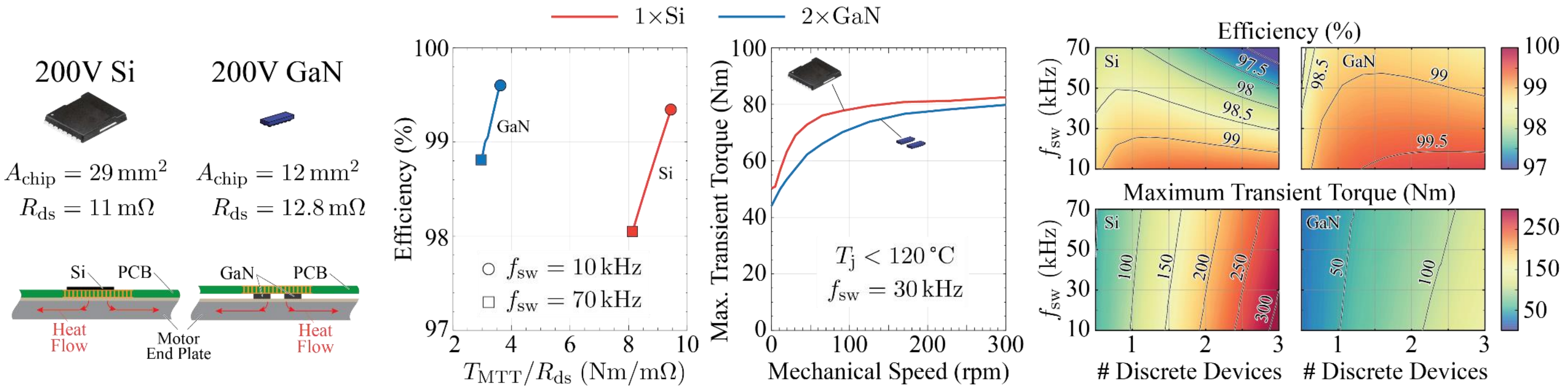


- *Small Size (0.4 kW @ 70 x 70x 170mm)*
- *Massive Saving in Cabling Effort / Simplified Installation*

Overload | Thermal Limit

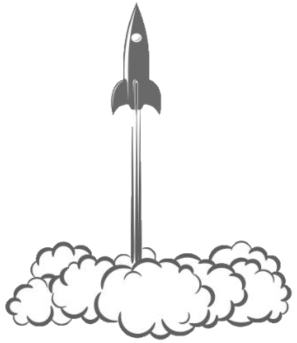
Remark Overload Capability

- Highly Dynamic Robotics VSDs → 3x ... 5x Rated Torque for Seconds
- Small Chip Area → Low Thermal Time Constant of GaN HEMTs
- Trade-Off Between Overload Rating & Rated Power Efficiency



- 200V GaN vs. Si (Multi-Level Inverter) Comparison

X-Technology #3

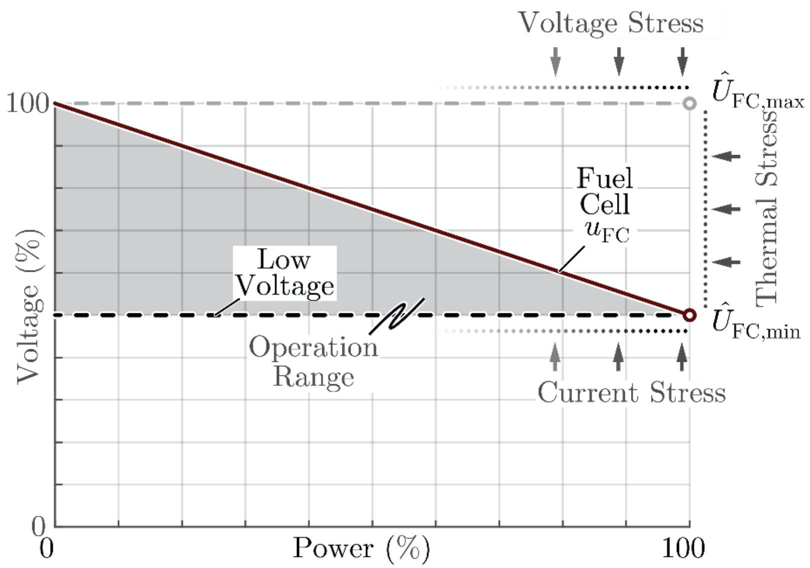


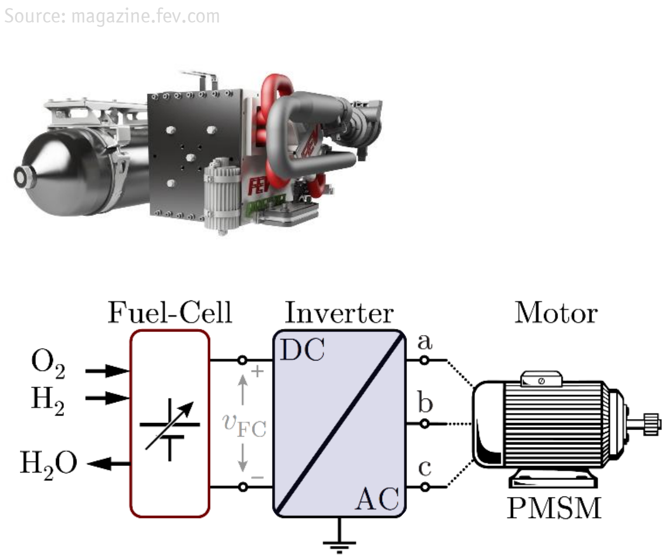
Functional Integration & Synergetic Association

Motivation

■ *General / Wide Applicability*

— *Adaption of (Load-Dependent) Supply Voltage & Motor Voltage*
— *Wide Speed Range → Wide Output Voltage Range*



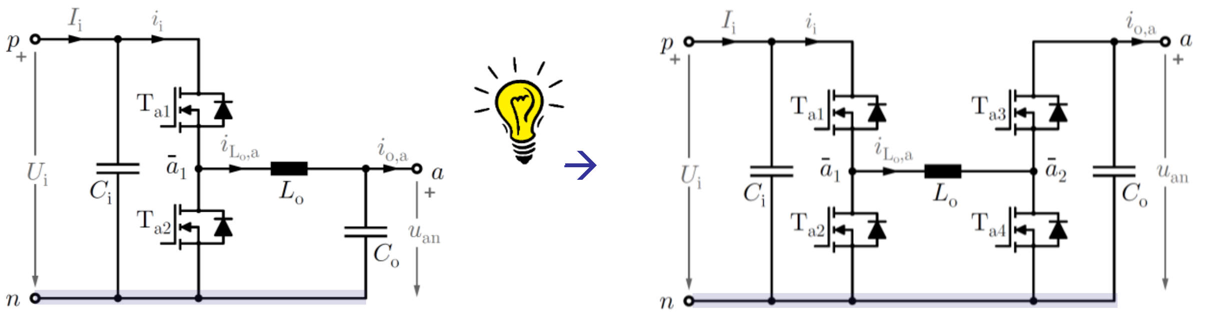


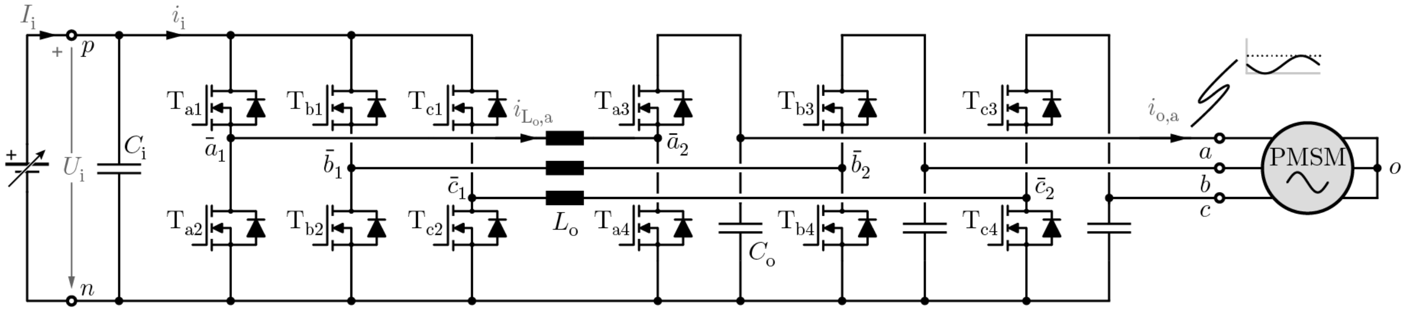
● *No Add. Converter for Voltage Adaption → Single-Stage Energy Conversion*

***Buck-Boost
Y-Inverter***

Derivation of Buck-Boost Y-Inverter

■ *Generation of AC-Voltages Using Unipolar Bridge-Legs*

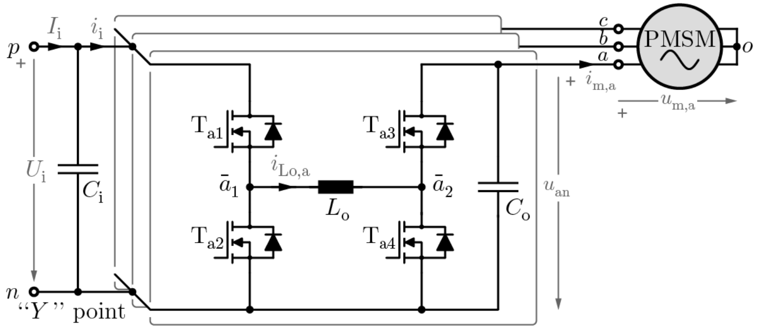




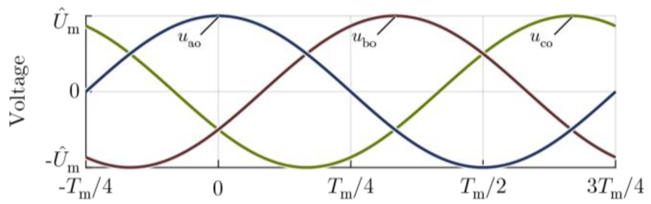
- *Switch-Mode Operation of Buck OR Boost Stage* → *Single-Stage Energy Conversion (!)*
- 3-Φ Continuous Sinusoidal Output / Low EMI → *No Shielded Cables / No Insul. Stress*
- Standard Bridge-Legs / Building Blocks → *1.2kV SiC MOSFETs*

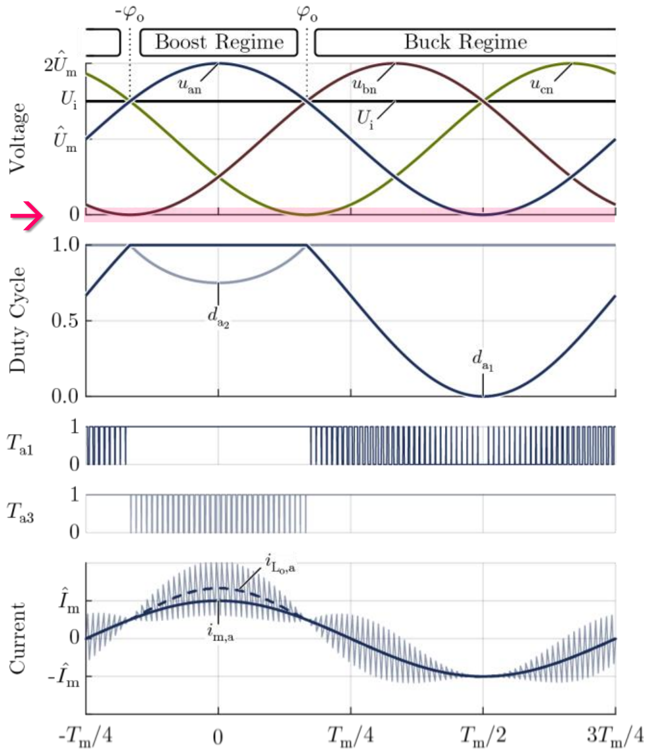
Sinusoidal Modulation

- *Y-Inverter*



- *Motor Phase Voltages*

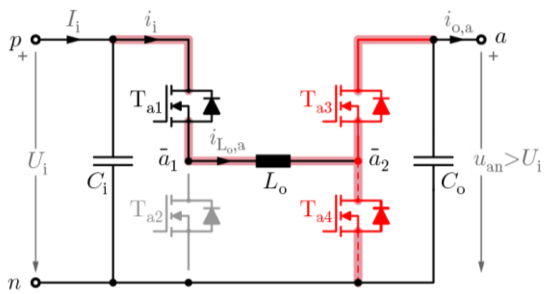




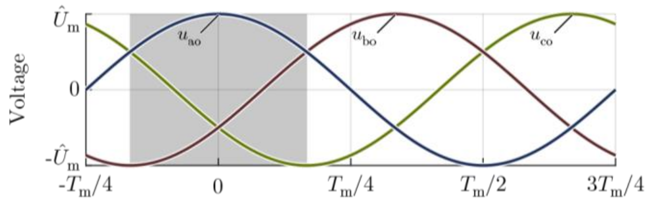
- *Const. DC Offset → Strictly Positive Output Voltages u_{aN}, u_{bN}, u_{cN}*
- *Mutually Exclusive Operation of the Half-Bridges → Low Switching Losses*

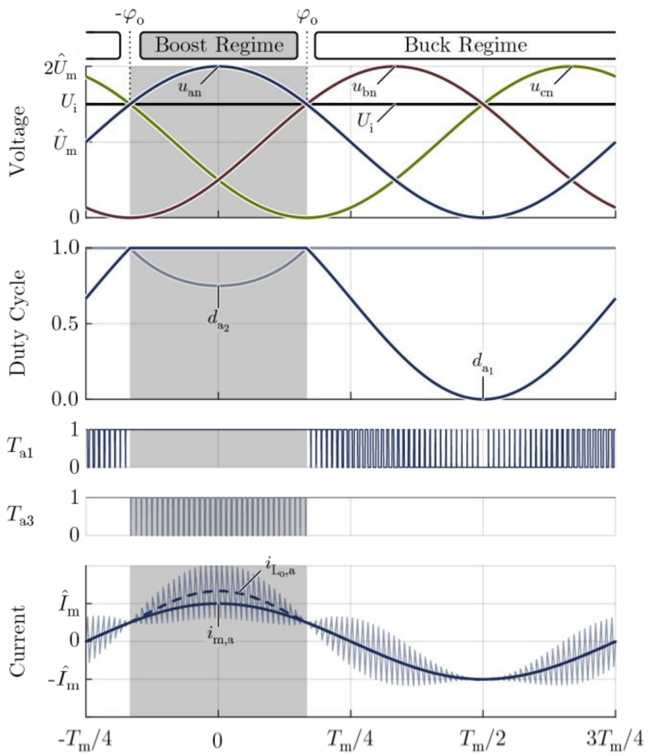
Boost-Operation $u_{an} > U_i$

- **Phase-Module**



- **Motor Phase Voltages**

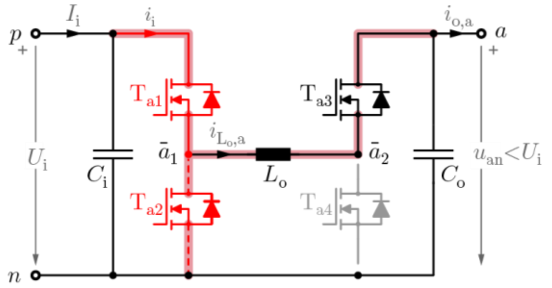




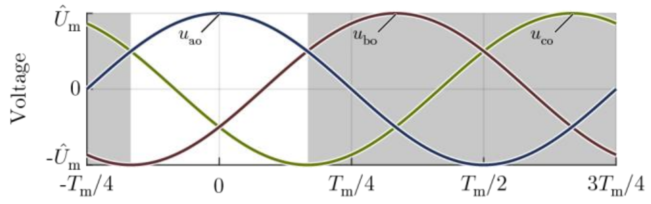
- *Current-Source-Type Operation*
- *Clamping of Buck-Bridge High-Side Switch → Quasi Single-Stage Energy Conversion*

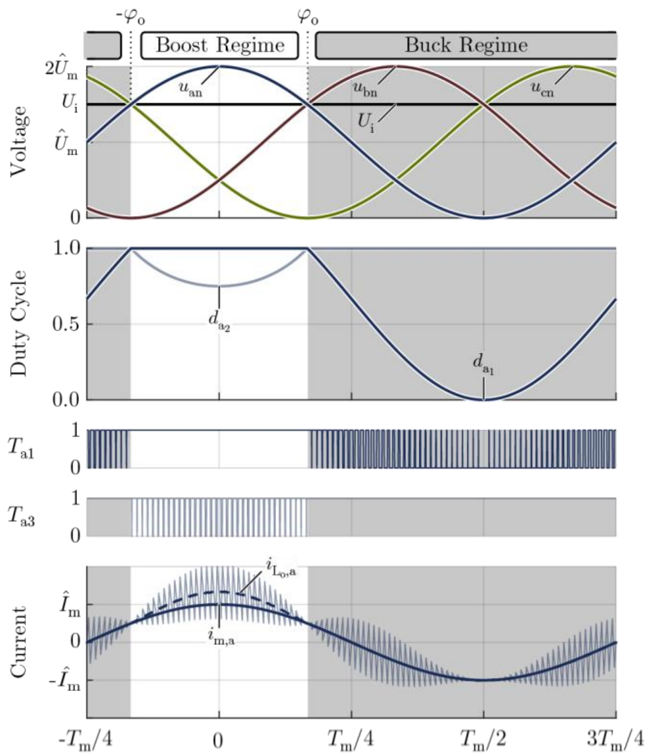
Buck-Operation $u_{an} < U_i$

■ ***Phase-Module***



■ ***Motor Phase Voltages***

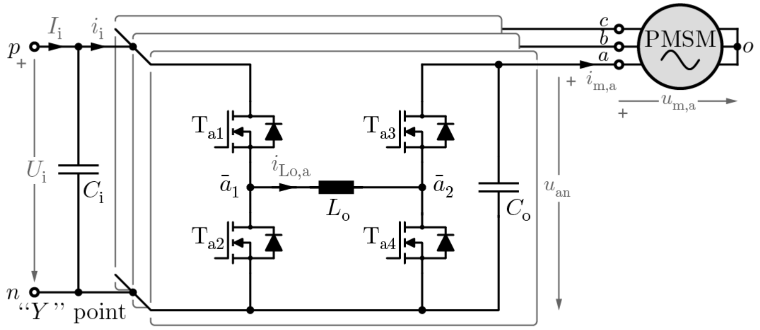




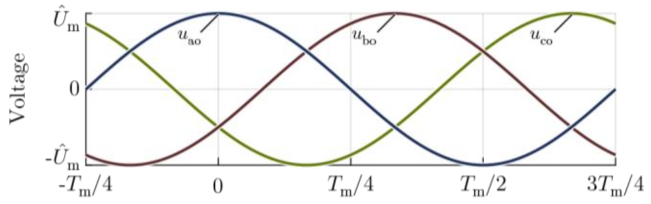
- *Voltage-Source-Type Operation*
- *Clamping of Boost-Bridge High-Side Switch → Quasi Single-Stage Energy Conversion*

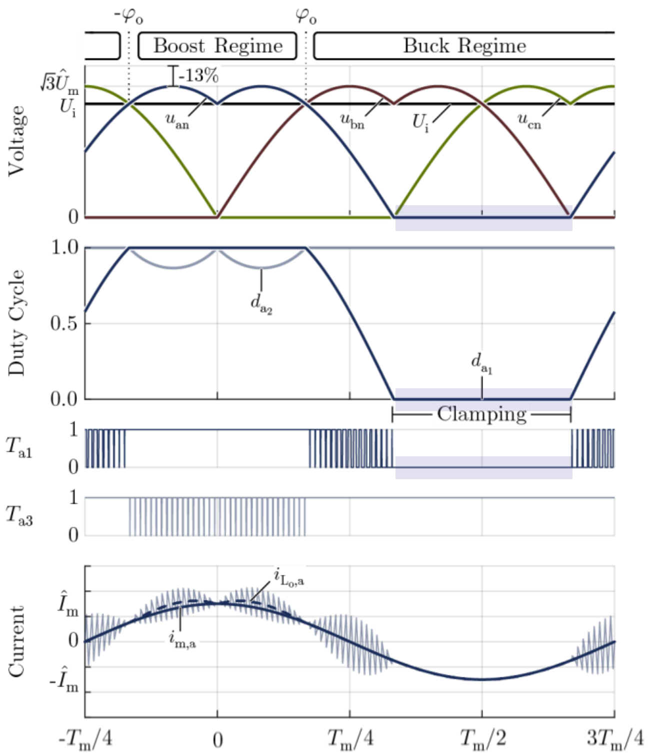
Discontinuous Modulation

- *Y-Inverter*



- *Motor Phase Voltages*

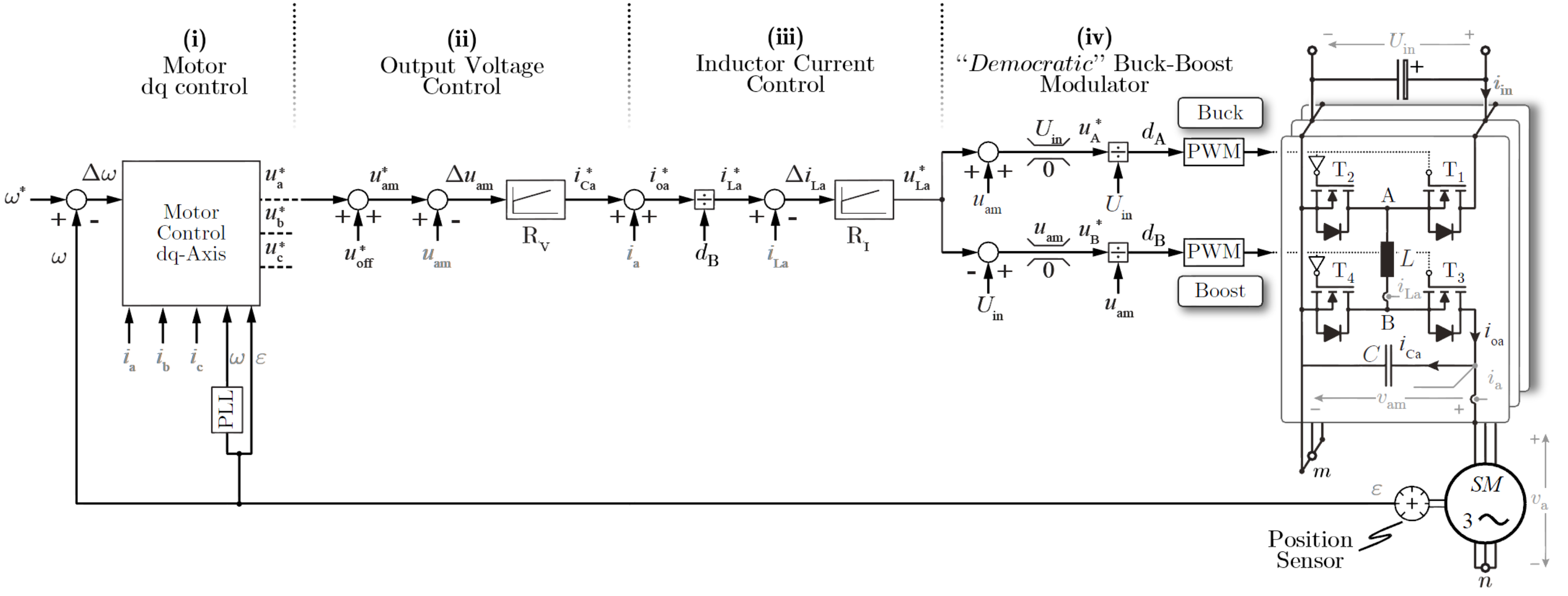




- *Clamping of Each Phase for 1/3 of the Fund. Period → Low Switching Losses (!)*
- *Non-Sinusoidal Module Output Voltages / Sinusoidal Line-to-Line Voltages*

Control Structure

- *Motor Speed Control*

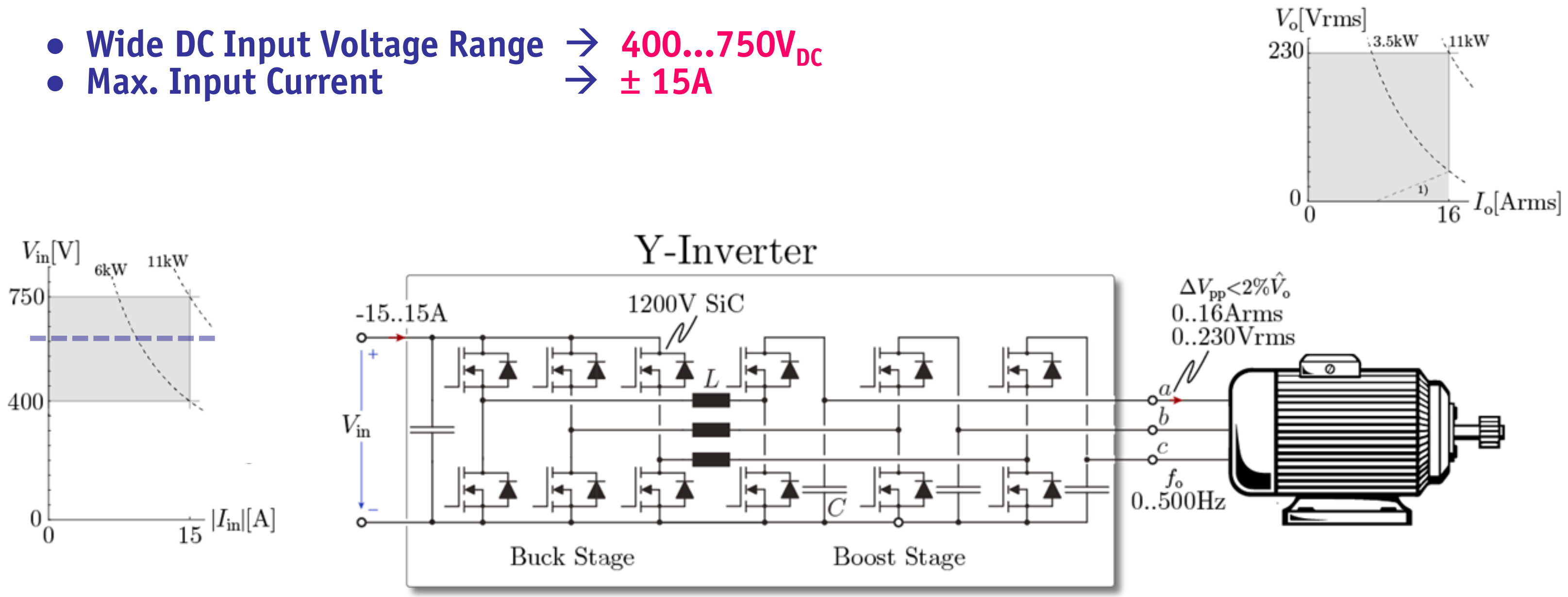


- *Cascaded Current / Voltage / Current Control Loops*
- *Seamless Transition between Boost- & Buck-Mode → "Democratic" Control*

Y-Inverter VSD

■ *Demonstrator Specifications*

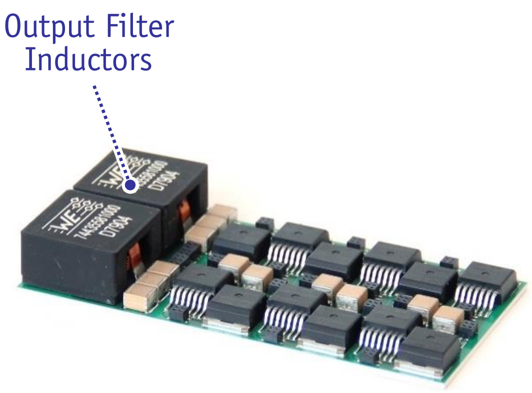
- Wide DC Input Voltage Range → 400...750V_{DC}
- Max. Input Current → ± 15A

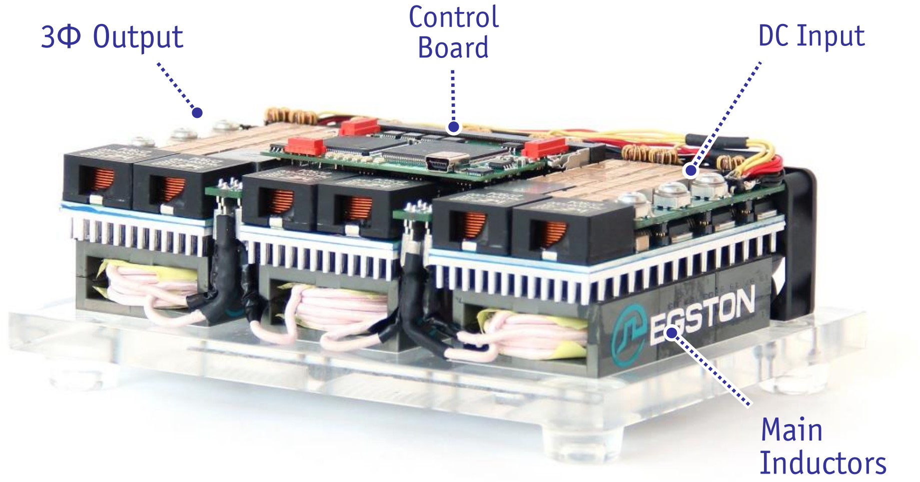


- Max. Output Power → 6...11 kW
- Output Frequency Range → 0...500Hz
- Output Voltage Ripple → 3.2V Peak @ Output of Add. LC-Filter

Y-Inverter Demonstrator

- DC Voltage Range 400...750V_{DC}
- Max. Input Current ± 15A
- Output Voltage 0...230V_{rms} (Phase)
- Output Frequency 0...500Hz
- Sw. Frequency 100kHz
- 3x SiC (75mΩ)/1200V per Switch
- IMS Carrying Buck/Boost-Stage Transistors & Comm. Caps & 2nd Filter Ind.





- Dimensions → 160 x 110 x 42 mm^3 (245W/in^3)

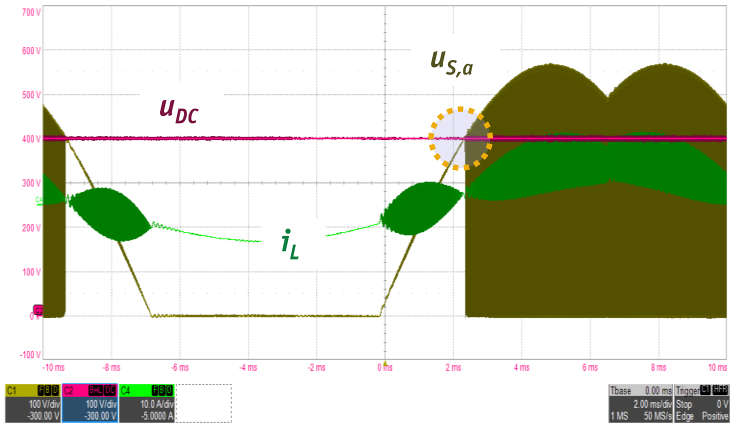
Y-Inverter - Measurement Results

■ *Stationary Operation*

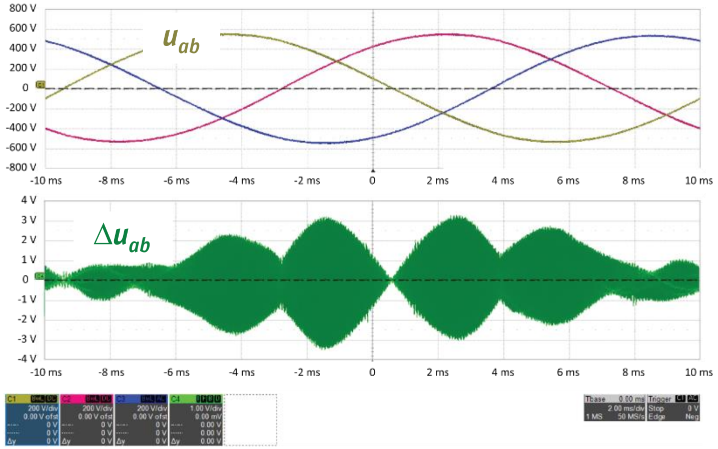
U_{DC} = 400V
U_{AC} = $400V_{rms}$ (Motor Line-to-Line Voltage)
f_O = 50Hz
f_S = 100kHz / *Discontinuous PWM*

P = 6.5kW

100V/div
10A/div



200V/div
1V/div

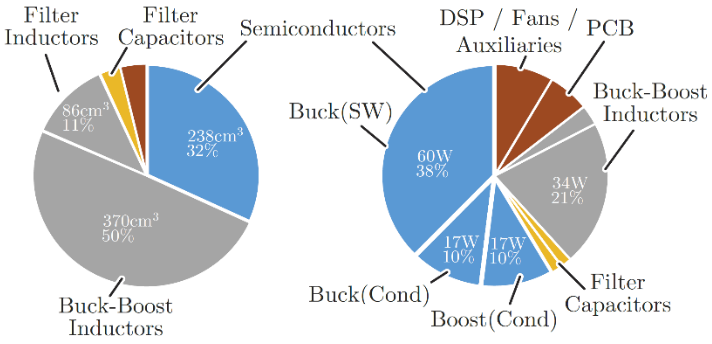


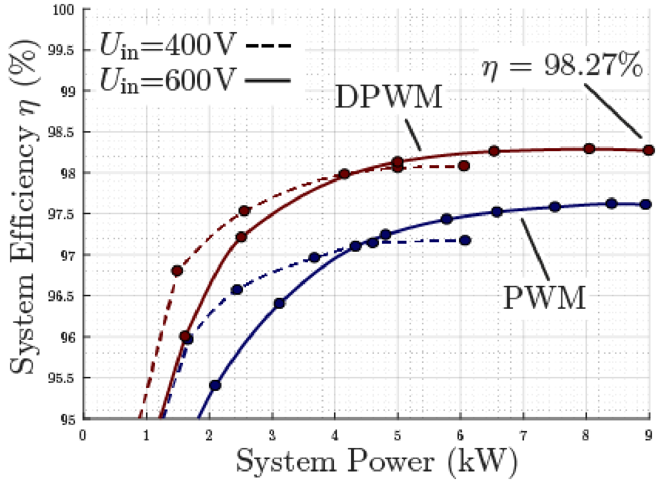
● *Line-to-Line Output Voltage Ripple < 3.2V*

Efficiency Measurements

- *Dependency on Input Voltage & Output Power Level*

U_{DC}= 400V / 600V
U_{AC}= 230V_{rms} (Motor Phase-Voltage)
f_S = 100kHz

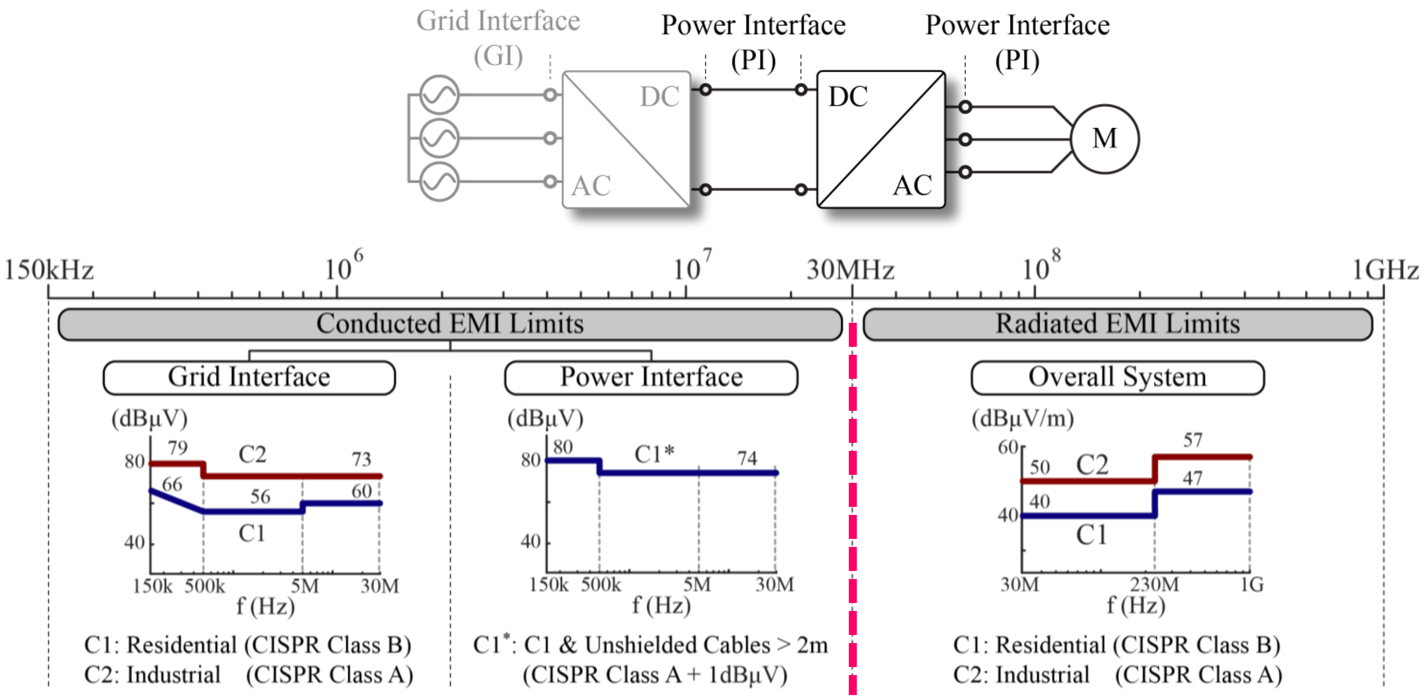




→ *Multi-Level Bridge-Leg Structure for Increase of Power Density @ Same Efficiency*

EMI-Limits (VSD Product Standard)

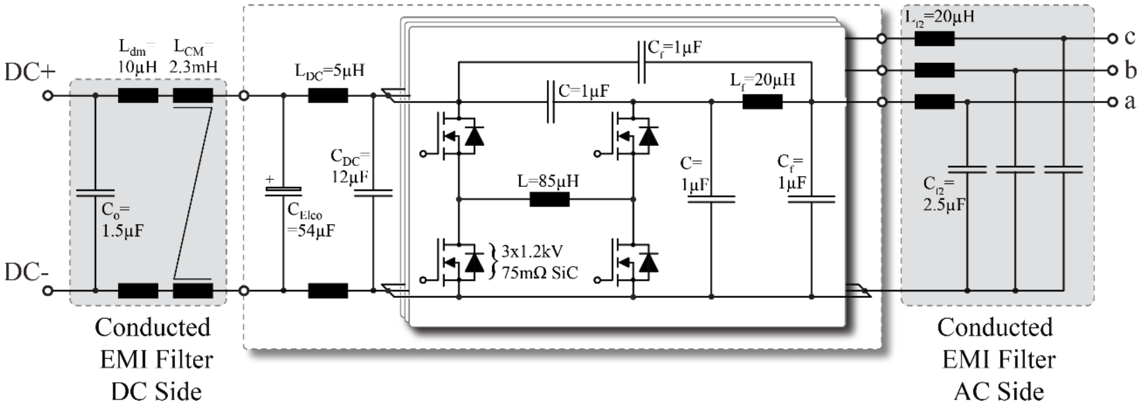
- **IEC 61800-3** → **Product Standard for Variable-Speed Motor Drives**
- **EMI Emission Limits** → **Grid Interface (GI) and Power Interface (PI)**
- **Application** → **Residential (C1) or Industrial (C2)**

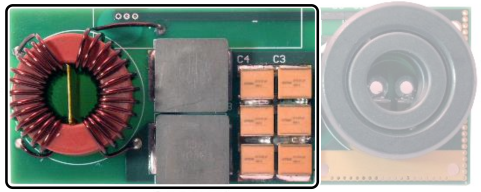


- *EMI-Filter Design for Unshielded Cables > 2m and Resid. Applications (Cond. & Rad.)*

Conducted EMI-Filter

- Separate Cond. DM & CM EMI-Filter on DC-Side & DC-Minus Ref. EMI-Filter on AC-Side





L_{CM} L_{DM} $C_{DM} = C_0$

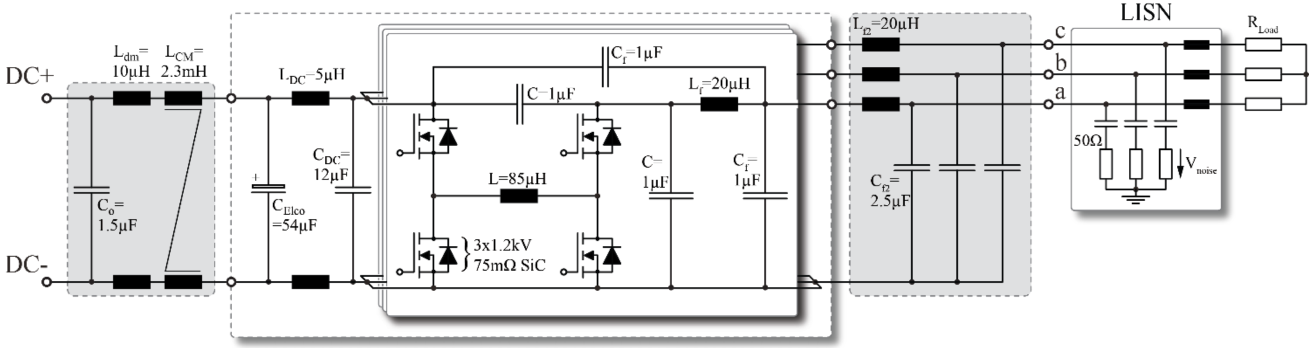
C_{f2} (on the back)

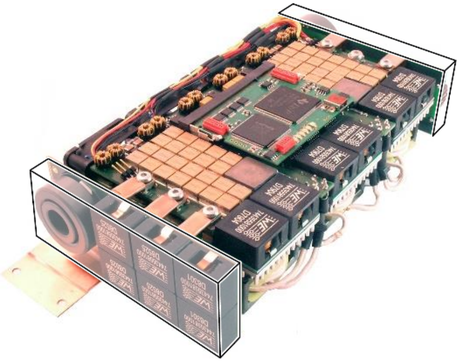
L_{f2}

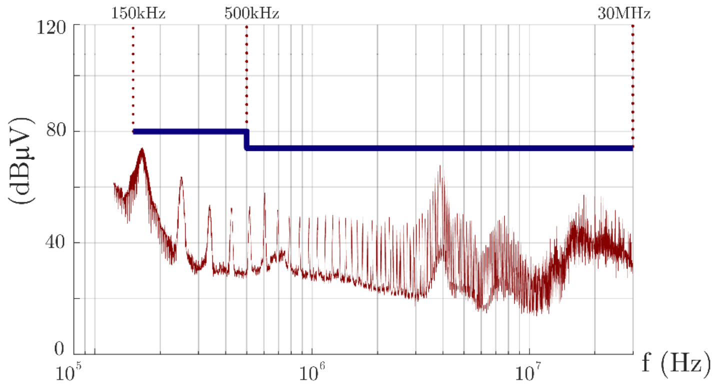
→ Low Add. EMI Filter Volume — 74cm³ for Each Filter (incl. Toroid. Rad. EMI Filter)
→ Total Power Density Reduces — 15kW/dm³ (740cm³) → 12kW/dm³ (890cm³)

Conducted EMI - Experimental Results

- Measurements of the Cond. EMI Noise on the AC-Side (QP, with 50Hz AC-LISN)



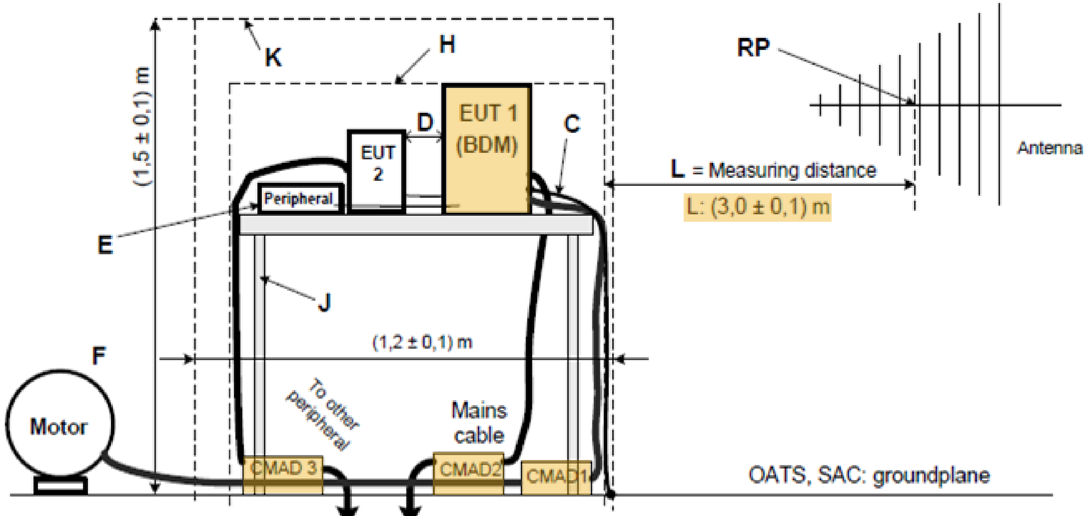




→ *Small 80uH CM-Ind. Added on AC-Side - (3cm³ of Add. Volume = 0.5% of Converter Vol.)*
→ *Conducted EMI with Unshielded Motor Cable Fulfilled*

Measurement of Radiated EMI-Noise (1)

- Equipment Under Test (EUT) Placed on Wooden Table with Specified Arrangement
- CM Absorption Devices (CMAD) Terminate All Cables on AC- & DC-Side (Total $l_{cable} \approx 1.5$m)
- Measurement of Radiated Noise with Antenna in 3m Distance



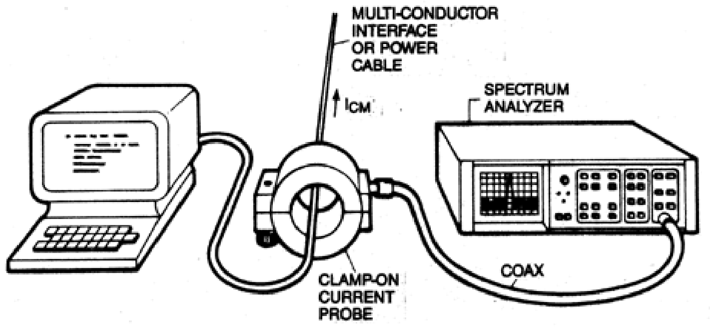
[IEC 61800-3]

[Schwarzbeck]

- *Either Open-Area Test Site (OATS) or Special Semi-Anechoic Chamber (SAC) Needed*
- *Alternative Pre-Compliance Measurement Method*

Measurement of Radiated EMI-Noise (2)

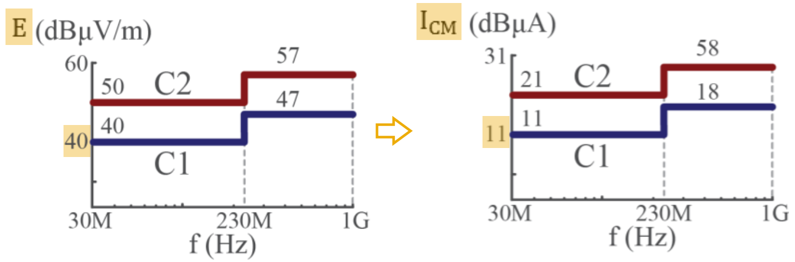
- CM-Currents NOT Returning IN THE CABLE are Dominant Source of Radiation
- Relation Between Radiated Electric Field and CM-Currents (!)



$$E = \begin{cases} \dfrac{\mu_0 \cdot f \cdot l_{cable} \cdot I_{cm}}{r} & \dfrac{\lambda}{4} \leq l_{cable} \\ \dfrac{\mu_0 \cdot \frac{c_0}{4} \cdot I_{cm}}{r} & \dfrac{\lambda}{4} > l_{cable} \end{cases}$$

[Electromagnetic Compatibility Engineering, H. Ott]

[Fischer FCC F-33-1]
up to 250MHz
$Z_{nom} = 6.3\Omega$

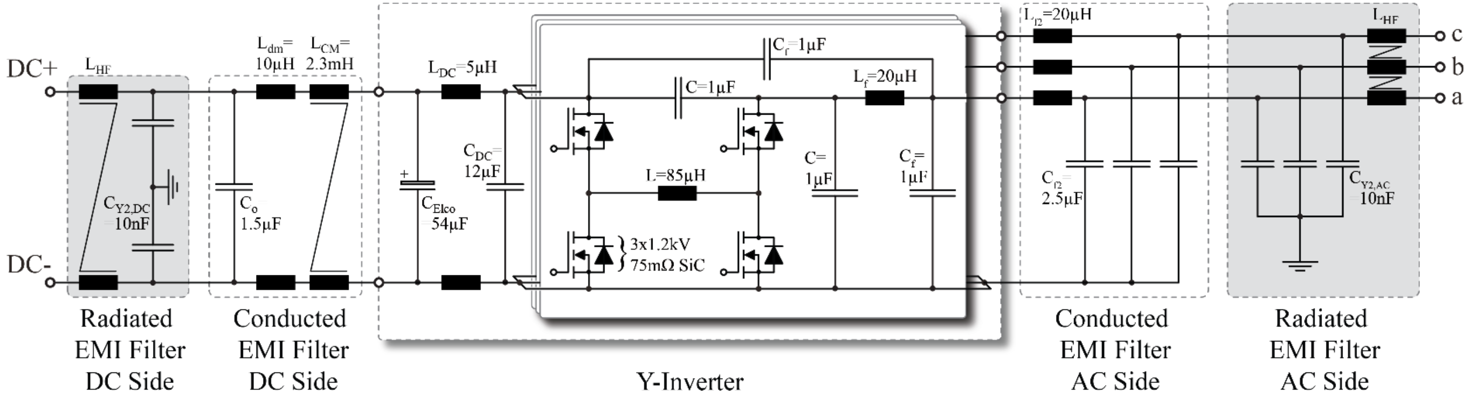


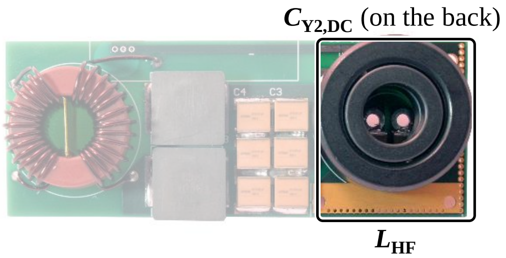
C1: Residential (CISPR Class B)
C2: Industrial (CISPR Class A)

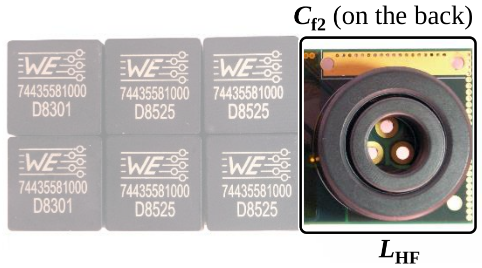
- *Max. Allow. El. Field Strength of 40dBuV/m → Max. CM-Current of 3.5uA (11dBuA)*
- *Current Probe Impedance of 6.3Ω (F-33-1) → Max. Noise Volt. of 26dBuV @ Test Receiver*

Radiated EMI-Filter Design

- Single-Stage HF CM-Filter on DC-Side and AC-Side
- Plug-On CM-Cores (NiZn-Ferrites) → Low Parasitics & Good HF-Att. up to 1GHz



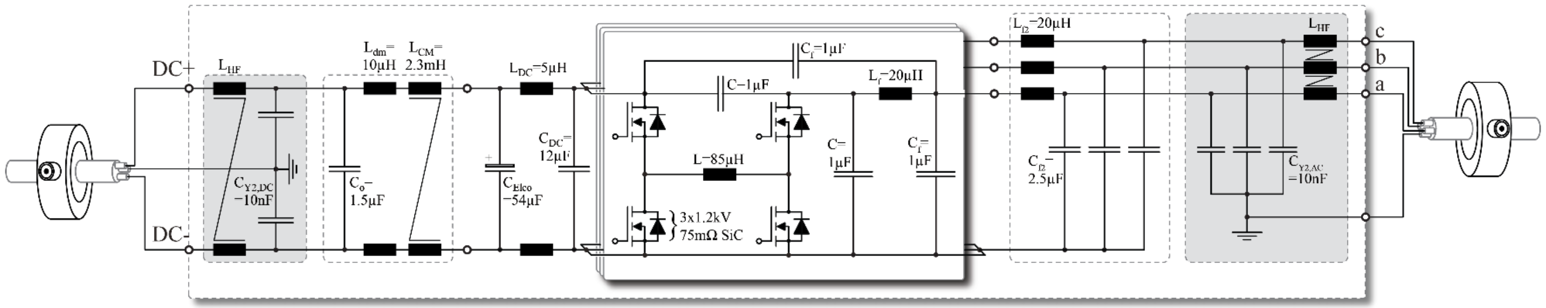


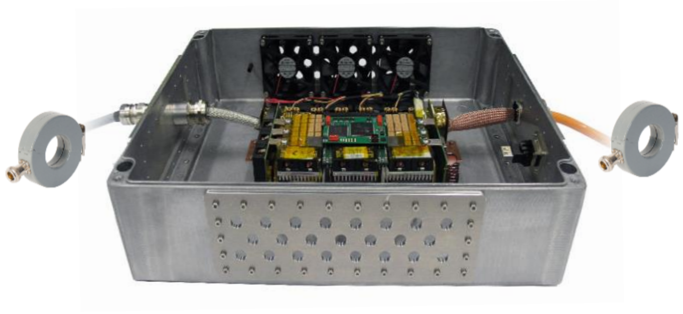


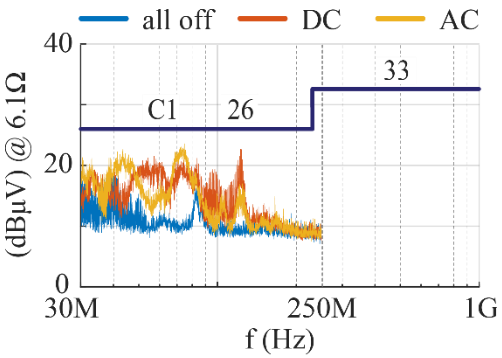
→ *Additional EMI Filter Volume Already Considered with Conducted EMI Filter*
→ *Total Power Density Slightly Reduces — 15kW/dm³ → 12kW/dm³*

Experimental Results - Radiated EMI

- Y-Inverter Placed in Metallic Enclosure → Emulate Housing, but UNshielded Cables (!)
- Measurement Setup → According IEC 61800-3
- Alternative Measurement Principle → Conducted CM-Current Instead of Radiation



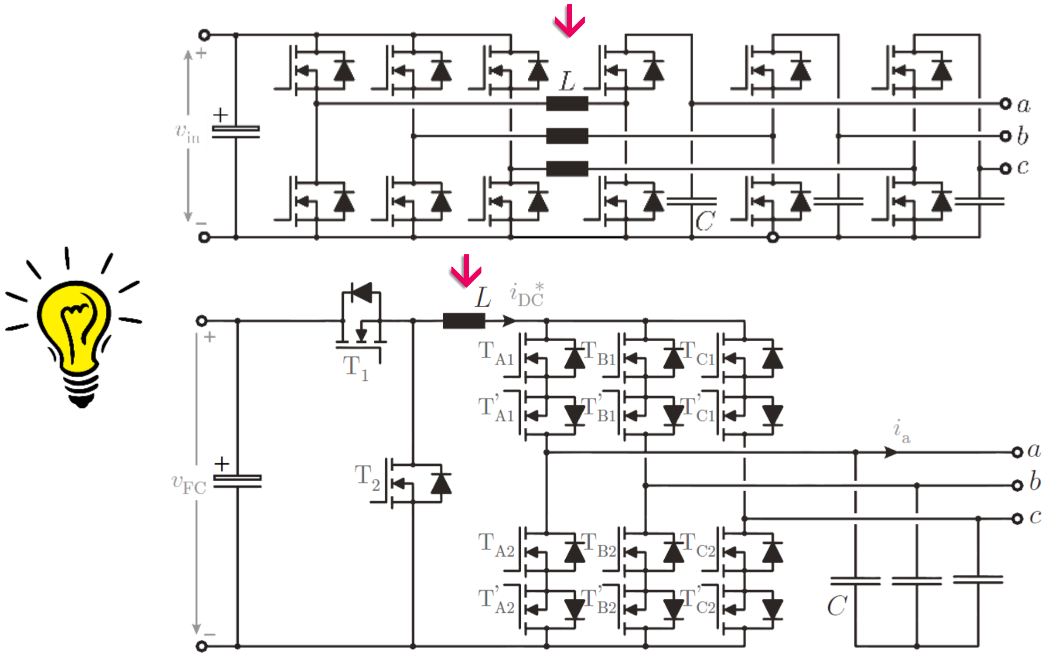




→ *Already Noticeable Noise Floor*
→ *HF-Emissions Well Below Equivalent EMI-Limit* → ***Next Step:*** *Verification Using Antenna*

Current Source Inverter (CSI) Topologies

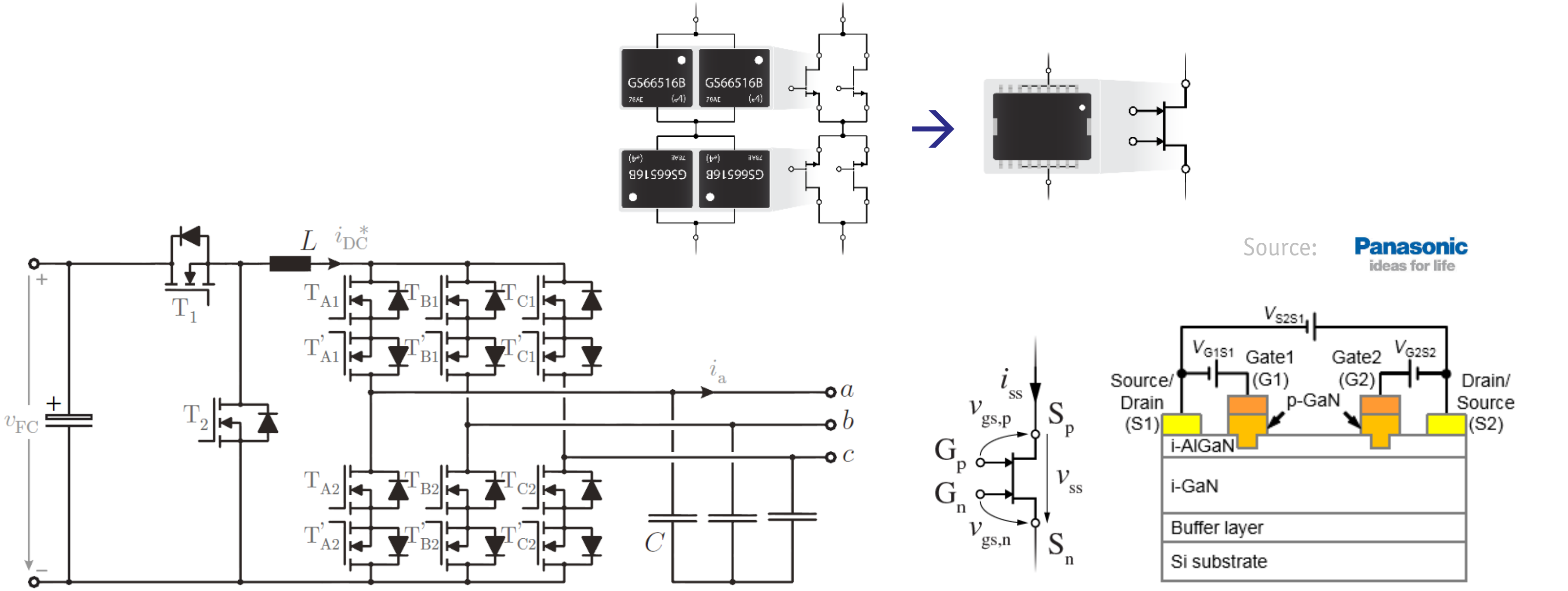
- *Phase Modular Concept* → *Y-Inverter* *(Buck-Stage / Current Link / Boost-Stage)*
- *3-Φ Integrated Concept* → *Buck-Stage & Current DC-Link Inverter*



→ *Low Number of Ind. Components* & *Utilization of Bidir. GaN Semicond. Technology*

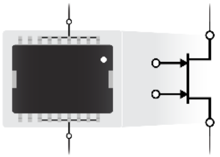
3-Φ Integrated Buck-Boost CSI

- *Bidirectional/Bipolar Switches → Positive DC-Side Voltage for Both Directions of Power Flow*

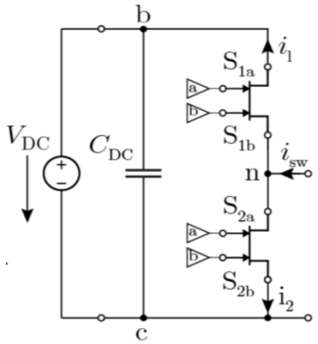


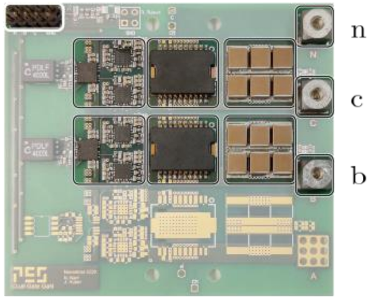
- *Monolithic Bidir. GaN Switches → Factor 4 Reduction of Chip Area Comp. to Discrete Realization*

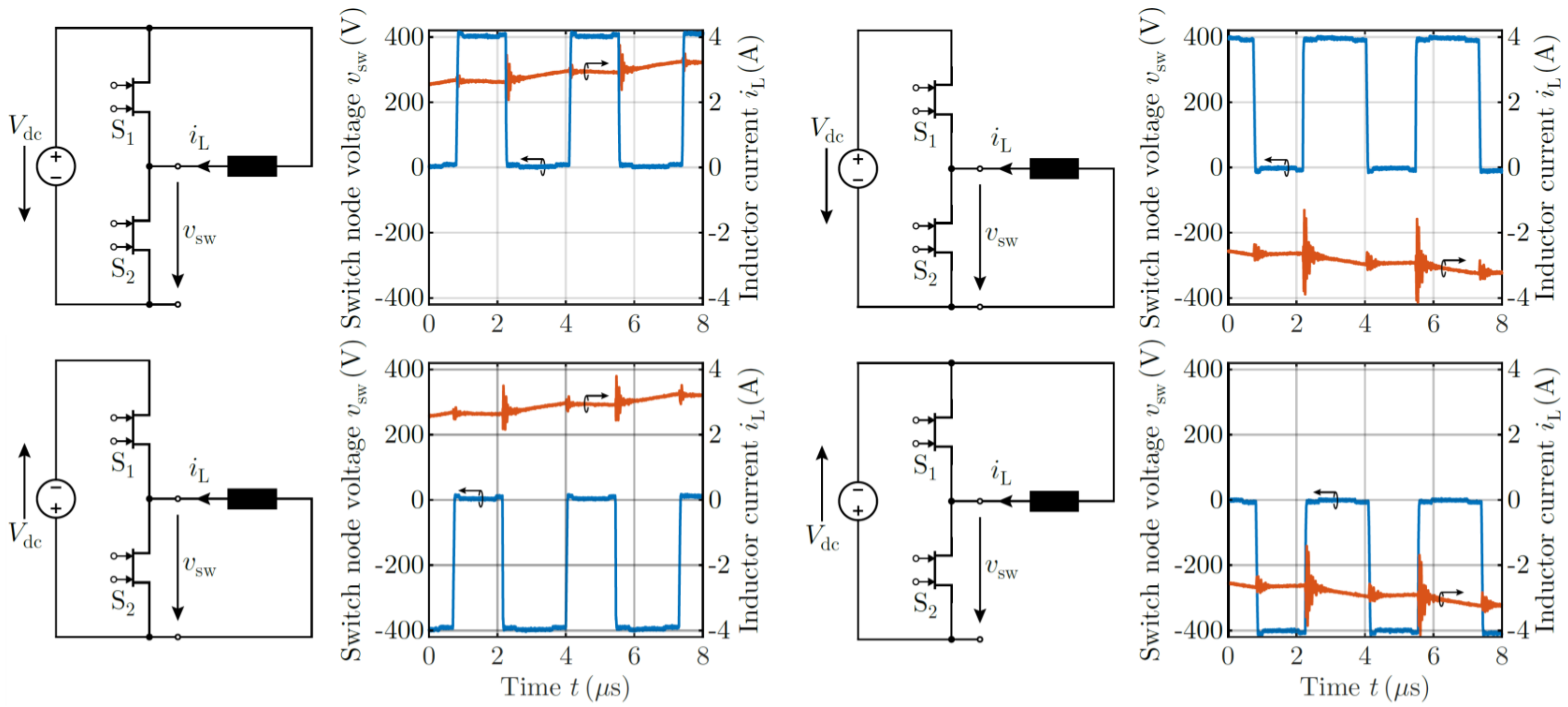
600V GaN Monolithic Bidir. Switch (M-BDS)



- *Power America Project — Based on Infineon's CoolGaN™ HEMT Technology ($R_{DS(on)}$= 70mΩ)* Infineon
- *Dual-Gate Device / Controllability of Both Current Directions*
- *Bipolar Voltage Blocking Capability | Normally On or Off*



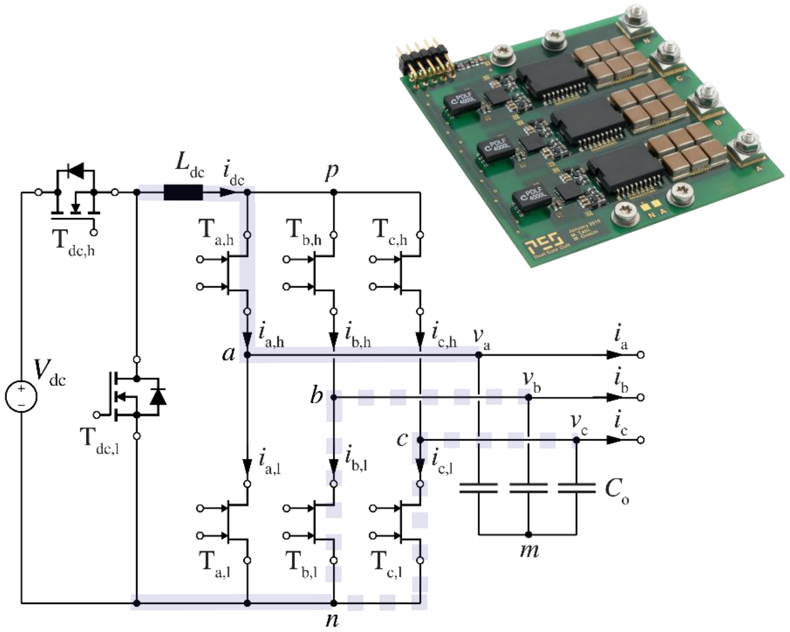


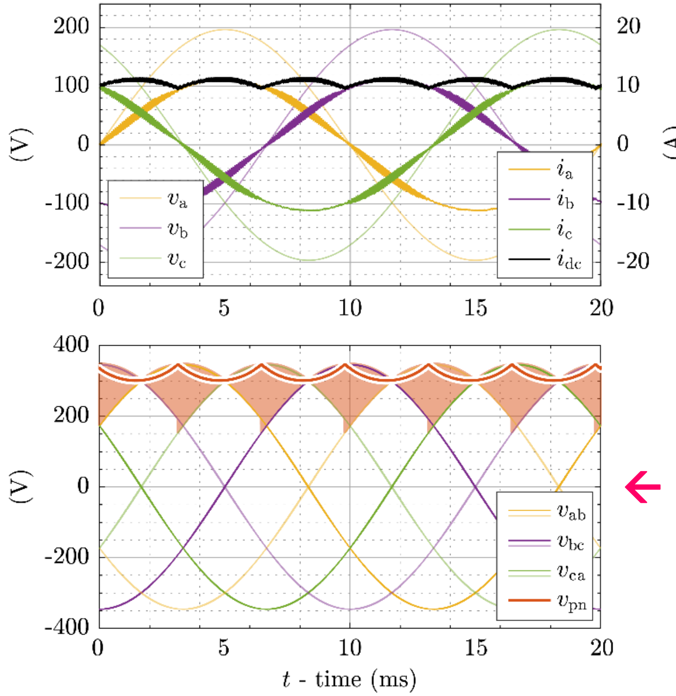


- *Analysis of 4-Quardant Operation of $R_{DS(on)}$= 140mΩ Sample @ ±400V*

3-Φ-Integrated Buck-Boost CSI

- *"Synergetic" Control of Buck-Stage & CSI Stage*
- *6-Pulse-Shaping of DC Current by Buck-Stage → Allows Clamping of a CSI-Phase*

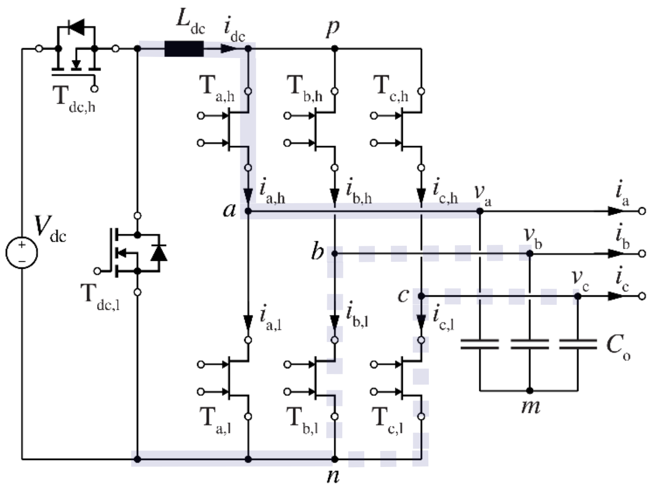


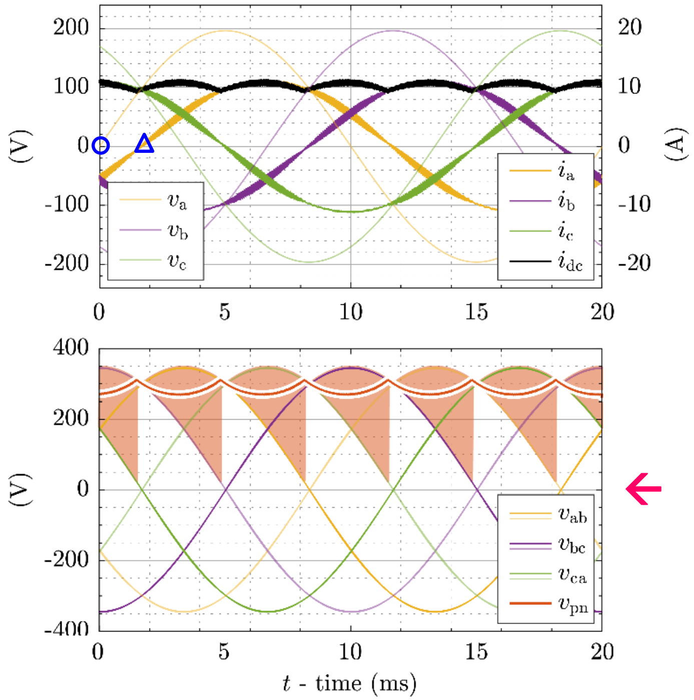


- *Switching of Only 2 of 3 Phase Legs → Reduction of Sw. Losses by ≈ 86% (!)*

3-Φ Integrated Buck-Boost CSI

- *"Synergetic" Control of Buck-Stage & CSI Stage*
- *6-Pulse-Shaping of DC Current by Buck-Stage → Allows Clamping of One CSI-Phase*

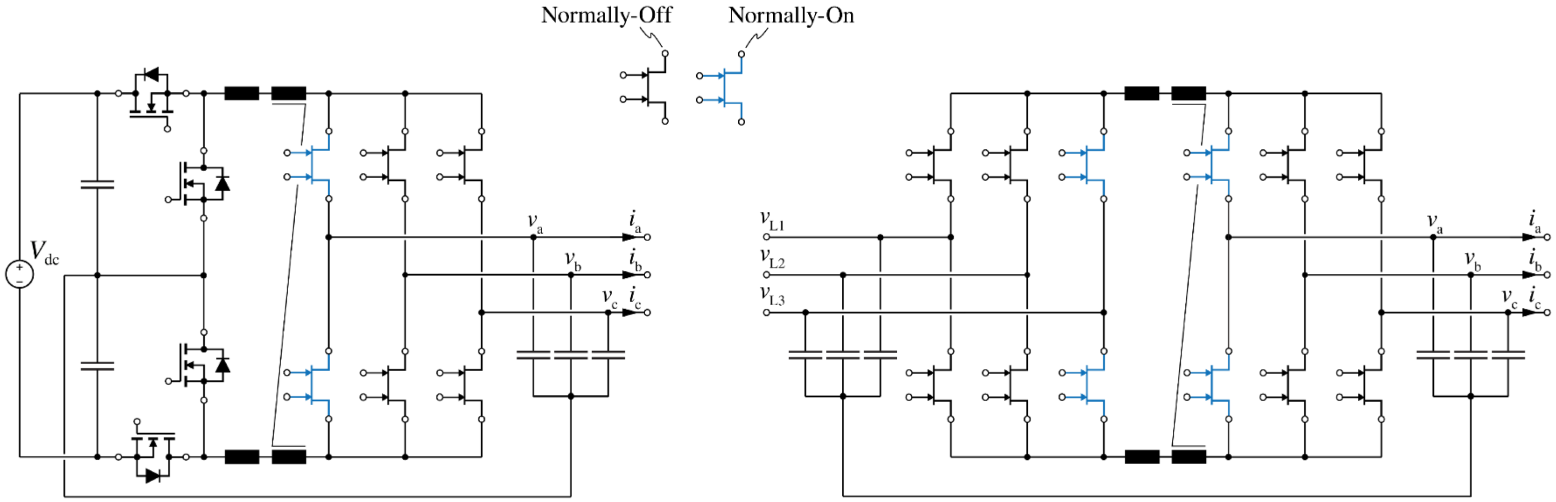




- *Operation for 30° Phase Shift of AC-Side Voltage & Current*

Future Research

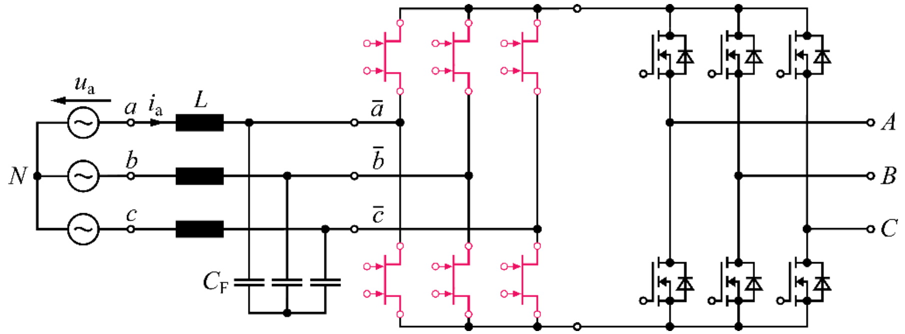
- *Advanced DC/AC Topologies incl. CM-Filtering*
- *Extension of 2/3-PWM to Bipolar DC-Link Voltage 3-Φ AC/AC Converter*
- *Multi-Objective Design & Comparative Evaluation*



- *Partial Use of "Normally-On" Switches for Freewheeling in Case of Auxiliary Power Loss*

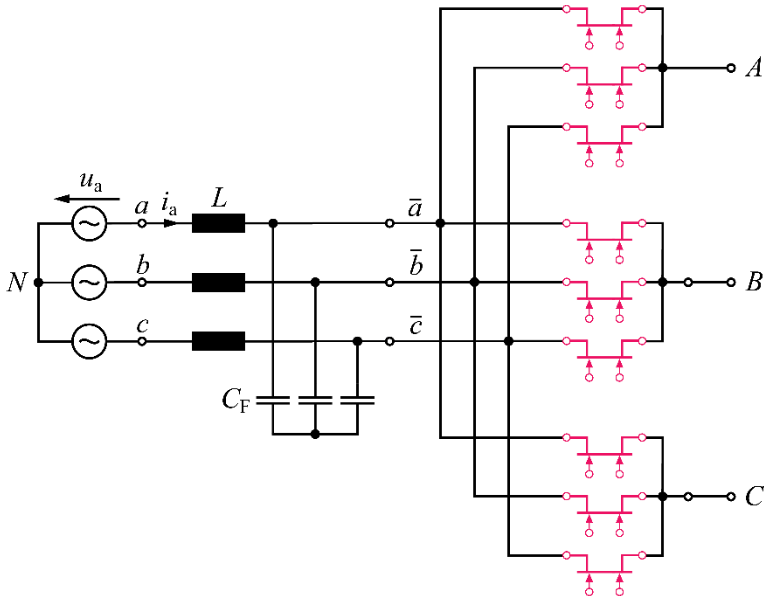
Remark 3-Φ AC/AC Matrix Converter

- *Indirect Matrix Converter (IMC)*
  - CSI GaN M-BDS AC/DC Front-End
  - ZCS Commutation of CSI Stage @ i_{DC}=0
  - No 4-Step Commutation



  - Higher # of Switches Compared to CMC
  - Lower Cond. Losses @ Low Output Voltage
  - Thermally Critical @ $f_{out} \rightarrow 0$

- *Direct Matrix Converter (CMC)*
  - 4-Step Commutation
  - Exclusive Use of GaN M-BDSs



  - Thermally Critical @ $f_{out} \approx f_{in}$

3-Φ PFC Rectifier System

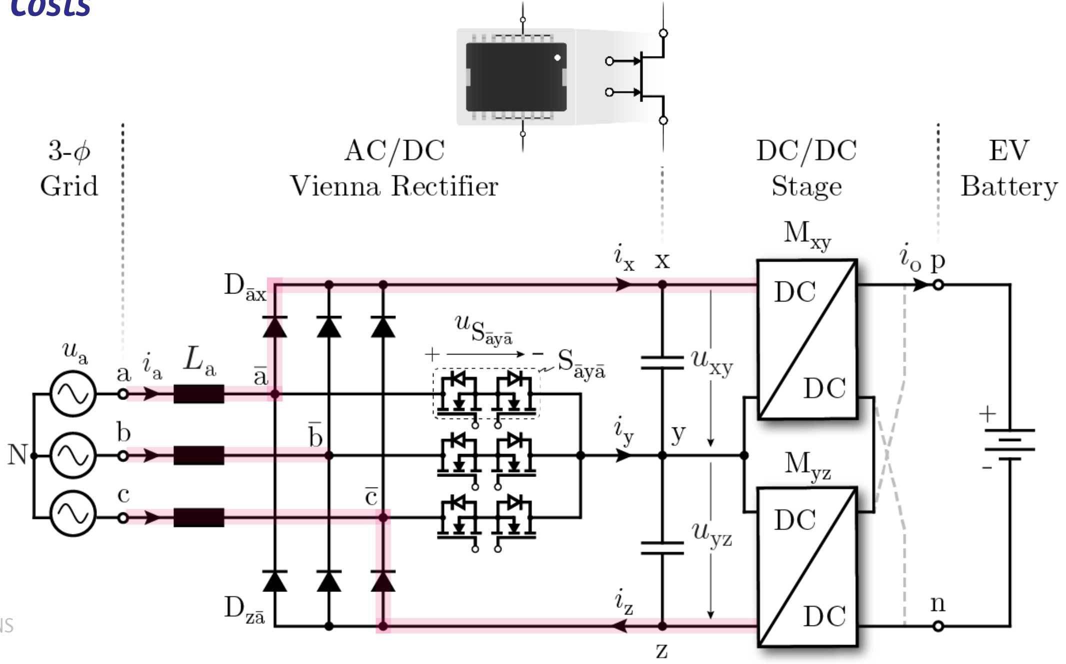
Synergetic Control
Matrix-Type Isolated Topology

Source: Porsche
Mission-E Project

Selected EV Charger Topology

- Isolated Controlled Output Voltage
- Buck-Boost Functionality & Sinusoidal Input Current
- *Applicability of 600V GaN M-BDSs*
- *High Power Density / Low Costs*

Source: SIEMENS

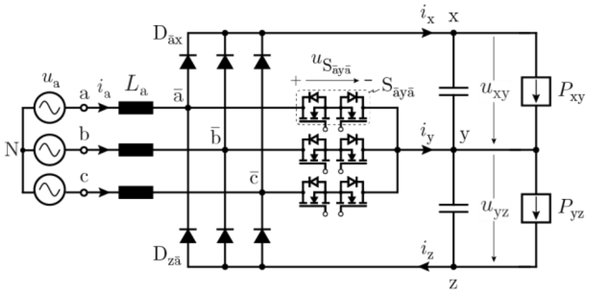


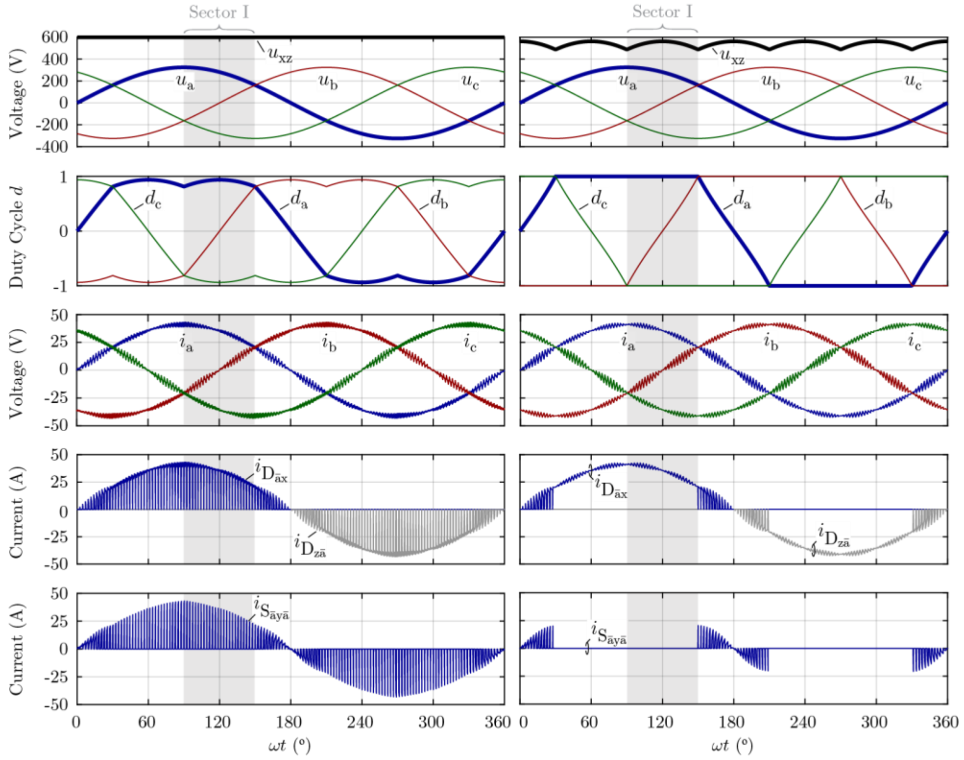
→ *Conventional / Independent* ***OR*** *"Synergetic Control" of Input & Output Stage*

Conventional vs. “Synergetic” Control

- *1/3-Modulation → Significant Red. of Losses of the Power Switches Comp. to 3/3-PWM*

- *Conduction Losses ≈ -80%*
- *Switching Losses ≈ -70%*

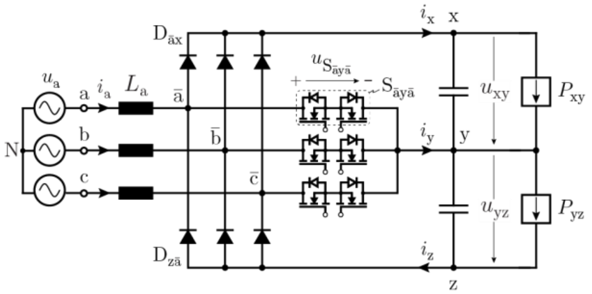


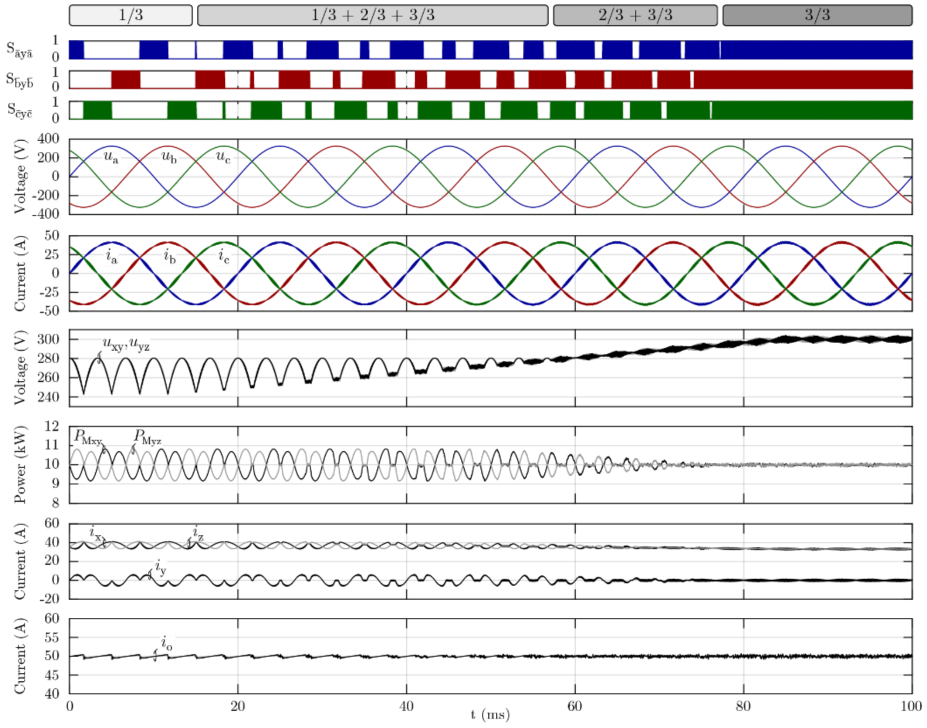


→ *Operating Point Dependent Selection of 1/3-PWM OR 3/3-PWM for Min. Overall Losses*

AC/DC Stage Transition to Full-Boost Operation

- *Different Operating Regimes* → *Synergetic* | *Partial-Boost* | *Full-Boost*



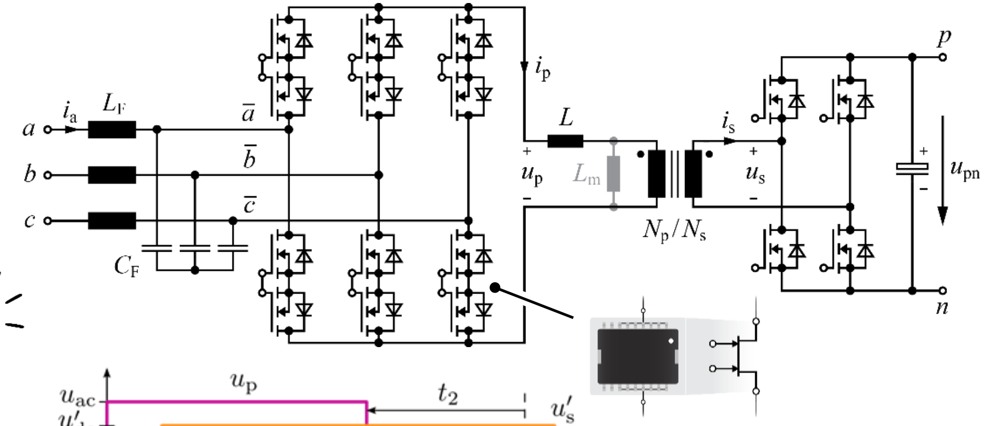


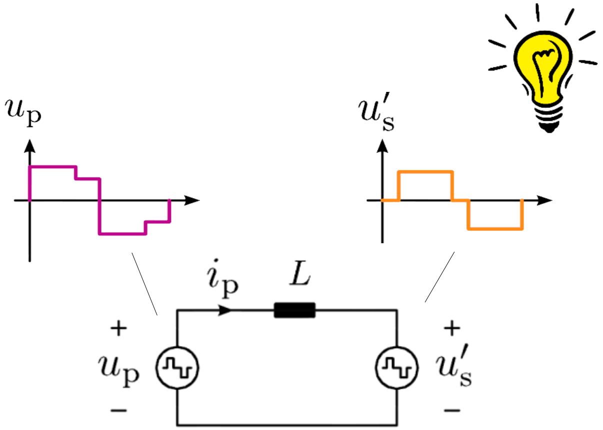
→ *Intermediate 2/3-Operation for Limiting DC-Link Center Point Current (Low DC-Cap.)*

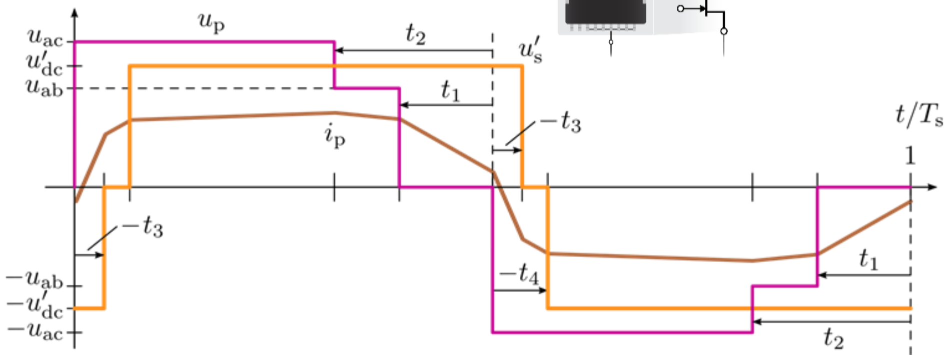
Isolated Matrix-Type Rectifier

Isolated 3-Φ Matrix-Type PFC Rectifier (1)

- *Based on Dual Active Bridge* (DAB) Concept
- *Opt. Modulation* (t_1...t_4) for Min. Transformer RMS Curr. & ZVS or ZCS
- Allows Buck-Boost Operation







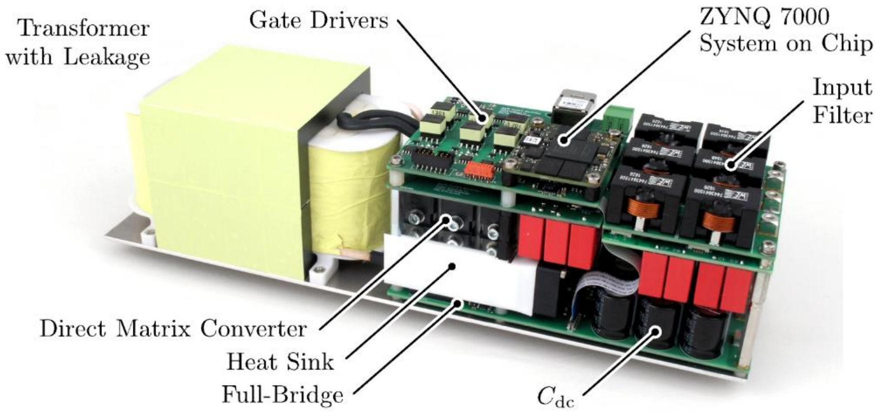
► Equivalent Circuit

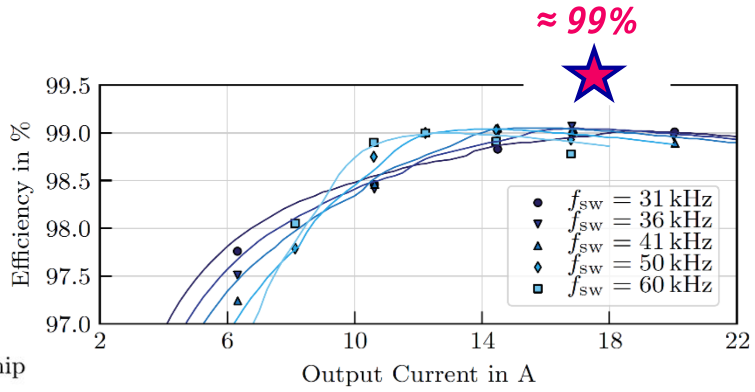
► Transformer Voltages / Currents

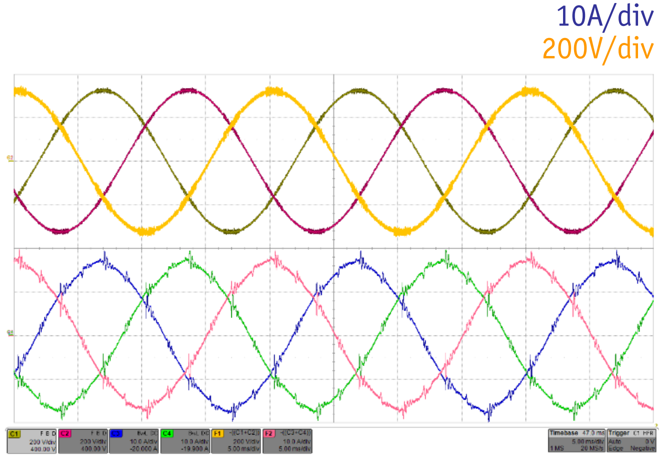
Isolated 3-Φ Matrix-Type PFC Rectifier (2)

- Efficiency η = 98.9% @ 60% Rated Load (ZVS)
- Mains Current $THD_I \approx 4\%$ @ Rated Load
- Power Density $\rho \approx 4\text{kW/dm}^3$

P_O = 8 kW
U_N = 400V_{AC} → U_O = 400V_{DC}
f_S = 36kHz

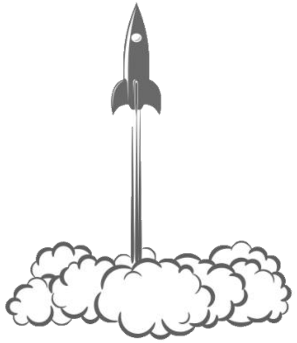






- 900V / 10mΩ SiC Power MOSFETs
- Opt. Modulation Based on 3D Look-Up Table

X-Technology #4

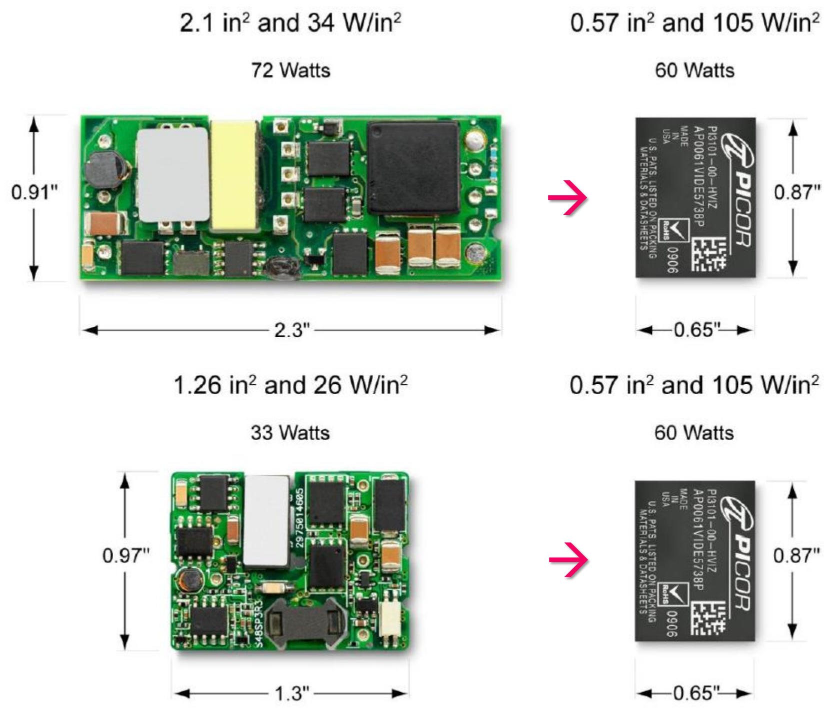


3D-Packaging
Automated Manufacturing

3D-Packaging / Heterogeneous Integration

- *System in Package (SiP) Approach*
- *Minim. of Parasitic Inductances / EMI Shielding / Integr. Thermal Management*
- *Very High Power Density (No Bond Wires / Solder / Thermal Paste)*
- *Automated Manufacturing*

Source: VICOR



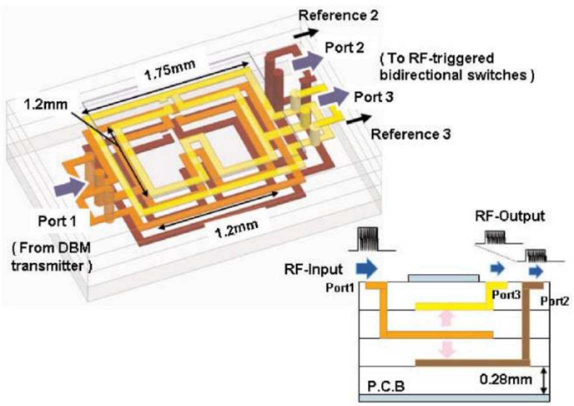
- *Future Application Up to 100kW (!)*
- *New Design Tools & Measurement Systems (!)*
- *University / Industry Technology Partnership (!)*

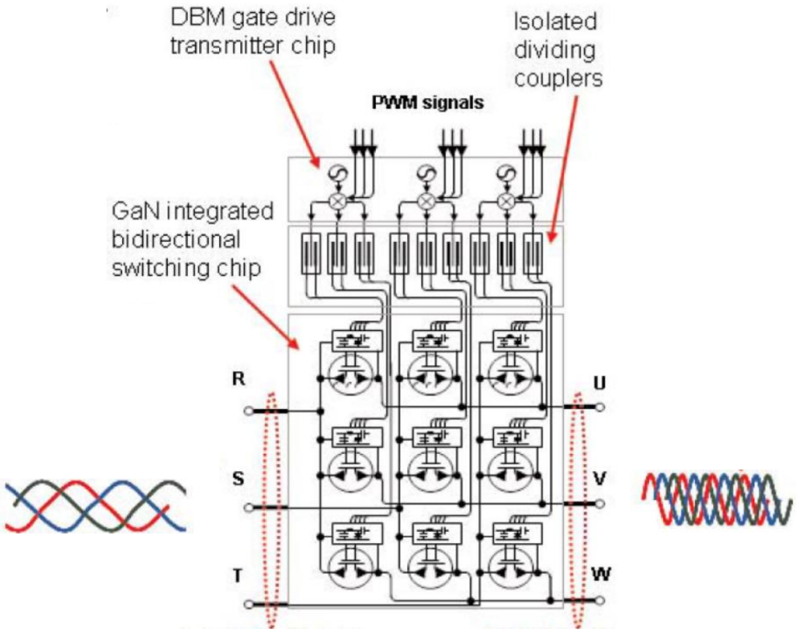
Monolithic 3D-Integration

Source: Panasonic ISSCC 2014

- GaN 3x3 Matrix Converter Chipset with Drive-By-Microwave (DBM) Technology
  - 9 Dual-Gate GaN AC-Switches
  - DBM Gate Drive Transmitter Chip & Isolating Couplers
  - Ultra Compact → 25 x 18 mm^2 (600V, 10A – 5kW Motor)

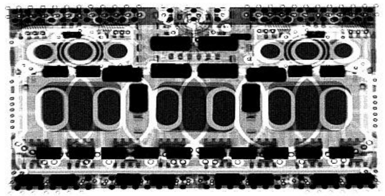
5.0GHz Isolated (5kVDC) Dividing Coupler





Remark – Future Experimental Analysis

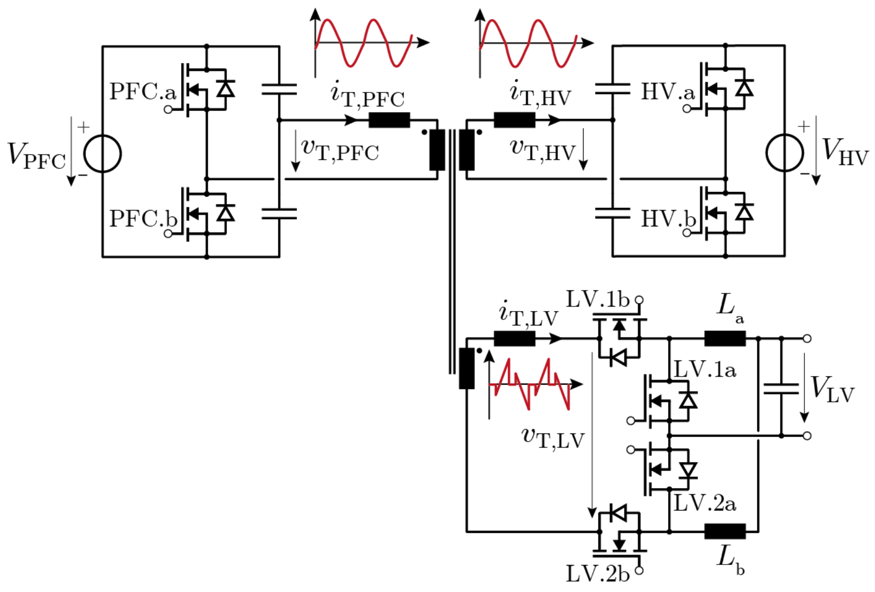
- No Access to Inner Details / Only Terminal Waveforms Available for Measurement (!)

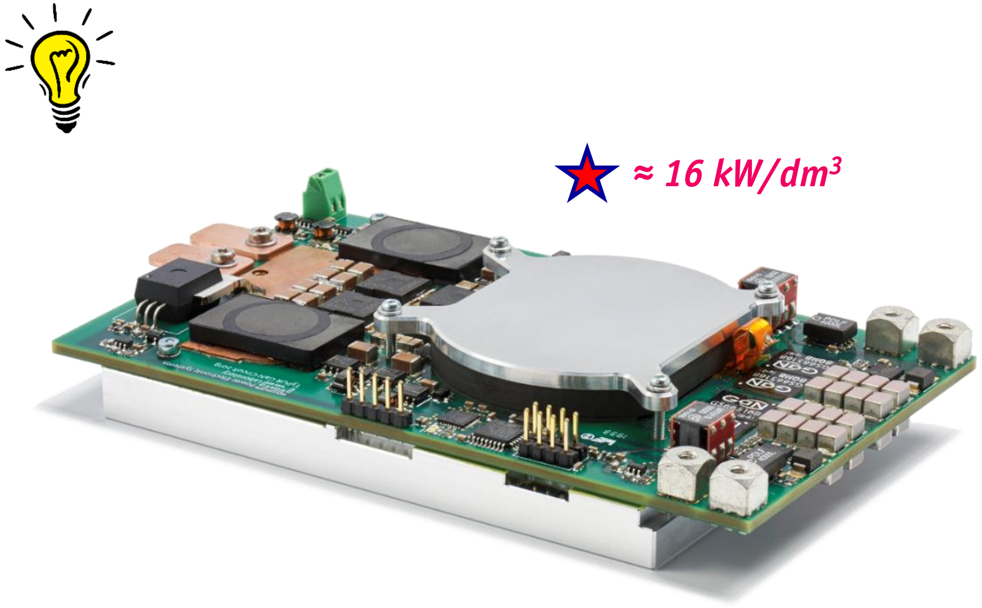


- Convergence of *Measurement & Simulation* → *"Augmented Reality" Oscilloscope*
- *Measured* Signals & *Simulated* Inner Voltages/Currents/Temp. Displayed Simultaneously
- Automatic Tuning of Simulation Parameter Models for Best Fit of Simulated/Measured Waveforms

PCB-Based 3-Port Resonant GaN DC/DC Converter

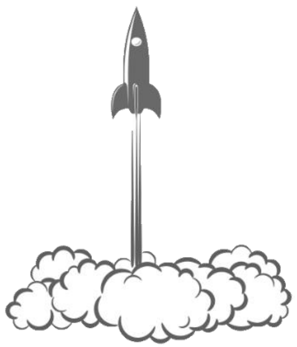
- Single Transformer & Decoupled Power Flow Control
- Charge Mode PFC → HV (250...500V) SRC DCX / Const. f_{sw}, Min. Series Inductance / ZVS
- Drive Mode HV → LV (10.5...15V) 2 Interleaved Buck-Converters / Var. f_{sw} / ZVS
- P = 3.6kW





- Peak Efficiency of 96.5% in Charge Mode / 95.5% in Drive Mode

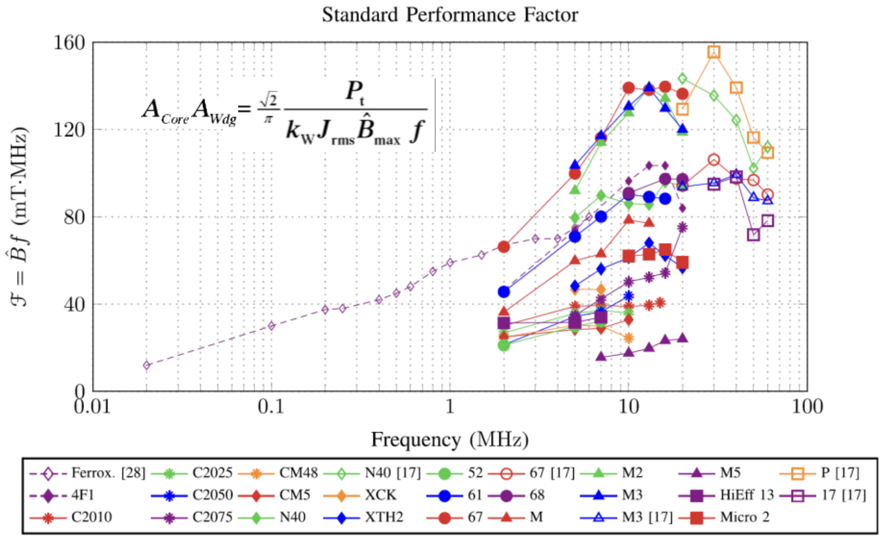
X-Technology #5



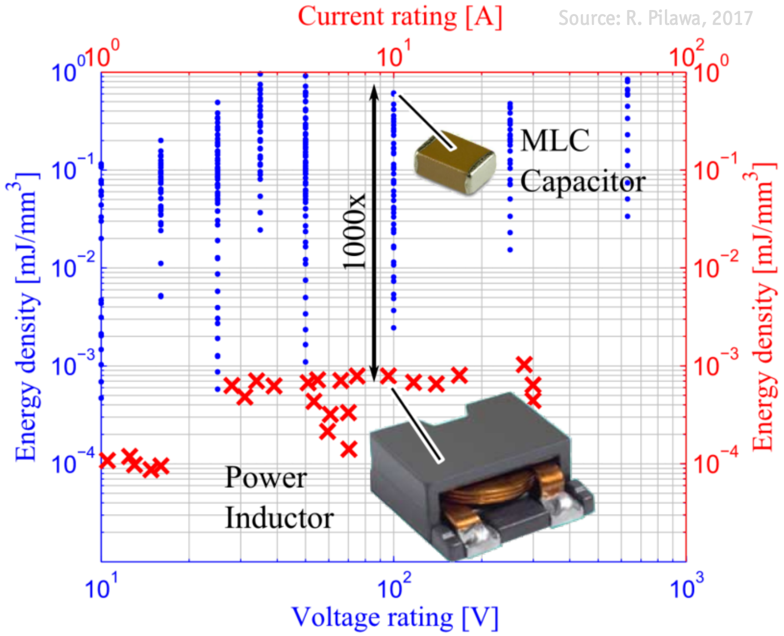
Ceramic Capacitors
HF (NiZn) Magnetics

HF Magnetic Materials & Ceramic Capacitors

- *High Performance Factor of Low Permeability Magnetic Materials for 2...20MHz*
- *Volumetric Efficiency (uF/cm³) Improvement of MLCCs Exceeds Moore´s Law (!)*
- *Hybrid Ind./Cap. Converter Concepts for Min. Magnetic Energy Storage Requirements*

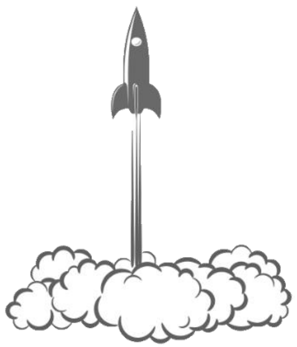


Source: A.J. Hanson, 2016



- *Performance Factor $\hat{B}\cdot f$ Indicates Power Handling Capability @ Const. Loss Density & Core Volume*

X-Technology #6

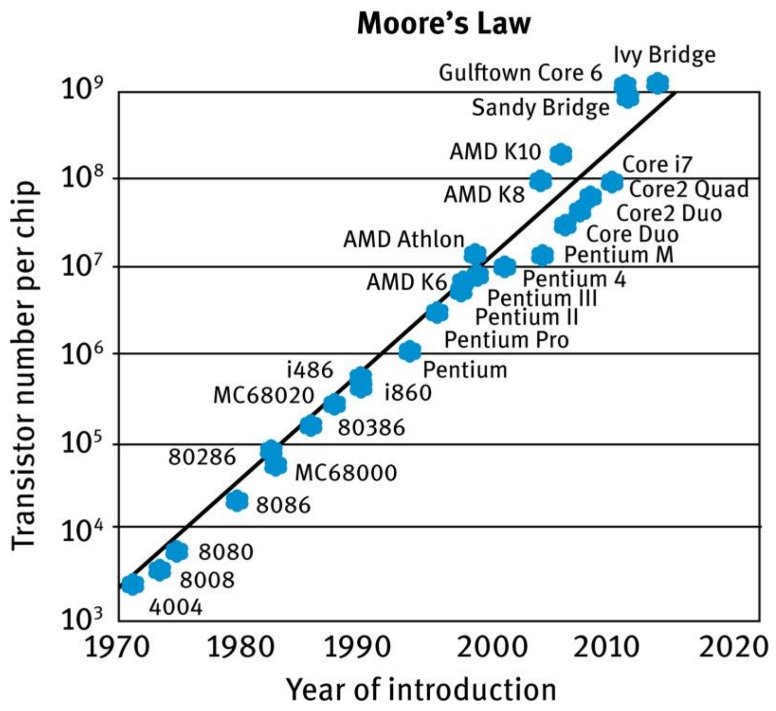


Automated Design
Digital Twin / Industry 4.0

Digital Signal & Data Processing

■ *Exponentially Improving uC / Storage Technology (!)*

— *Extreme Levels of Density / Processing Speed*
— *Software Defined Functions / Flexibility*
— *Cont. Relative Cost Reduction*



Source: Ostendorf & König /DeGruyter

- *Fully Digital Control of Complex Systems*
- *Massive Computational Power → Fully Automated Design & Manufacturing / Industrial IoT (IIoT)*

Automated Design Roadmap

- *End-to-End Horizon of Modeling & Simulation*
- *Design for Cost / Volume / Efficiency Target / Manufacturing / Testing / Reliability / Recycling*

Autonomous Design → Design 4.0

– *Independent* Generation of Full Designs for Final Expert Judgement

Augmented Design

– *Suggestion* of Design Details Based on Previous Designs

Assisted Design ←

– *Support* of the User with Abstracted Database of Former Designs

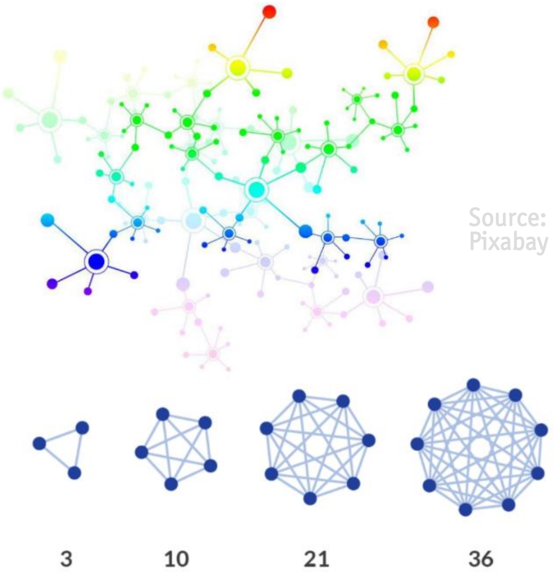
State-of-the-Art

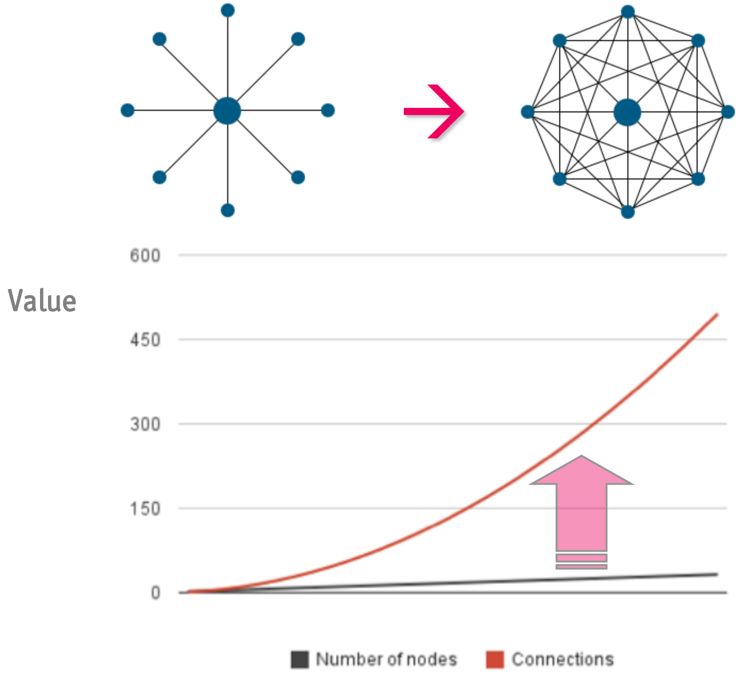
– *User Defined* Models and Simulation / Fragmented

- *AI-Based Summaries → No Other Way to Survive in a World of Exp. Increasing # of Publications (!)*

Scaling Law – Power Electronics 4.0

- **Metcalfe's Law**
  - *Moving from Hub-Based Concept to Community Concept Increases Value Exponentially (~n(n-1) or ~n log(n))*



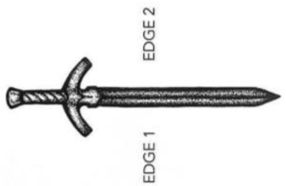


- *Automated Design / Digital Control / Digital Twin*

Conclusion

— *S-TCM Full ZVS Inverters*
— *Multi-Level/Cell Inverter Topologies*
— *Buck-Boost Inverter w/ Integrated Output Filter*
— *Inverter Motor Integration*

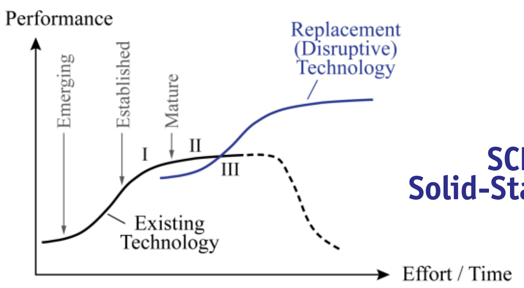
Summary

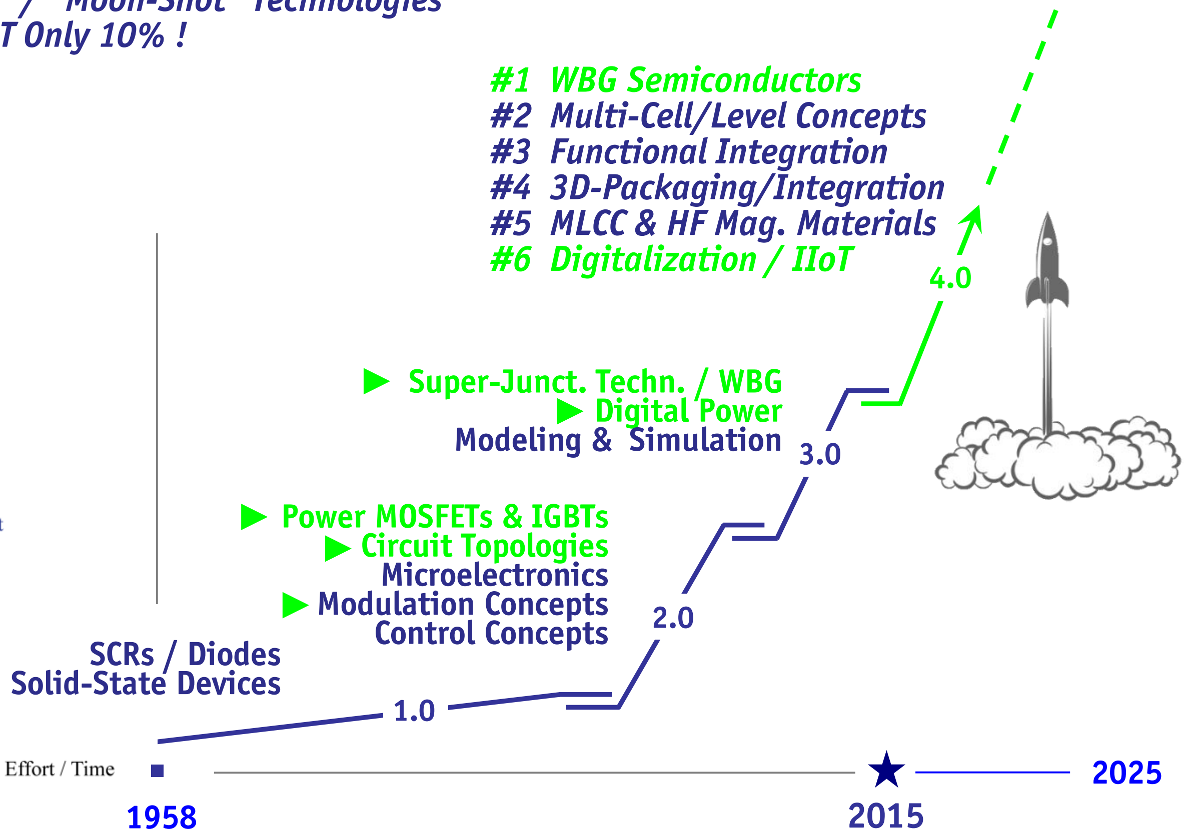


— *Low On-Resistance & High Sw. Speed SiC / GaN*
— *Monolithic Bidirectional GaN*
— *Integration of Switch / Gate Drive / Sensing / Monitoring*
— *SiC/GaN 4.0*

S-Curve of Power Electronics

- *Power Electronics 1.0 → Power Electronics 4.0*
- *Identify "X-Concepts" / "Moon-Shot" Technologies*
- *10 x Improvement NOT Only 10% !*

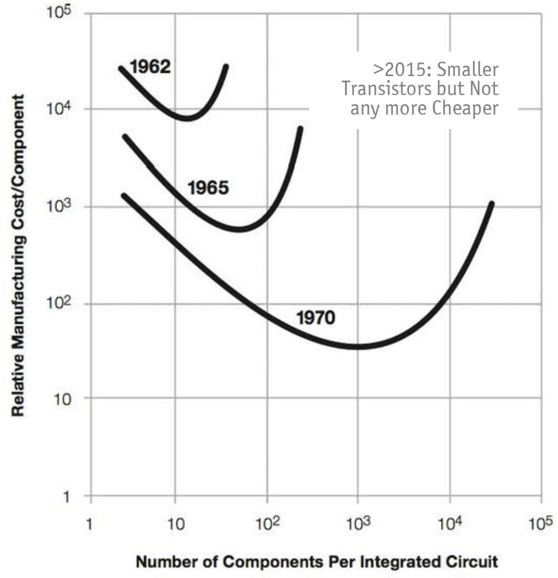




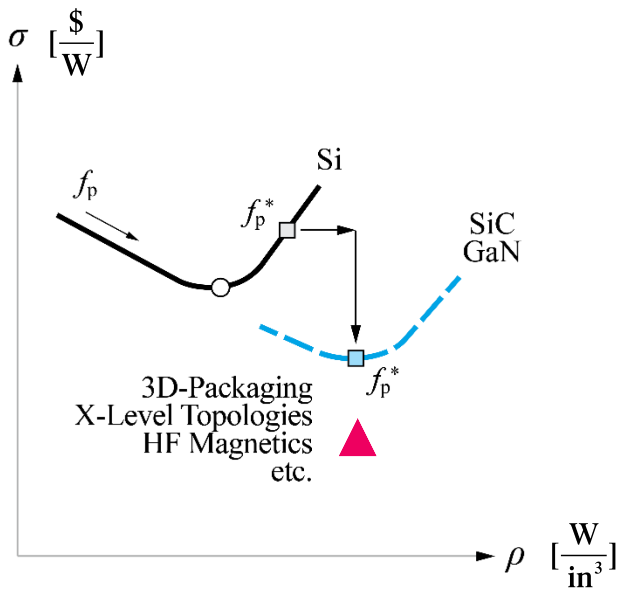
Comparison to "Moores Law"

- "Moore´s Law" Defines Consecutive Techn. Nodes Based on Min. Costs per Integr. Circuit (!)
- Complexity for Min. Comp. Costs Increases approx. by Factor of 2 / Year

Economy of Scale → ← Lower Yield



Gordon Moore: The Future of Integrated Electronics, 1965 (Consideration of Three Consecutive Technology Nodes)

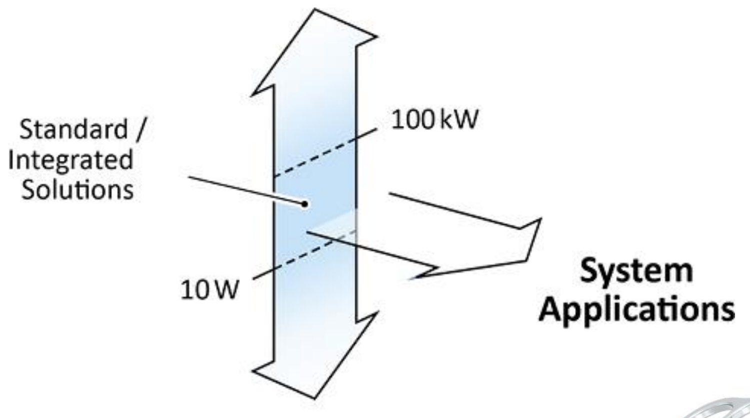


▶ Definition of "$\eta^*, \rho^*, \sigma^*, f_p^*$–Node" Must Consider Conv. Type / Operating Range etc. (!)

Future Development

- Commoditization / Standardization
- Extreme Cost Pressure (!)

"There is Plenty of Room at the Top" → *Medium Voltage/Frequency Solid-State Transformers*



Power-Supplies on Chip ← **"There is Plenty of Room at the Bottom"**

- Key Importance of Technology Partnerships of Academia & Industry

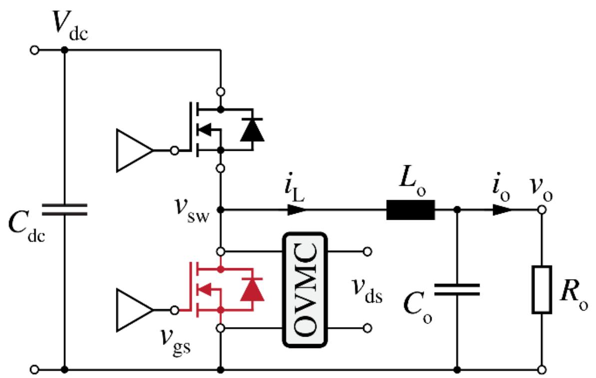
Thank you!

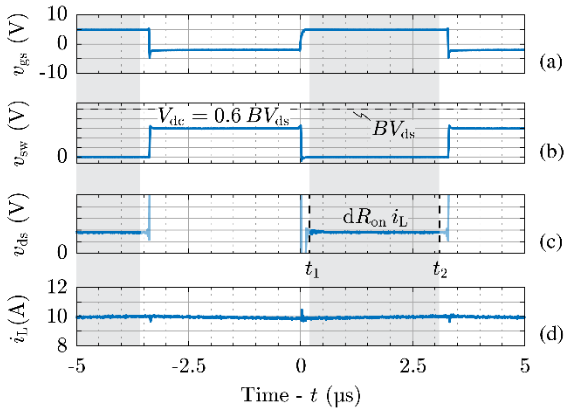
Appendix A

*Accurate Measurement of
SiC/GaN Power Semiconductor
On-State & Switching Losses*

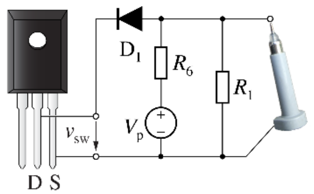
On-State Voltage Measurement (1)

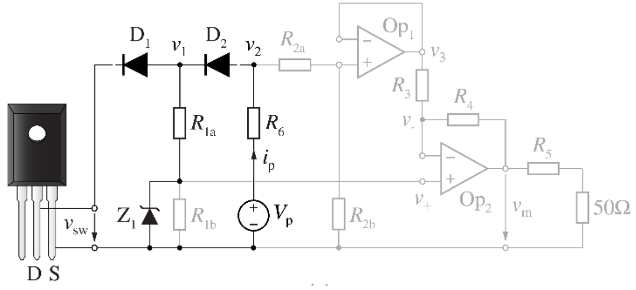
- *Device / Load Current / Gate Voltage / Junction Temp. → On State-Resistance $R_{DS(on)}$*





$R_{DS(on)} = v_{DS(on)} / i_L$

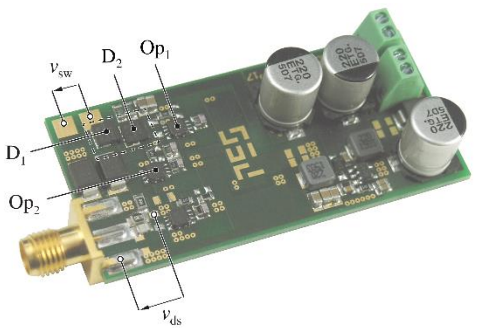


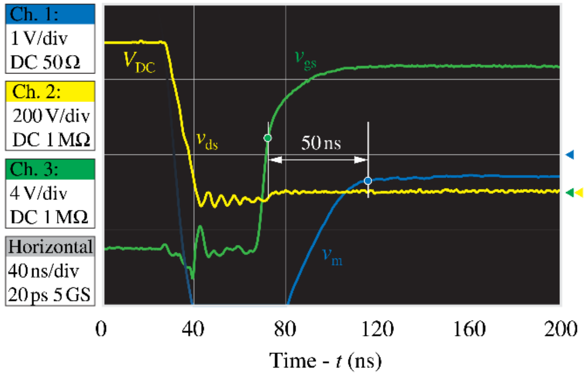


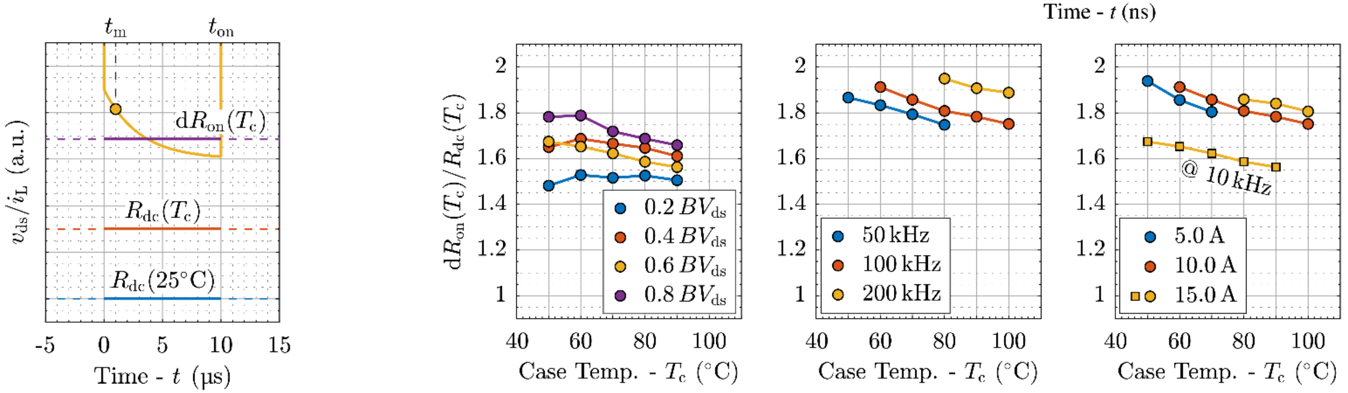
- *Decoupling High Blocking Voltage and (Very) Low On-State Voltage (≈1V << BV_{DS})*

On-State Voltage Measurement (2)

- *High Accuracy* → *Compensation of Decoupling Diode Forward Voltage*
- *Fast Dyn. Response* → *Valid Measurement 50ns After Turn-On*



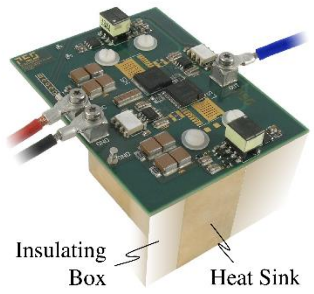


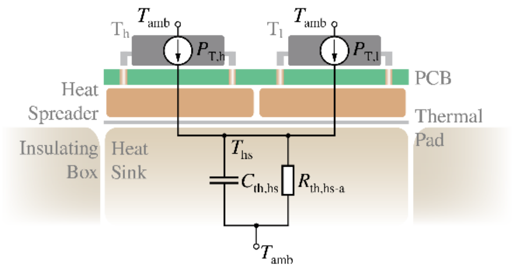


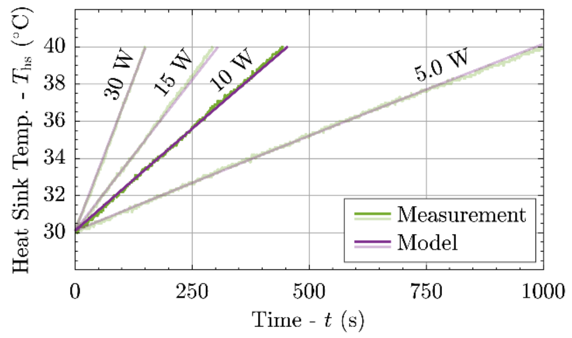
- *Example — Dyn. $R_{DS(on)}$ of GaN HEMTs → 2x $R_{DS(on)}$ @ 100kHz - 0.6BV_{DS}*

Switching Loss Measurement

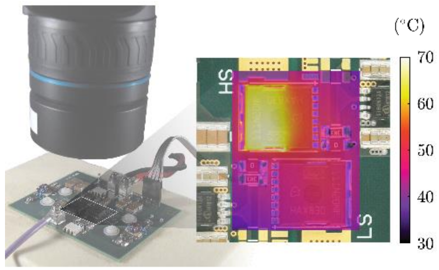
- *Heat-Sink Temp.-Based Transient Calorim. Method → 15 min / Measurement*

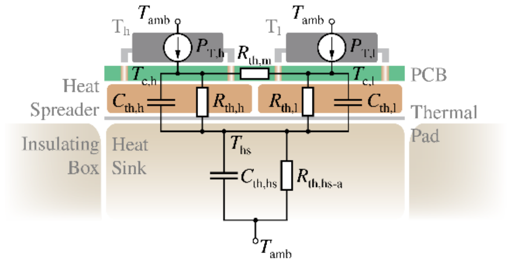


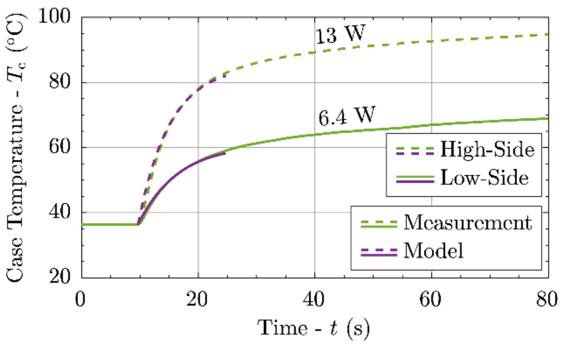




- *Case Temp.-Based Ultra-Fast Method → 15 sec / Measurement*

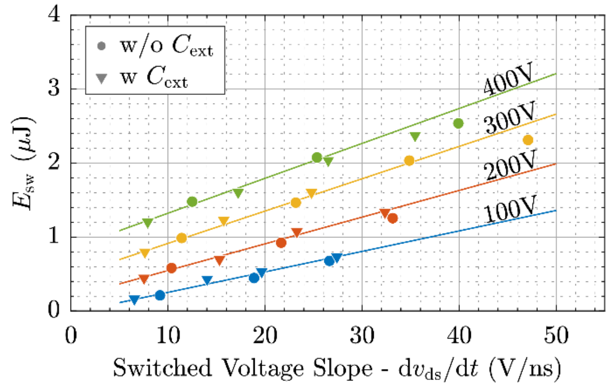


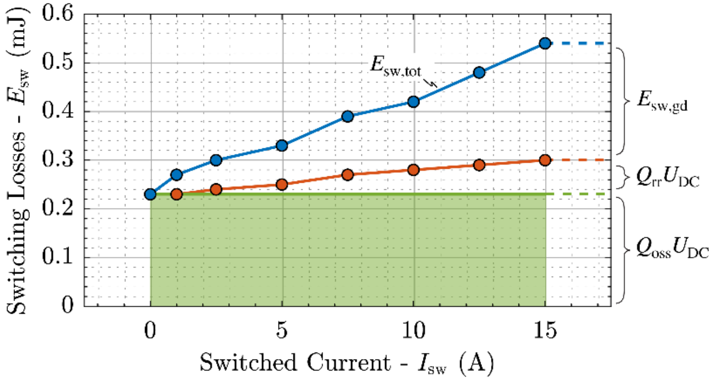




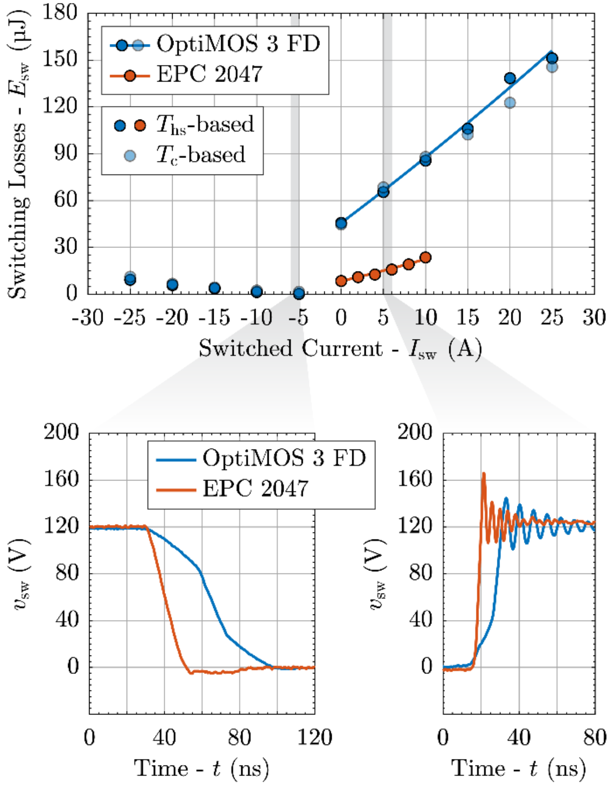
Example Measurement Results

■ 650V GaN (ZVS)





■ 200V Si vs. GaN (Hard-Sw. & ZVS)



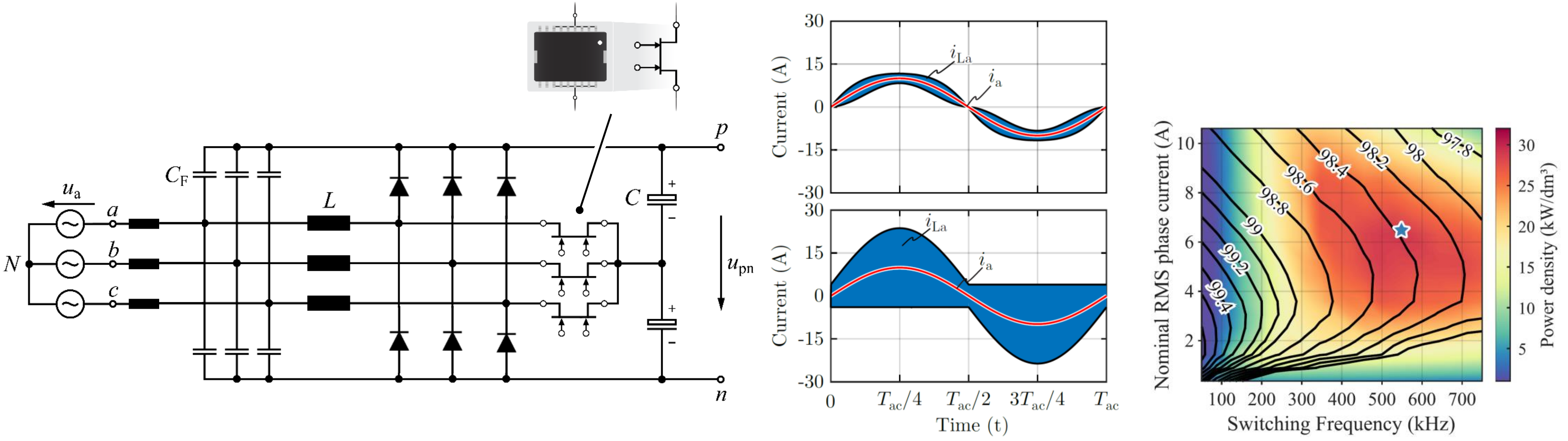
■ 1.2kV SiC (Hard-Sw.)

Appendix B

T-Type M-BDS Topology
Integr. Active Filter PFC Rectifier
Swiss Rectifier

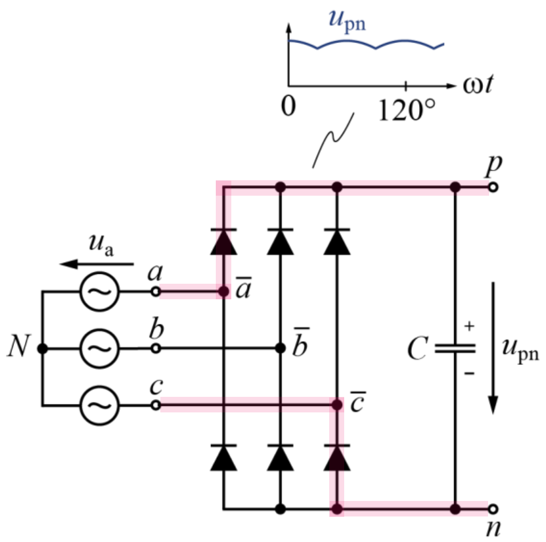
Remark — T-Type PFC Rectifier Topology

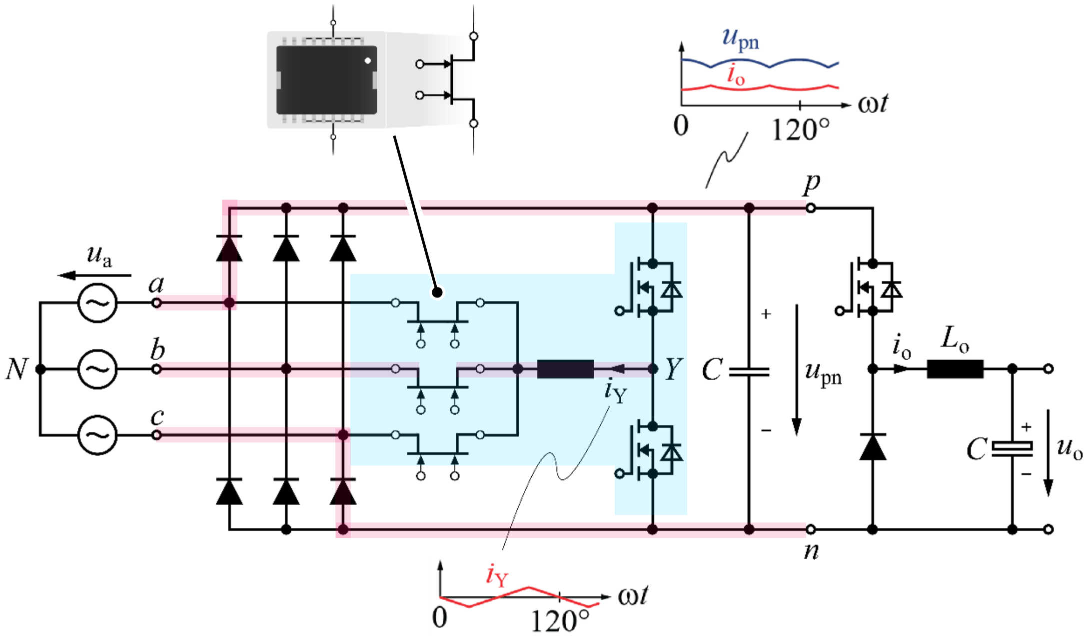
- *Application of 600V M-BDSs @ U_{pn}= 800V in Combination w/ 1200V SiC MOSFETs*
- *Hard-Switching Cont. Cond. Mode (CCM) or ZVS TCM Operation*



- *Max. Power Density | 98.4% Efficiency @ CCM w/ f_{sw}= 550kHz*

Integr. Active Filter (IAF) Rectifier





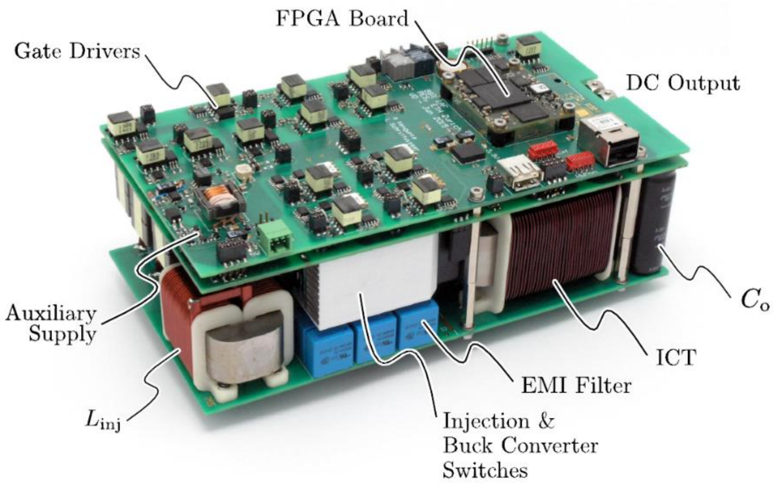
■ Non-Sinusoidal Mains Current

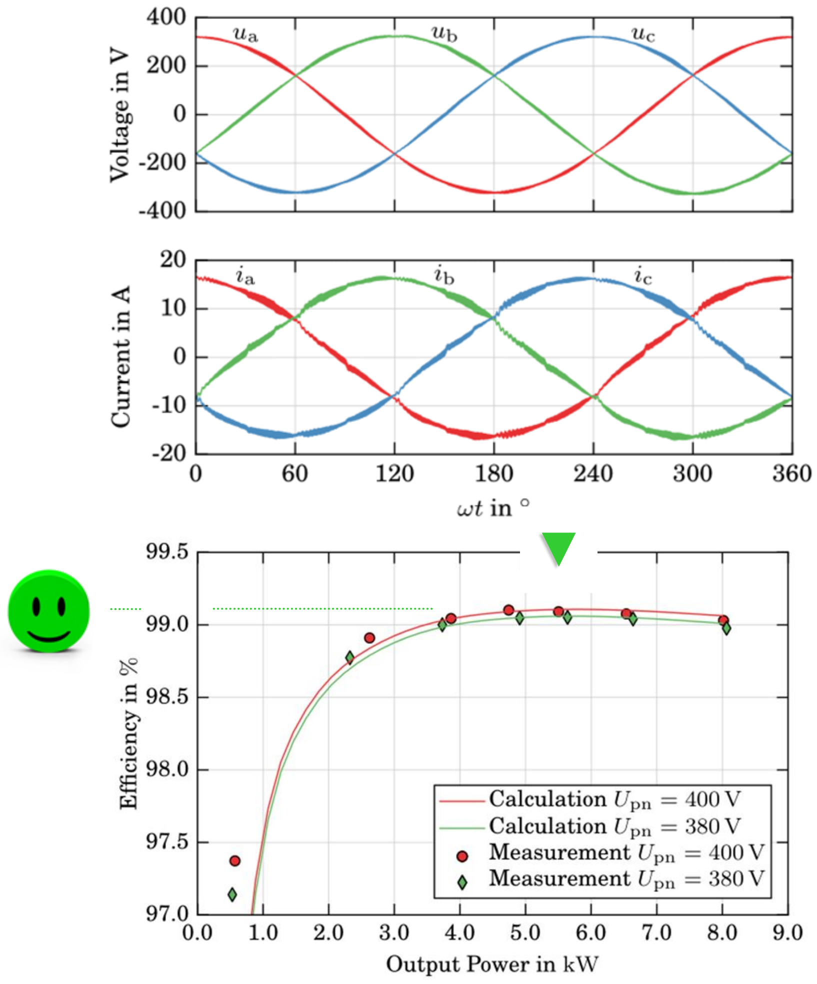
→ P_0= const. Required
→ *3-Φ Unfolder Front End*
→ *3rd Harmonic Injection in Middle Phase*
→ *Basic Idea: M. Jantsch, 1997 (for PV Inv.)*

IAF Rectifier Demonstrator

- Efficiency η > 99.1% @ 60% Rated Load
- Mains Current $THD_I \approx 2\%$ @ Rated Load
- Power Density $\rho \approx 4\text{kW/dm}^3$

P_0= 8 kW
U_N= 400V$_{AC}$ → U_0= 400V$_{DC}$
f_S = 27kHz



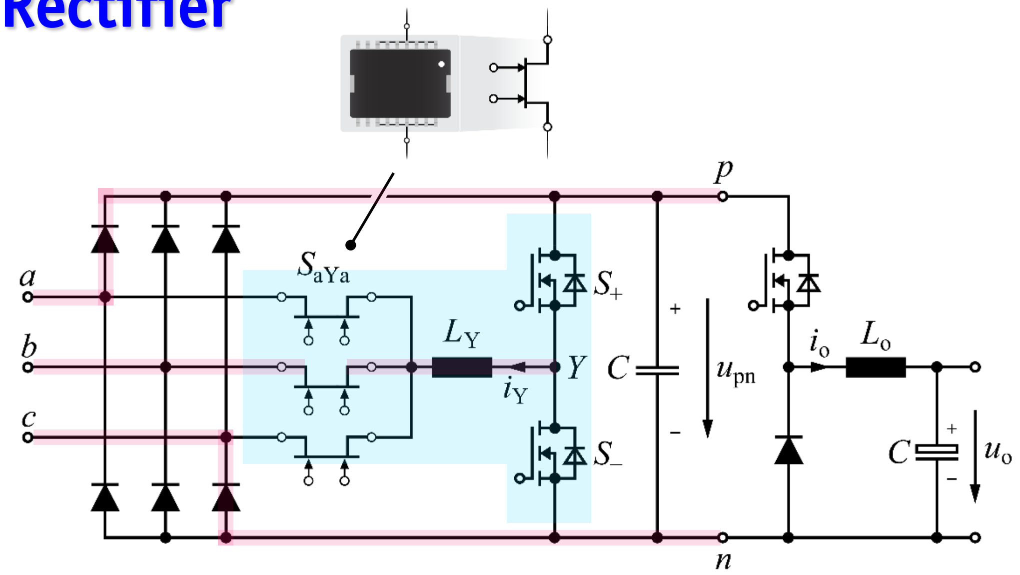


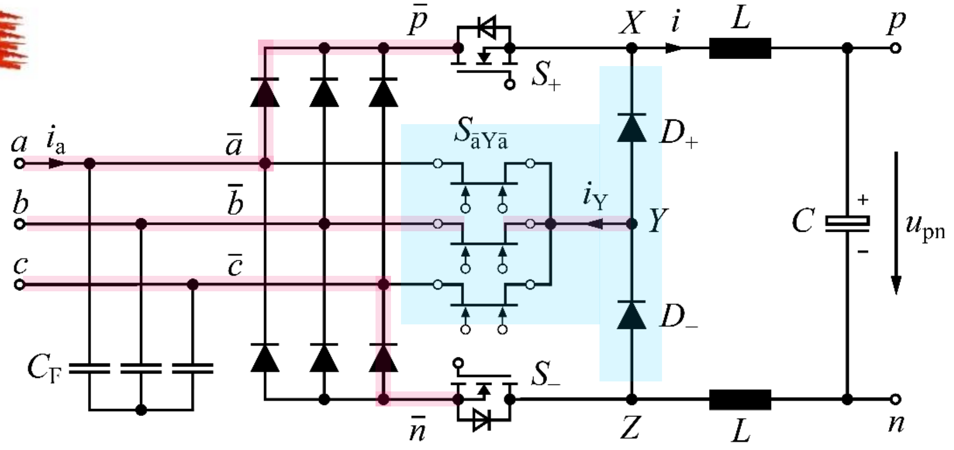
- ▶ SiC Power MOSFETs & Diodes
- ▶ 2 Interleaved Buck Output Stages

SWISS Rectifier

IAF Rectifier → Swiss Rectifier

- Controlled Output Voltage
- Sinusoidal Mains Current
- i_y Def. by KCL: E.g. $i_a - i_c$



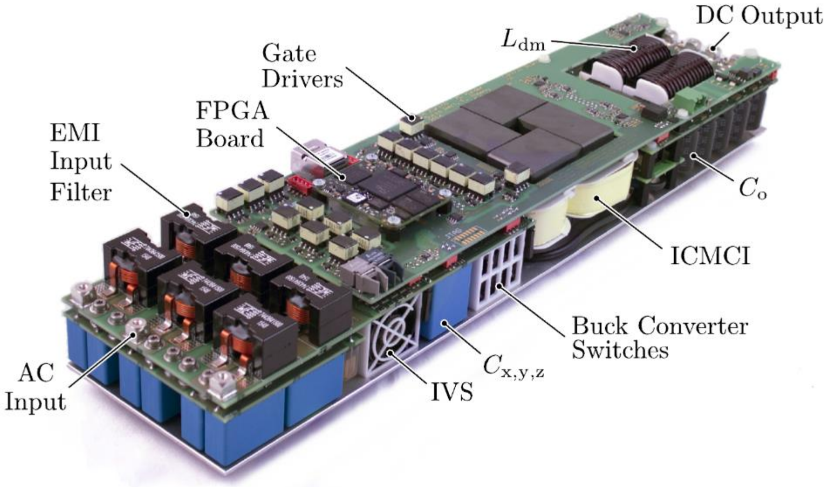


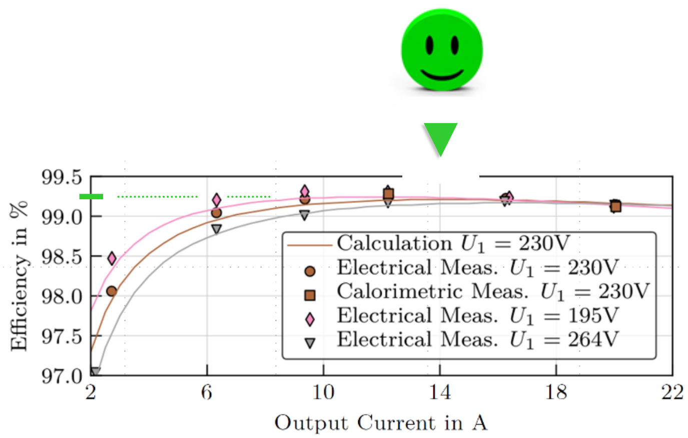
▶ Low Complexity

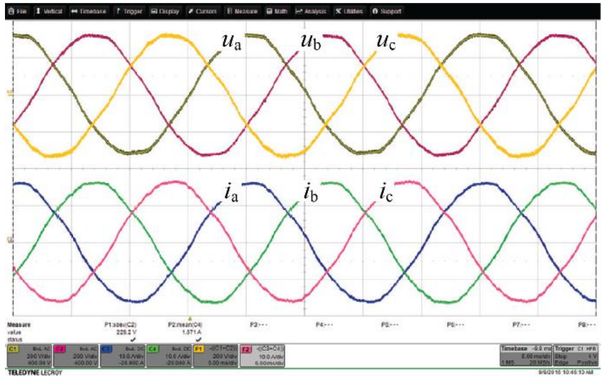
Swiss Rectifier Demonstrator

- Efficiency η = 99.26% @ 60% Rated Load
- Mains Current $THD_I \approx 0.5\%$ @ Rated Load
- Power Density $\rho \approx 4\mathrm{kW/dm^3}$

P_O = 8 kW
U_N = 400V_{AC} → U_O = 400V_{DC}
f_S = 27kHz







► SiC Power MOSFETs & Diodes
► Integr. CM Coupled Output Inductors (ICMCI)

— **The END** —