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***Abstract*—Aiming for ever more compact and efficient Electric Vehicle (EV) battery chargers, in this paper a three-phase phase-modular buck-boost Three-Level Flying Capacitor Y-Rectifier (3L-FC-YR) is introduced. The unique circuit structure of the 3L-FC-YR requires time-varying flying capacitor voltages, making the safe and performant operation of such a converter system challenging. Accordingly, a special clamping modulation strategy is proposed which assures equal blocking voltage distribution among the power semiconductors. Further, control strategies and protection circuitry for system startup or failure-mode handling are discussed, such that all practical aspects of the 3L-FC-YR are covered. The concept is verified by means of closed-loop circuit simulations and the resulting waveforms are presented. Finally, a Pareto comparison considering the efficiency and power density limits of the 3L-FC-YR and the standard 2L-YR is conducted considering an extremely wide DC output voltage range of 200 V to 920 V according to the DC CCS HPC350 EV charging standard. The results indicate a significantly higher performance of the 3L approach and/or the feasibility of a CISPR 11 Class A compliant 3L-FC-YR prototype with a peak efficiency of 98.5 % and power density of 19 $\mathrm{kW/dm^3}$ (311 $\mathrm{W/in^3}$).**

***Index Terms*—EV charger, AC/DC converter, three-phase, three-level, SiC, flying capacitor, buck-boost Y-Rectifier**

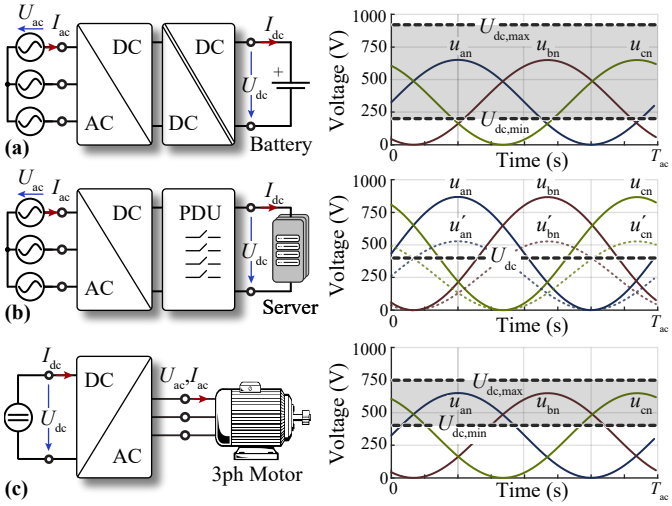

Fig. 1: Typical application examples for three-phase AC/DC converters with buck-boost capability: **(a)** EV battery charger, **(b)** server supply and **(c)** DC-supplied motor drive system powered by e.g. a fuel-cell or a battery.

I. Introduction

The proliferation of three-phase AC/DC converters with buck-boost capability increases, as a large set of applications requires converter operation within wide input-output voltage ranges. Typical examples are highlighted in **Fig. 1**, where the three-phase AC voltages (with line-to-neutral voltage amplitude $\hat{U}_{\mathrm{ac}}$) are converted into a DC voltage U_{dc} or vice versa:

Fig. 1a shows an Electric Vehicle (EV) battery charger powered from the European three-phase grid with $\hat{U}_{\mathrm{ac}} = 325\,\mathrm{V}$, where for the DC Combined Charging System (DC CCS) High Power Charging (HPC) class [1] a DC voltage range from $U_{\mathrm{dc,min}} = 200\,\mathrm{V}$ to $U_{\mathrm{dc,max}} = 920\,\mathrm{V}$ has to be covered. The charger system comprises a Power Factor Correction (PFC) rectifier front-end and an isolated DC/DC converter. If the DC/DC stage is realized as an ultra efficient series resonant converter with limited output voltage controllability [2], the rectifier front-end is required to cover the complete DC output voltage range. Further, bidirectional converters are preferred as power can be fed back to the AC grid, hence enabling EV batteries to serve as distributed energy storage elements. **Fig. 1b** presents a server supply rectifier generating a constant DC bus voltage of $U_{\mathrm{dc}} = 400\,\mathrm{V}$ which supplies the server racks via a Power Distribution Unit (PDU) [3]. The AC input voltage level provided by a supplying medium voltage transformer depends on the geographic location and is typically $480\,\mathrm{V_{rms}}$ (i.e. $\hat{U}_{\mathrm{ac}} = 390\,\mathrm{V}$) in the US and $400\,\mathrm{V_{rms}}$ (i.e. $\hat{U}'_{\mathrm{ac}} = 325\,\mathrm{V}$) in Europe and can further vary in a range of $+20\,\%/-10\,\%$. Last, **Fig. 1c** shows a DC-supplied motor drive system, where motor speed-dependent output AC voltages are generated from a DC voltage, which also varies in a wide range if the system is powered by e.g. a battery [4] or a fuel-cell [5].

The phase-modular buck-boost Two-Level Y-Rectifier (2L-YR) [5] [6] allows for a compact AC/DC converter realization with a low number of inductive components. The 2L-YR is a bidirectional converter and is applicable to all aforementioned applications, where in the following an EV battery charger rectifier front-end is considered (cf. **Fig. 1a**). As the power density is a key metric of EV chargers, the utilization of three-level (3L) FC bridge-legs [7] which allows a substantial reduction of the inductive component volume [8] but poses several challenges, is analyzed in this paper. The main power circuit structure of a 3L-FC-YR is depicted in **Fig. 2b** (module a

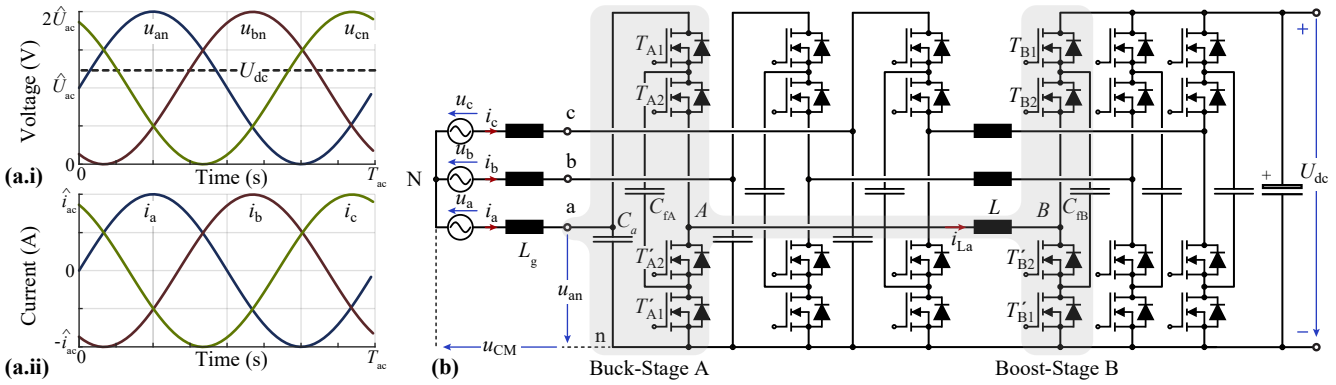

Fig. 2: Proposed Three-Level Flying Capacitor Y-Rectifier (3L-FC-YR) interfacing the three-phase grid and a DC source (e.g. a solar panel) or load (e.g. an EV battery or a passive load). The converter terminal voltages with respect to the negative DC-link rail n and the sinusoidal input currents are shown in **(a.i)** and **(a.ii)**, respectively, and in **(b)** the main power circuit is depicted with module a highlighted in grey.

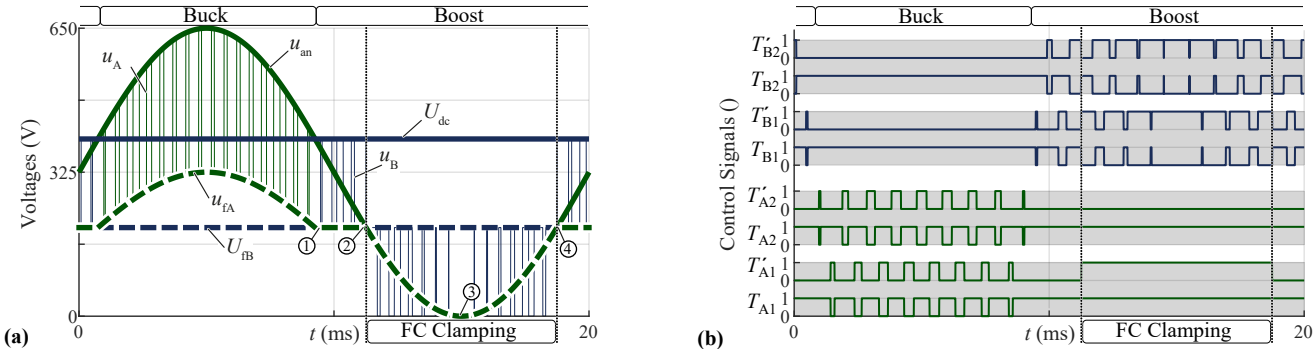

Fig. 3: **(a)** Terminal and FC voltages and **(b)** corresponding semiconductor control signals of the 3L-FC-YR phase module a (cf. **Fig. 2b**).

is highlighted), where semiconductors with lower rated voltage (compared to the 2L-YR) and hence improved figure of merit can be employed [9]. As the high-frequency operation of buck-stage A and boost-stage B is mutually exclusive in each phase module [5], while time-varying input FC voltage references are given, the safe and performant operation of such a converter system is challenging.

Accordingly, this paper describes the relevant aspects of the 3L-FC-YR topology and in **Section II** a dedicated clamping modulation strategy assuring the FC voltage management is derived. In **Section III**, the proposed modulation concept is verified by means of a closed-loop circuit simulation of the system. Furthermore, as the safe start-up of FC converters is critical [10], a start-up control sequence and added passive safety elements are presented in **Section IV**. Then, a Pareto power density / efficiency and a virtual prototype comparison of the 3L-FC-YR and the 2L-YR is conducted in **Section V**. Finally, in **Section VI** the findings are summarized.

II. Operating Principle

The main power circuit of the 3L-FC-YR interfacing the grid AC voltages $u_\mathrm{a}, u_\mathrm{b}, u_\mathrm{c}$ and the DC output voltage U_dc is depicted in **Fig. 2b** and consists of three identical FC DC/DC buck-boost phase modules. As for the standard 2L-YR [5] strictly positive converter terminal voltages $u_\mathrm{an}, u_\mathrm{bn}, u_\mathrm{cn}$ (cf. **Fig. 2a.i**) are generated with respect to the negative DC-link terminal n and since the common-mode offset voltage $u_\mathrm{CM} = \frac{1}{3}(u_\mathrm{an} + u_\mathrm{bn} + u_\mathrm{cn})$ has no corresponding current path, sinusoidal grid currents $i_\mathrm{a}, i_\mathrm{b}, i_\mathrm{c}$ (cf. **Fig. 2a.ii**) can be impressed. Here, the offset voltage is constant with $u_\mathrm{CM} = \hat{U}_\mathrm{ac}$ and hence the maximum input voltage is given by $U_\mathrm{an,max} = 2 \cdot \hat{U}_\mathrm{ac}$. Note that the voltage u_CM is only constrained by the requirement of strictly positive terminal voltages $u_\mathrm{an}, u_\mathrm{bn}, u_\mathrm{cn}$ and can also be used to enable e.g. discontinuous Pulse Width Modulation (PWM) [5] [11].

The three modules of a 3L-FC-YR are operated independently and therefore the modulation strategy is explained here only for phase module a, where the derivation of the duty ratios for the converter stages A and B is identical to the standard 2L-YR [5]. In order to achieve single-stage high-frequency energy conversion, the phase module a is working depending on the instantaneous modulation depth $m(t) = u_\mathrm{an}(t)/U_\mathrm{dc}$ (i.e. the input-output voltage ratio, cf. **Fig. 3a**) in one of the two possible operation modes. In **boost operation** (i.e. $u_\mathrm{an} \leq U_\mathrm{dc}$) the upper switches of the input buck-bridge-leg T_A1 and T_A2 are permanently turned on (hence the switch-node A is clamped to the input terminal), while the stage B is PWM operated and stepping up the input voltage u_an. In **buck operation** (i.e. $u_\mathrm{an} > U_\mathrm{dc}$) the upper switches of the boost-bridge-leg T_B1 and T_B2 are permanently turned on (the switch-node B is clamped to the positive DC-link rail), while stage A is PWM operated and stepping down the input voltage u_an. Accordingly, the respective time varying duty cycles are defined by $d_\mathrm{A}(t) = \min(1, \frac{1}{m(t)})$ and $d_\mathrm{B}(t) = \min(1, m(t))$,

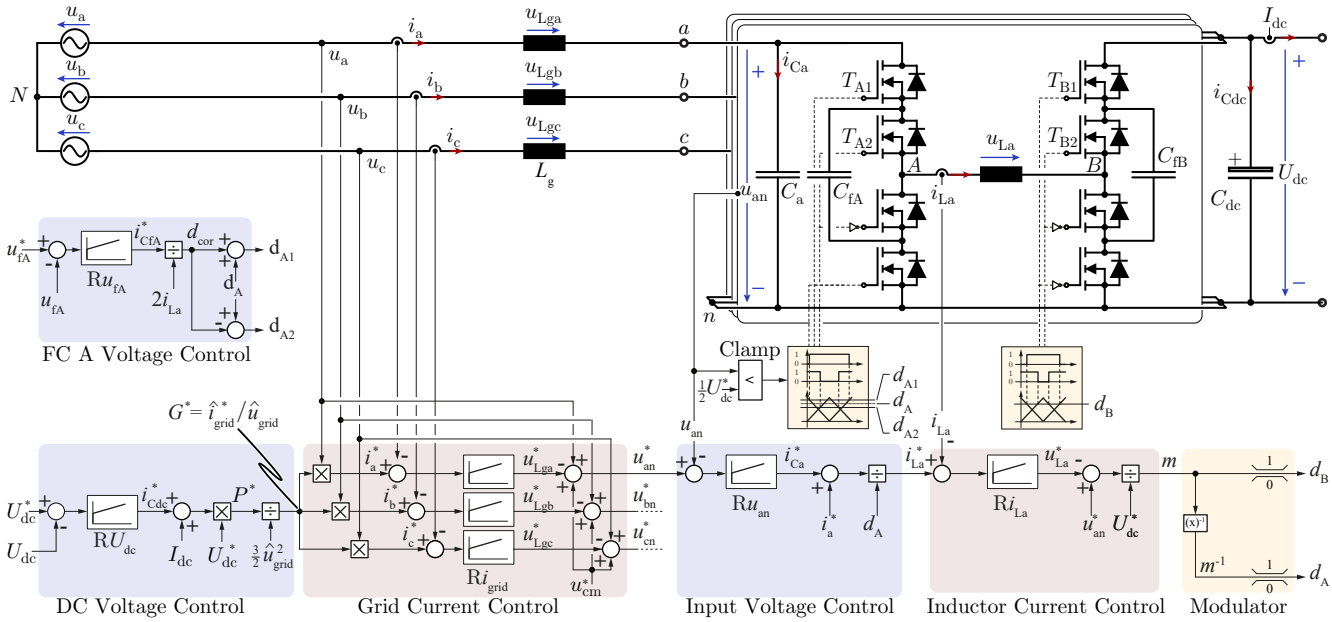

Fig. 4: Cascaded DC output voltage control scheme with the required measurements for a 3L-FC-YR.

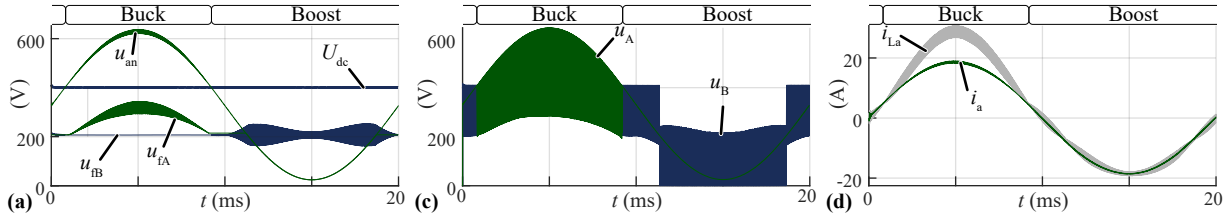

Fig. 5: 3L-FC-YR phase module a closed loop circuit simulation waveforms of **(a)** terminal and FC voltages, **(b)** switch-node voltages and **(c)** currents, for $\hat{U}_{\mathrm{ac}}$ =325 V, U_{dc} =400 V and P =9 kW. The converter operating parameters and component values are $f_{\mathrm{s,eff}} = 2 \cdot f_{\mathrm{s}} = 200\,\mathrm{kHz}$, $L = 85\,\mu\mathrm{H}$, $C_{\mathrm{a}} = 2\,\mu\mathrm{F}$, $L_{\mathrm{g}} = 20\,\mu\mathrm{H}$ and $C_{\mathrm{fA}} = C_{\mathrm{fB}} = 0.5\,\mu\mathrm{F}$.

assuring the mutually exclusive high-frequency operation of stages A and B. The semiconductor control signals (cf. **Fig. 3b**) are generated in a known manner using two 180° phase shifted PWM carriers for the outer (e.g. T_{A1} and T'_{A1}) and inner (e.g. T_{A2} and T'_{A2}) half-bridges of each stage. By doing so, the inductor current i_{La} equally charges and discharges the FCs during one switching period and natural balancing of the FC voltages is enabled [7] [12].

It is important to note that the natural balancing only holds if the respective stage is high-frequency operated. If the module is running e.g. in buck operation (i.e. $m > 1$), the stage B switch-node is clamped to the positive DC-link rail such that C_{fB} is bypassed and hence remains at constant voltage. Given the ideally constant FC voltage $u_{\mathrm{fB}} = U_{\mathrm{dc}}/2$ (cf. **Fig. 3a**), the operation of the boost-stage B is unproblematic and greatly resembles a FC voltage source rectifier. In contrast, the input stage A FC voltage would ideally follow $u_{\mathrm{fA}} = u_{\mathrm{an}}/2$. Converters with time-varying FC voltages are hardly known in literature [13] [14], where [13] relies solely on passive balancing, and in [14] the DC bias-free FC voltage is imposed by means of a passive 2:1 transformer. Here, actively or passively maintaining the input stage A FC voltage at $u_{\mathrm{fA}} = u_{\mathrm{an}}/2$ is only possible during buck operation, and the key time instances for the voltage regulation of C_{fA} are highlighted in **Fig. 3a**:

When starting boost operation (1), C_{fA} is bypassed and it's voltage remains constant at $u_{\mathrm{fA}} = U_{\mathrm{dc}}/2$. More critical, the antiparallel diode of T'_{A1} starts conducting once the input voltage u_{an} falls below u_{fA} (2), paralleling C_{a} and C_{fA}. Accordingly, C_{fA} is fully discharged until (3). There, the input voltage u_{an} starts to rise again and T'_{A1} builds up voltage, while C_{fA} (without further measures) remains fully discharged, resulting in a massive blocking voltage imbalance among the semiconductors of stage A when starting buck operation in the subsequent AC period. Accordingly, the proposed modulation scheme includes the simultaneous turn-on of T_{A1} and T'_{A1} when $u_{\mathrm{fA}} < U_{\mathrm{dc}}/2$, such that C_{fA} is actively clamped to C_{a} when u_{an} starts rising (3) and is only released once the desired FC voltage level is reached in (4). Hence, equal stage A semiconductor blocking voltage sharing is given when entering again buck operation in the subsequent AC period.

III. Control Structure

Fig. 4 displays the cascaded 3L-FC-YR PFC rectifier control structure and **Fig. 5** presents waveforms from a closed-loop circuit simulation:

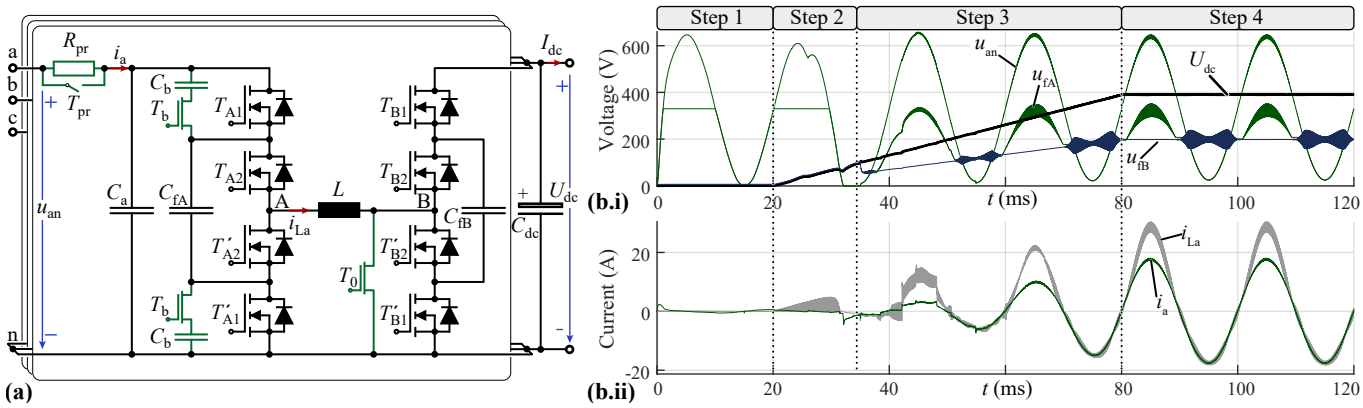

Fig. 6: **(a)** 3L-FC-YR phase module a with passive protection circuitry, i.e. precharging resistor R_{pr} and bypass switch T_{pr}, balancing capacitors C_{b} and normally-on semiconductors T_{b} and T_0. **(b)** Voltage and current waveforms of module a during a controlled ramp-up of the DC output voltage to U_{dc} =400 V.

The control strategy bases on standard PFC rectifier control and sinusoidal grid current references i_{a}^*,i_{b}^*,i_{c}^* are derived based on the DC voltage control error and the measured AC voltages u_{a},u_{b},u_{c}. Then, the input terminal voltage references u_{an}^*,u_{bn}^*,u_{cn}^* are set in order to enforce the required grid currents. The subsequent phase module control (shown again for phase a only in **Fig. 4**) consists of input voltage and inductor current regulator, where the output signal is fed into the 2L-YR modulator [5], generating duty ratios for the mutually exclusive operation of buck-stage A and boost-stage B. The control signals of the power semiconductors are then generated using PWM blocks and taking into account the derived clamping logic for the buck-stage A (cf. **Fig. 3b**).

Simulations revealed insufficient natural FC voltage balancing performance for stage A, which is dependent on how good the capacitor C_{a} resembles a voltage source [15]. Due to dynamic capacitance limitations for C_{a}, the natural balancing quality is poor and further active control measures are required to enforce the desired time-varying voltage waveform of C_{fA} (cf. **Fig. 3a**). Hence, an additional FC voltage control block is added to regulate u_{fA} by slightly changing the duration of the redundant FC charging and discharging intervals by means of a correction duty cycle d_{cor} [16].

The resulting closed loop circuit simulation voltage and current waveforms for the 3L-FC-YR with an effective switching frequency of 200 kHz (i.e. switches operating with 100 kHz) are shown in **Fig. 5**. Sinusoidal grid currents can be realized, verifying the derived control structure where the transition from buck to boost operation (and vice versa) is completely seamless. Also, the FC voltages follow closely the desired voltage profile shown in **Fig. 3a** despite a substantial switching-frequency voltage variation.

IV. Critical Operating Conditions

System start-up is a critical operating condition for any FC converter [10] and it is crucial to maintain FC voltage balancing. The 3L-FC-YR phase module a with the passive protection circuitry necessary for a safe system start-up is depicted in **Fig. 6a**, where a precharging resistor R_{pr} (with a bypass switch T_{pr}) limits the input filter inrush currents when connecting the converter to the grid.

As the grid line-to-line voltage is impressed on the input terminals and since the antiparallel diodes of the stage A semiconductors prevent negative voltages u_{an} and u_{fA}, a minimum constant offset voltage $u_{\mathrm{CM}} = \hat{u}_{\mathrm{ac}}$ is naturally established. Hence a maximum input capacitor voltage $U_{\mathrm{an,max}} = 2 \cdot \hat{U}_{\mathrm{ac}}$ (e.g. $U_{\mathrm{an,max}} = 650\,\mathrm{V}$ for $\hat{U}_{\mathrm{ac}} = 325\,\mathrm{V}$) results. During the control system initialization (or also in failure mode) the semiconductors of stage A and B cannot be actively controlled and are disabled, hence the FC clamping strategy (cf. **Fig. 3**) cannot be performed and critical semiconductor blocking voltage stresses could result in stage A. Accordingly, the passive protection circuitry depicted in **Fig. 6a** further includes balancing capacitors C_{b} connected with normally-on switches T_{b} in parallel to the semiconductors T_{A1} and $T_{\mathrm{A1}}^{'}$. The capacitance value of C_{b} is selected such that equal AC voltage sharing results among the stage A semiconductors, while the antiparallel diodes also establish equal DC bias voltage sharing. Last, an additional normally-on semiconductor connects the switch-node of stage B to the negative DC-link rail in order to prevent an uncontrolled rise of U_{dc}. Note that all normally-on devices are deactivated in normal operation.

In case of an active load (e.g. a solar panel or an EV battery), U_{dc} has a nonzero voltage value after system initialization, and the 3L-FC-YR can directly start PFC operation with the control structure discussed in **Section III**. In contrast, for a passive load with initially $U_{\mathrm{dc}} = 0\,\mathrm{V}$ a special four-step start-up control strategy is required to ramp up the DC-link voltage in a controlled manner as presented in **Fig. 6b**: As soon as the power semiconductors can be actively controlled (**Step 1**), the pre-charging resistors are bypassed, the normally-on semiconductors T_{b} are disabled and the clamping modulation assures all FC voltages within safe boundaries. Note that during **Step 1** the clamping of C_{fA} is released when $u_{\mathrm{an}}(t) \geq U_{\mathrm{an,max}}/2 = \hat{U}_{\mathrm{ac}}$. During **Step 2**, the DC-link voltage is ramped up to the minimum value $U_{\mathrm{dc,PFC}}$ for PFC operation (e.g. $U_{\mathrm{dc,PFC}} = 50\,\mathrm{V}$) in discontinuous conduction mode and with non-sinusoidal

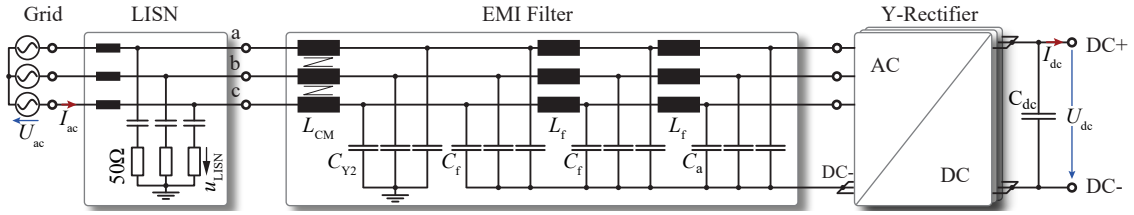

Fig. 7: Y-Rectifier (3L-FC-YR or 2L-YR) with an EMI input filter connected to the three-phase AC grid via a LISN, which allows to measure the EMI emissions.

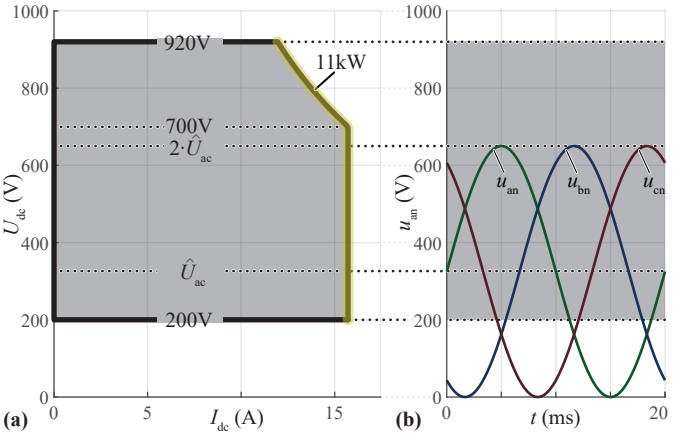

Fig. 8: **(a)** DC output voltage and current range according to the DC CCS HPC350 EV charging standard [1]: The current is scaled to a nominal power of 11 kW and the operating points considered for the performance evaluation are highlighted in yellow. **(b)** Input capacitor voltages $u_{\mathrm{an}}, u_{\mathrm{bn}}, u_{\mathrm{cn}}$ resulting for $\hat{U}_{\mathrm{ac}} = 325\,\mathrm{V}$.

grid currents. The stage B semiconductors T_{B1} and $T_{\mathrm{B1}}^{'}$ are permanently turned on and clamp C_{fB} to the DC-link, and T_{B2} as well as $T_{\mathrm{B2}}^{'}$ are turned off with their body diodes acting as diode bridge rectifier. The buck-stage A applies voltage pulses to the inductor L, while the clamping of C_{fA} is maintained. As soon as $U_{\mathrm{dc}} > U_{\mathrm{dc,PFC}}$, standard cascaded PFC control with sinusoidal grid currents is performed during **Step 3** and the DC-link voltage is further ramped up until steady-state operation (**Step 4**) at nominal DC voltage is reached.

V. Performance Evaluation

In the following, a comprehensive Pareto comparison [17] between the 2L-YR and 3L-FC-YR topology is conducted to identify the performance limits in power density ρ and efficiency η for an EV battery charger rectifier front-end connected to the European three-phase grid with $\hat{U}_{\mathrm{ac}} = 325\,\mathrm{V}$ (cf. **Fig. 7**) and complying with the CISPR 11 Class A EMI emission limits [18]. **Fig. 8a** presents the considered DC output voltage and current range according to the DC CCS HPC350 EV charging standard [1] with the nominal system power scaled to 11 kW. Nominal output power is provided from $U_{\mathrm{dc,max}} = 920\,\mathrm{V}$ to $U_{\mathrm{dc}} = 700\,\mathrm{V}$ and below a current limit of $I_{\mathrm{dc,max}} = 15.7\,\mathrm{A}$ applies. The resulting input capacitor voltages $u_{\mathrm{an}}, u_{\mathrm{bn}}, u_{\mathrm{cn}}$ for $\hat{U}_{\mathrm{ac}} = 325\,\mathrm{V}$ are also shown in **Fig. 8b**: Containing a constant offset voltage $u_{\mathrm{CM}} = \hat{U}_{\mathrm{ac}}$ the maximum input capacitor voltage is $U_{\mathrm{an,max}} = 2 \cdot \hat{U}_{\mathrm{ac}} = 650\,\mathrm{V}$ and accordingly DC output voltages $U_{\mathrm{dc}} \geq 650\,\mathrm{V}$ correspond to pure boost operation. In contrast, for DC voltage values $U_{\mathrm{dc}} < 650\,\mathrm{V}$, intervals of buck and boost operation result within one mains period.

In a first step, the degrees of freedom and design constraints of the power stage including the semiconductors as well as the buck-boost inductor L are discussed in **Section V-A**. Then, **Section V-B** presents the EMI emission mechanisms of the 3L-FC-YR and the 2L-YR, as well as the corresponding filter design to ensure compliance with the EMI emission limits. Given the wide DC output voltage range, the components of the power stage and the EMI filter are dimensioned for the respective worst-case operating point. The loss performance is then evaluated over the DC output voltage range U_{dc} and for the respective maximum output power according to the boundary of the operating range highlighted in **Fig. 8a**. Finally, the results of the performance comparison are presented in **Section V-C**.

A. Power Stage

The bridge-leg structure of the 2L-YR and the 3L-FC-YR is shown in **Fig. 9a** and **Fig. 9b**, respectively (the input capacitor C_{a} is attributed to the EMI filter and hence not shown). The top-level degrees of freedom in the realization of the power stage are the switching frequency f_{s} as well as the maximum relative inductor current ripple $\Delta I_{\mathrm{L,p.u.}}$ defining the required buck-boost inductor value L. For f_{s}, values from 24 kHz to 144 kHz, i.e. above the hearing threshold and up to the lower limit of the regulated CISPR frequency band are considered. The relative peak current ripple $\Delta I_{\mathrm{L,p.u.}} = \Delta I_{\mathrm{L,max}}/\hat{I}_{\mathrm{ac}}$ depends on the operating voltage range as well as the switching frequency and values from 25 % to 150 % are evaluated. Note that for a given switching frequency, an inductance value scaled by 1/4 for the 3L-FC-YR (with twice the effective switching frequency and half the voltage level amplitude) yields the same value $\Delta I_{\mathrm{L,p.u.}}$ as for the 2L-YR.

For a maximum DC output voltage of $U_{\mathrm{dc,max}} = 920\,\mathrm{V}$ Silicon Carbide (SiC) semiconductors with a voltage rating of 1700 V have to be employed in the boost-stages B of the 2L-YR to assure sufficient voltage margin for safe and reliable operation [19]. On the contrary, 900 V SiC devices with superior performance are applicable for the 3L-FC-YR. Aiming at a symmetric bridge-leg structure, the same semiconductors and switching frequency are employed in the buck-stage A

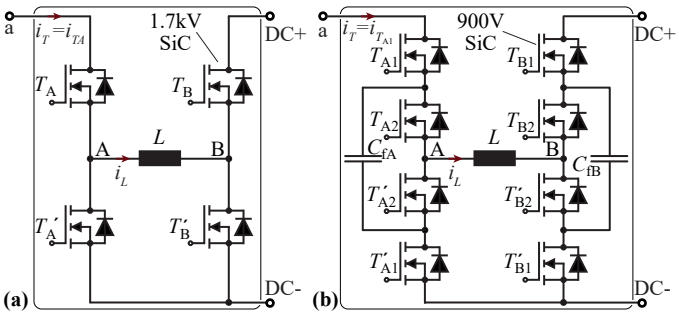

Fig. 9: Y-Rectifier phase-module structure for **(a)** 2L-YR and **(b)** 3L-FC-YR.

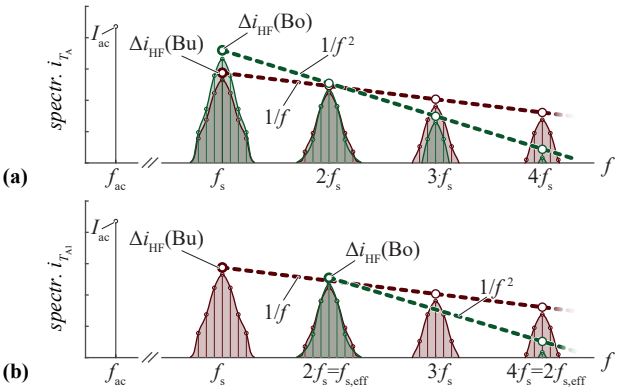

Fig. 10: Exemplary input current i_{T} (cf. **Fig. 9**) frequency domain spectrum of **(a)** 2L-YR and **(b)** 3L-FC-YR.

and the boost-stage B. This also allows to omit the 3L-FC-YR passive FC voltage balancing circuitry discussed in **Section IV**, as the $900\,\mathrm{V}$ SiC semiconductors can withstand the resulting blocking voltages even if the FC voltage balancing cannot be maintained during system initialization or failure. The semiconductor losses are assessed based on the $10\,\mathrm{m\Omega}$ $900\,\mathrm{V}$ (Cree third gen. C3M0010090K [20]) and the $45\,\mathrm{m\Omega}$ $1700\,\mathrm{V}$ (Cree second gen. C2M0045170P [21]) SiC semiconductors. Different numbers of parallel switches N_{par} are evaluated, where also values $N_{\mathrm{par}} < 1$ are considered to account for the availability of devices with higher on-state resistance (i.e. the semiconductor chip area is varied continuously for the power stage optimization). The required heatsink volume is approximated considering the worst-case semiconductor losses and a *Cooling System Performance Index* [22] $\mathrm{CSPI} = 20\,\mathrm{W}/(\mathrm{K}\cdot\mathrm{dm}^3)$. For the buck-boost inductor winding and core losses are evaluated for different core geometries and winding realizations according to [23].

B. EMI Filter

The goal of the EMI filter design is to attenuate the converter emissions below the CISPR 11 Class A QP limit values of $79\,\mathrm{dB\mu V}$ from $150\,\mathrm{kHz}$ to $500\,\mathrm{kHz}$, and $73\,\mathrm{dB\mu V}$ from $0.5\,\mathrm{MHz}$ to $30\,\mathrm{MHz}$, where an additional margin of $10\,\mathrm{dB}$ is considered to account for component tolerances and attenuation derating at high frequencies resulting for practical power components. The emissions are measured with a three-phase LISN (cf. **Fig. 7**) which decouples the converter from the grid for high frequencies $\geq 150\,\mathrm{kHz}$ and redirects high-frequency converter emissions to a $50\,\Omega$ receiver.

The Y-Rectifier is a hybrid voltage / current source converter topology, where the high-frequency components of the current of the buck-stage A upper most semiconductor i_{T} (i.e. $i_{\mathrm{T}} = i_{\mathrm{TA}}$ for the 2L-YR in **Fig. 9a** and $i_{\mathrm{T}} = i_{\mathrm{TA1}}$ for the 3L-FC-YR in **Fig. 9b**) is the most relevant quantity defining the EMI emissions and the required filter attenuation [24]: As can be seen in **Fig. 7**, in case of a theoretical absence of the EMI filter (including the input capacitor C_{a}), the high-frequency content of i_{T} would directly be flowing via the corresponding LISN resistors, hence causing a voltage drop u_{LISN} which may exceed the emission limits. For a $50\,\Omega$ LISN resistor, the voltage emission limit can be translated into a corresponding current limit, e.g. $45\,\mathrm{dB\mu A} = 79\,\mathrm{dB\mu V} - 34\,\mathrm{dB\Omega}$, which allows to assess the required filter attenuation for a given current i_{T}.

The high-frequency content of i_{T} varies during one mains period and depends on the converter operating mode, as a triangular current ripple results in boost operation with $i_{\mathrm{T}} = i_{\mathrm{L}}$, and a square-wave current in buck operation. The 2L-YR current spectrum of $i_{\mathrm{T}} = i_{\mathrm{TA}}$ is outlined in **Fig. 10a** for buck (red) and boost (green) operation and the emissions result around multiples of the switching frequency $n \cdot f_{\mathrm{s}}$. The high-frequency spectrum in boost operation (triangular current, approximately $-40\,\mathrm{dB/dec}$ [25]) decays faster with frequency compared to buck operation (square-wave current, approximately $-20\,\mathrm{dB/dec}$ [25]) due to the attenuation provided by the inductor L.

Then, the 3L-FC-YR current spectrum of $i_{\mathrm{T}} = i_{\mathrm{TA1}}$ is highlighted in **Fig. 10b**. Given the effective switching frequency $f_{\mathrm{s,eff}} = 2 \cdot f_{\mathrm{s}}$, boost (green) emissions result around multiples of $n \cdot f_{\mathrm{s,eff}}$. In contrast, the buck emissions (green) are defined by the operation of T_{A1}, and hence the spectrum results around multiples of the switching frequency $n \cdot f_{\mathrm{s}}$, where the decay rate with frequency is again lower compared to the spectrum for boost operation.

The maximum high-frequency RMS current Δi_{HF} over one switching period of i_{T} for both the 2L-YR and the 3L-FC-YR is approximately given by

$$\Delta i_{\mathrm{HF}} = \begin{cases} \hat{I}_{\mathrm{ac}} \sqrt{1/d_{\mathrm{A,min}} - 1} & \text{(Buck, at } f_{\mathrm{s}}\text{)} \\ \frac{1}{\sqrt{3}} \frac{1}{8} \frac{U_{\mathrm{dc}}}{f_{\mathrm{s}} L} \cdot \left(\frac{f_{\mathrm{s}}}{f_{\mathrm{s,eff}}}\right)^2 & \text{(Boost, at } f_{\mathrm{fs,eff}}\text{)}. \end{cases} \tag{1}$$

Note that in boost operation Δi_{HF} depends on the inductance value L, as well as the (effective) switching frequency f_{s} ($f_{\mathrm{s,eff}}$). The maximum value Δi_{HF} results for $U_{\mathrm{dc,max}}$ and a boost duty cycle $d_{\mathrm{B}} = 0.5$ for the 2L-YR and for the 3L-FC-YR with $d_{\mathrm{B}} = 0.25$. In contrast, assuming unity power factor and neglecting the high-frequency inductor current ripple, Δi_{HF} in buck operation is defined by the minimum buck duty cycle $d_{\mathrm{A,min}}$ within one mains period as well as the peak AC current $\hat{I}_{\mathrm{ac}}$, and does not depend on the power stage design parameters. For the considered DC operating range in **Fig. 8a**, the system output power (and accordingly the grid

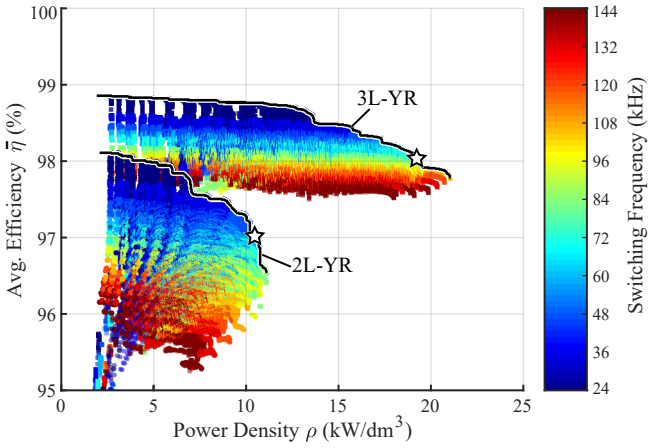

Fig. 11: $\bar{\eta}\rho$-Pareto front of the 3L-FC-YR and the 2L-YR for the realization of an 11 kW CISPR 11 Class A compliant EV battery charger rectifier front-end.

current $\hat{I}_{\mathrm{ac}}$) is reduced for voltages below $U_{\mathrm{dc}} = 700\,\mathrm{V}$ and hence the maximum value of Δi_{HF} results for $U_{\mathrm{dc}} = 325\,\mathrm{V}$ (i.e. $U_{\mathrm{dc}} = U_{\mathrm{an,max}}/2$ with $d_{\mathrm{A,min}} = 0.5$) and is given by $\Delta i_{\mathrm{HF}} = 10.5\,\mathrm{A_{rms}} \approx 140\,\mathrm{dB\mu A}$.

The high-frequency spectrum of the current i_{T} can be approximated as illustrated in **Fig. 10** by attributing Δi_{HF} to a single (effective) switching-frequency component and

$$\hat{i}_{\mathrm{T}}(n \cdot f_{\mathrm{s}}) = \frac{\Delta i_{\mathrm{HF}}}{n^k}, \tag{2}$$

where the spectrum decays with $k = 1$ in buck operation ($1/f$,$-20\,\mathrm{dB/dec}$) and $k = 2$ in boost operation ($1/f^2$, $-40\,\mathrm{dB/dec}$) [25]. Note that the boost 3L-FC-YR spectral components result at multiples of the effective switching frequency $n \cdot f_{\mathrm{s,eff}}$ (cf. **Fig. 10b**).

The required filter attenuation is then defined by the design frequency $f_{\mathrm{D}} = n_{\mathrm{D}} \cdot f_{\mathrm{s}}$ (or $f_{\mathrm{D}} = n_{\mathrm{D}} \cdot f_{\mathrm{s,eff}}$ for boost operation of the 3L-FC-YR) equal the first switching frequency harmonic n_{D} within the regulated emission band above 150 kHz. Note that for the 3L-FC-YR, the design frequency of buck- and boost-stage is not necessarily identical, e.g. for $f_{\mathrm{s}} = 72\,\mathrm{kHz}$, the design frequency is $f_{\mathrm{D}} = 3 \cdot f_{\mathrm{s}} = 216\,\mathrm{kHz}$ in buck operation and $f_{\mathrm{D}} = 2 \cdot f_{\mathrm{s,eff}} = 288\,\mathrm{kHz}$ in boost operation.

The EMI input filter optimization procedure considers DC-link referenced filter stages (cf. **Fig. 7**) attenuating both Differential Mode (DM) and Common Mode (CM) emissions [26]. A filter comprising a single capacitor C_{a} would require extremely high values of C_{a}, where the total capacitance per phase module is limited to 10 µF in order to avoid excessive capacitive currents and corresponding conduction losses. Accordingly, up to two additional LC filter stages are evaluated within the filter optimization process, where filter stages with identical component values are selected to minimize the filter volume [27]. A minimum separation between filter resonance frequencies and switching frequency by a factor of $3/2$ constrains the selection of filter component values to avoid exciting resonances in the EMI filter. Hence, for a switching frequency of e.g. 72 kHz, the filter resonance frequencies have to be below 48 kHz.

TABLE I: SELECTED DESIGNS

Performance	**2L-YR**	**3L-FC-YR**
Avg. efficiency $\bar{\eta}$	97.0 %	98.1 %
Pk. efficiency η_{max}	97.7 %	98.5 %
Power density ρ	11 kW/dm^3	19 kW/dm^3
Volume	1037 dm^3	572 dm^3
Power stage		
f_{s} / $f_{\mathrm{s,eff}}$	60 kHz / -	72 kHz / 144 kHz
R_{on} (Semi, $T_{\mathrm{j}} = 120\,^{\circ}\mathrm{C}$)	50 mΩ	17 mΩ
L $(\Delta I_{\mathrm{L,p.u.}})$	68 µH (125 %)	18 µH (100 %)
Core	N87 3 x E 47/20/16	N87 3 x E 32/16/9
Winding	14 turns	9 turns
	3 mm diam.	3 mm diam.
	75 µm litz wire	100 µm litz wire
C_{dc}	22 µF	18 µF
$C_{\mathrm{fA}} = C_{\mathrm{fB}}$	-	2 µF
EMI filter		
f_{D}	180 kHz	216 kHz
Min. attenuation at f_{D}	62 dB	62 dB
Attenuation at f_{D}	82 dB	84 dB
Topology	$LC - LC$	$LC - LC$
L_{f}	16 µH	10 µH
$C_{\mathrm{f}} = C_{\mathrm{a}}$	2.9 µF	3.3 µF

Aiming at an ultra-compact filter realization, $X7R$ ceramic capacitors [28] are considered. Also, in contrast to the buck-boost inductor L with substantial high-frequency stresses and losses, only the low-frequency conduction losses are relevant for the EMI filter inductors. Therefore, commercially available flat wire inductors are employed. The fundamental-frequency voltage and current stresses of the passive components are identical for the 2L-YR and 3L-FC-YR and defined by the operating range presented in **Fig. 8**. Hence the same set of filter components is applicable in both topologies and to realize a given filter attenuation.

Note that the DC-link referenced filter does not attenuate emissions resulting from the parasitic switch-node capacitances [24], which are estimated to 35 pF per semiconductor in a TO-247-4 package. Therefore, an additional filter stage comprising safety capacitors C_{Y2} to protective earth and a CM choke L_{CM} is required (cf. **Fig. 7**). However, according to [29] up to $C_{\mathrm{Y2}} = 240\,\mathrm{nF}$ can be employed while still complying with a ground current limit of 3.5 mA. Hence, a small CM choke in the range of $\approx$ 200 µH is sufficient to attenuate the emissions resulting from the switch-node capacitances and accordingly this additional filter stage is not included in the filter optimization procedure.

C. Results

Fig. 11 displays the performance limits of the 3L-FC-YR and the standard 2L-YR topology for the realization of an 11 kW CISPR 11 Class A compliant EV battery charger rectifier front-end. The average efficiency $\bar{\eta}$ results for operating points along the operating boundary highlighted in **Fig. 8a** and the power density values ρ were scaled by a factor of $3/4$ to account for the fact that in practice the resulting converter volume is larger than the sum of the boxed volumes of the individual components (i.e. assumed to be 75 % of the total converter volume)

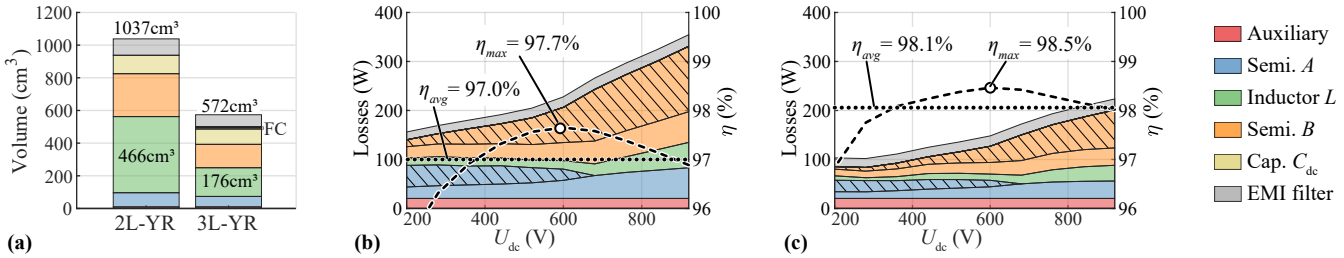

Fig. 12: Performance comparison of the designs highlighted with a star in **Fig. 11**: **(a)** converter volume distribution (scaled by a factor $4/3$), as well as system losses and efficiency of **(b)** the 2L-YR and **(c)** the 3L-FC-YR over DC output voltage and for the maximum output power according to **Fig. 8**. Semiconductor switching losses are represented by hatched areas and the design details are given in **Tab. I**.

Employing FC bridge-legs, power densities of up to $21\,\mathrm{kW/dm^3}$ (with $\bar{\eta} = 97.8\,\%$) can be achieved for the 3L-FC-YR, while the power density of the 2L-YR is limited to $11\,\mathrm{kW/dm^3}$ (with $\bar{\eta} = 96.6\,\%$). The scatter points indicate the design switching frequencies, and the maximum power densities of the 3L-FC-YR and the 2L-YR results for $f_\mathrm{s} = 108\,\mathrm{kHz}$ (i.e. $f_\mathrm{s,eff} = 216\,\mathrm{kHz}$) and $f_\mathrm{s} = 84\,\mathrm{kHz}$, respectively. For switching frequencies higher than these threshold values, the gain in filter volume is out-weighted by the additional switching losses and corresponding heatsink volume. As the 2L-YR employs semiconductors with higher voltage rating, the maximum switching frequency resulting in a Pareto-optimal result ($84\,\mathrm{kHz}$) is lower compared to the 3L-FC-YR ($108\,\mathrm{kHz}$).

Two designs are highlighted with a star in **Fig. 11** and the corresponding converter performance and specifications are summarized in **Tab. I**. The selected 3L-FC-YR design shows an average efficiency elevated by 1.1 percentage points and a converter volume reduction of $45\,\%$ compared to the 2L-YR. A detailed volume distribution is provided in **Fig. 12a**, where the buck-boost inductor L as well as the semiconductors (and the associated heatsink) are the main drivers of converter volume. Both systems employ a similar switching frequency (2L-YR with $60\,\mathrm{kHz}$ and 3L-FC-YR with $72\,\mathrm{kHz}$) and accordingly as discussed in **Section V-A**, a small value of L results for the 3L-FC-YR and enables a highly compact power inductor realization. Further, employing superior $900\,\mathrm{V}$ SiC semiconductors, smaller semiconductor on-state resistance values can be selected for the 3L-FC-YR ($17\,\mathrm{m\Omega}$ as compared to $50\,\mathrm{m\Omega}$ for the 2L-YR), while the switching losses remain tolerable.

Two additional LC filter stages attenuate the EMI emissions for the selected 3L-FC-YR and 2L-YR designs (cf. **Tab. I**). The required attenuation is identical for both topologies, as the design frequency f_D equals the third switching frequency harmonic, while a slightly lower filter crossover frequency (and hence larger filter) is required for the 2L-YR with a lower switching and design frequency. Given the specified minimum separation of filter resonance frequencies and switching frequency (cf. **Section V-B**), the selected component values yield a filter realization providing more than the minimum required emission attenuation for both topologies. As can be observed in **Fig. 12a**, the contribution of the EMI filter to the overall converter volume is small for both topologies, which is mainly due to the fact that ultra compact $X7R$ ceramic capacitors were considered for the filter realization.

The system performance is depending on the DC output voltage and current. **Fig. 12b** and **Fig. 12c** present the calculated converter losses and efficiencies for the selected 2L-YR and 3L-FC-YR design, respectively, over the DC output voltage range U_dc and for the maximum output power according to the boundary of the operating range highlighted in **Fig. 8a**. There, the switching losses (hatched areas) of the buck-stage A and the boost-stage B are highlighted separately from the conduction losses. Note that with increasing output voltage U_dc the system power increases linearly up to $700\,\mathrm{V}$ (due to operation with the maximum DC output current) where the nominal power of $11\,\mathrm{kW}$ is reached. The buck effort (cf. **Fig. 8**) and accordingly also the stage A switching losses decrease with increasing U_dc and for $U_\mathrm{dc} \geq U_\mathrm{an,max} = 650\,\mathrm{V}$ the buck-stage A is not switched within an AC period and accordingly no switching losses result, such that stage A only causes conduction losses. The peak efficiency results for both topologies in the vicinity of $U_\mathrm{dc} = 600\,\mathrm{V}$ and is equal to $\eta_\mathrm{max} = 97.7\,\%$ for the 2L-YR and $\eta_\mathrm{max} = 98.5\,\%$ for the 3L-FC-YR. For higher output voltages, the efficiency of both systems drops again due to the increasing switching losses, where the decrease in efficiency is less severe for the 3L-FC-YR.

VI. Conclusion

In this paper, aiming at evermore compact and efficient AC/DC buck-boost converter realizations for applications such as EV chargers, the circuit structure and operating principle of a new Three-Level Flying Capacitor Y-Rectifier (3L-FC-YR) is introduced. The required modulation and control strategies necessary for safe and performant operation are derived and verified by means of closed-loop circuit simulations. Critical operating conditions are discussed and a passive voltage balancing circuit is proposed. A performance comparison between the proposed 3L-FC-YR and the standard 2L-YR by means of an $\bar{\eta}\rho$-Pareto optimization reveals that the 3L-FC-YR allows to reduce the converter system volume by $45\,\%$, while the average system efficiency can be increased by $1.1\,\%$ (i.e. losses relative to system input power are reduced by $35\,\%$ on average). The high performance of the 3L-FC-YR is mainly enabled by the elevated switching frequency and the higher number of voltage levels, allowing a massive volume reduction

of the buck-boost inductor, as well as the superior performance of SiC semiconductors with lower rated voltage.

The results indicate the feasibility of an ultra-compact CISPR 11 Class A compliant 3L-FC-YR prototype covering a wide DC output voltage range of $200\,\mathrm{V}$ to $920\,\mathrm{V}$ and featuring a power density of $19\,\mathrm{kW/dm^3}$ ($311\,\mathrm{W/in^3}$) and a peak efficiency of $98.5\,\%$.

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