Multi-Level Topology Evaluation for Ultra-Efficient Three-Phase Inverters

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***Abstract*—Multi-level topologies reduce the requirements on inductors and filters, however, given the high number of series connected semiconductors, it is still unclear if they are a suitable option to achieve ultra-high efficiency while maintaining a reasonable power density. For this purpose, an extensive quantitative evaluation of different topologies is carried out, to determine the required volume for a targeted 99.5 % efficiency of a 10 kW three-phase inverter. This includes the EMI noise filtering, where the Common Mode filter is placed on the DC-side to save losses and the impact of the upcoming EMI regulations covering the range from 2 kHz to 150 kHz is discussed. With an evaluation of multi-level topologies, it is shown that even if a high number of levels can reduce the size of the magnetic components by an order of magnitude, the volume and losses of the capacitive components required to create the multi-level voltage output have to be considered. An evaluation is done to quantify the performance of topologies ranging from two-level to seven-level topologies, and detailed designs of the three-level T-type and seven-level Hybrid Active Neutral Point Clamped converters are presented, achieving a relatively high power density of 2.2 kW/dm^3 and 2.7 kW/dm^3 respectively.**

I. Introduction

There is currently a strong trend in power electronics for improving efficiency and power density [1]. This is especially true for grid connected converters such as telecom rectifiers, photovoltaic (PV) inverters and Uninterruptible Power Supply (UPS) systems, where for the latter typically a back-to-back connection of a rectifier and inverter stage of the same topology is used. The introduction of the three-level T-type topology allowed significant performance improvement using Si-IGBTs compared to the formerly used two-level approach [2], since the switching losses are reduced by switching only half of the DC-link voltage, and the volume of the magnetic components decreases due to the three-level voltage characteristic. This was later improved with the commercialization of 1200 V SiC MOSFETs and diodes which reduced conduction losses, i.e. are not showing a current independent voltage drop. This allowed to reach efficiencies of up to 99 % using simpler two-level topologies for inverter stages with relatively high peak power densities [3], which is important since the maximum weight that a single person is allowed to handle is limited by regulation (e.g. to 25 kg in Switzerland [4]). In a next step, with new semiconductor technologies available (e.g. 650 V and 900 V SiC devices and GaN technology), it has to now be determined whether efficiencies well above 99 % can be achieved while keeping a relatively low volume, and if so, what is the most effective technology. In this context, although

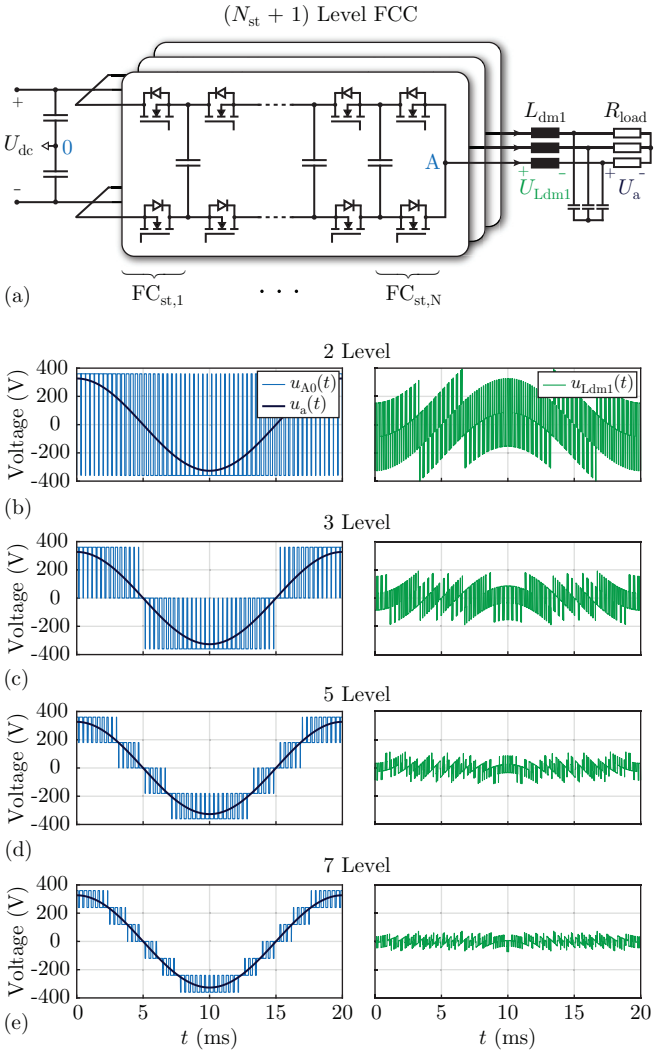

Fig. 1. A three-phase (N_{st}+1) level Flying Capacitor Converter (FCC), with N_{st} FC stages (a). FCC output node voltage referenced to the DC-link midpoint $u_{A0}(t)$ and the filtered output voltage $u_a(t)$ (left), and the first stage DM inductor voltage (right) considering a CM filter or a floating neutral point of the load (b-e). Note, that for a clear representation, the switching frequency is chosen for each case such that the effective frequency of the voltage waveform applied to the inductor is only 3 kHz.

multi-level converters have been widely used for high- and medium-voltage applications [5], recently the Flying Capacitor Converter (FCC) has been proposed for lower voltage PV applications [6]. These use low-voltage, industry-qualified and

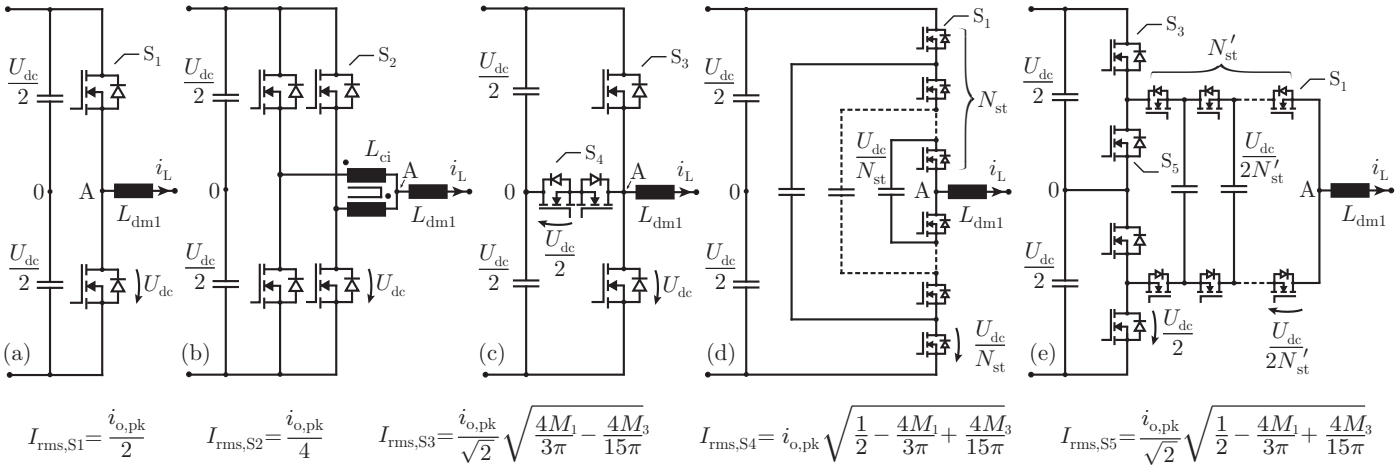

Fig. 2. Bridge leg topologies considered in the evaluation, shown for a single phase. (a) Two-level converter, (b) two-level interleaved converter with a CI, (c) three-level T-type converter, (d) the $(N_{\mathrm{st}}+1)$-level FCC and (e) the $(2N'_{\mathrm{st}}+1)$-level HANPC converter. The RMS currents for the different switches are also shown, where the duty cycle is $D = M_1 \cdot \sin(wt) + M_3 \cdot \sin(3wt)$, M_1 is the modulation index, M_3 is the amplitude of the superimposed third harmonic injection and $i_{\mathrm{o,pk}}$ is the peak output current.

low-cost (compared to SiC) Silicon MOSFETs, and obtain a significantly higher amount of levels, i.e. 5,6,7..., substantially minimizing the volume of the inductive components. For the Google Little Box Challenge, a FCC based 2 kW inverter with GaN technology achieved a power density of 13.2 kW/dm^3 (216 W/in^3) at 97.6 % peak efficiency [7].

However, it is still unclear how much of a benefit this new multi-level approach allows for ultra-efficient applications, since the conduction losses increase (more devices in series in the conduction path), but the switching losses and the volume of the magnetic components are reduced due to lower voltage switching and the staircase output voltage envelope of the converters, as shown in Fig. 1. Therefore, the topic of this paper is to quantitatively analyze, on the one hand, the classic two- and three-level topologies, where the interleaving of two-level bridge legs is considered (in order to achieve a three-level characteristic), and on the other hand, the multi-level approaches of the FCC and the Hybrid Active Neutral Point Clamped (HANPC) converter concepts [8]. In Section II the evaluated topologies to reach the efficiency target are introduced, followed by Section III, where the framework and results of the topology comparison are shown. Then, a detailed 3D CAD model of the three-level T-type converter and the seven-level HANPC converter with the corresponding loss and volume distributions is presented in Section IV, and in Section V the impact of upcoming EMI regulations for the frequency range between 2 kHz and 150 kHz is analyzed. Finally, in Section VI the main results of the paper are summarized.

II. Evaluated Topologies

The considered topologies to achieve the efficiency target of 99.5 % are presented in Fig. 2, together with the RMS currents of the switches for Continuous Conduction Mode (CCM). The specifications for the converter are given in Table I.

TABLE I
Converter specifications.

Efficiency Target	99.5 %
P_{rated}	10 kW
$P_{\mathrm{rated,max}}$	12.5 kW
U_{dc}	720 V
$U_{\mathrm{ac,ll,rms}}$	400 V_{rms}
f_{mains}	50 Hz
EMI Filter Requirement	Class A

A. Two- and Three-Level Converters

Two- and three-level topologies are the conventional solutions for three-phase converters [2,3,9]. In this context, the standard two-level, two-level interleaved and three-level T-type converter are considered, as shown in Fig. 2(a-c). Their common characteristic is that they all use switches that have to be rated to block the full DC-link voltage, and hence, semiconductors in the 1200 V range are required. The two-level interleaved topology offers a three-level output voltage $u_{\mathrm{A0}}(t)$ with the insertion of an additional magnetic component, i.e. a Coupling Inductor (CI). In the case of the three-level T-type converter, the third level is achieved by inserting two additional switches towards the midpoint, which advantageously only have to block half of the DC-link voltage. Although both the two-level interleaved and T-type bridge legs achieve three-level output voltage waveforms, the latter only hard-switches half of the DC-link voltage, whereas the former switches the full DC-link voltage.

B. Multi-Level Converters

To asses the potential of multi-level converters for high-efficiency applications, two topologies are taken into account: the FCC and the HANPC converter, whose bridge leg schematics are shown in Fig. 2(d) and (e), respectively. In the case of the FCC, all of the switches are rated to block the same voltage, namely $\frac{U_{\mathrm{dc}}}{N_{\mathrm{st}}}$, where N_{st} is the number of FC stages. For the

HANPC converter, half of the FC stages are saved by inserting four switches that have to block half of the DC-voltage and switch at mains frequency (S_3 and S_5 in Fig. 2), that can be considered to be lossless from a switching loss point of view. Furthermore, the saved FC stages are the ones with the highest capacitor voltage rating, which is favorable from a volume perspective. For the same number of output levels as a FCC, the low voltage switches of the HANPC converter have the same blocking voltage requirement as the FCC. In both topologies, it is the low-voltage semiconductors that are switching at switching frequency. Both of these converters are expandable to a higher number of levels, by adding additional FC stages. The FCC is considered for three, five and seven levels, whereas the HANPC converter is considered for five and seven levels. The choice of the levels is taken in accordance to the semiconductor availability, since for instance the lack of competitive MOSFETs in the 350-400 V range directly rules out a four-level solution for the FCC.

III. Topology Comparison Methodology and Results

A. Loss Distribution

The first step of designing an ultra-high efficiency converter is to allocate the loss budget for each of the main loss sources, which are the semiconductor conduction losses, switching losses and magnetic component losses [10]. For such high efficiency targets, paralleling switches has to be considered to reduce the conduction losses. To find an optimal loss distribution between the conduction and switching losses of the semiconductors, the minimum switching losses for a symmetric half-bridge with the same devices can be expressed as [11]

$$\begin{aligned} P_{\text{sw}} &= N f_{\text{sw}} Q_{\text{oss}}(V_{\text{n}}) V_{\text{n}} + f_{\text{sw}} Q_{\text{rr}}(I_{\text{sw,avg}}) V_{\text{n}} \\ &= N f_{\text{sw}} C_{\text{oss,q}}(V_{\text{n}}) V_{\text{n}}^2 + f_{\text{sw}} Q_{\text{rr}}(I_{\text{sw,avg}}) V_{\text{n}} \ , \end{aligned} \tag{1}$$

where N is the number of switches in parallel, f_{sw} is the switching frequency, V_{n} is the switched voltage, $Q_{\text{oss}}(V_{\text{n}})$ is the voltage dependent output capacitance charge of the switch, $C_{\text{oss,q}}(V_{\text{n}})$ is voltage dependent charge equivalent output capacitance of the switch, Q_{rr} the reverse recovery charge, and $I_{\text{sw,avg}}$ the average switched current. The reverse recovery losses are in a first step considered to be linear with the switched current and independent of the number of devices in parallel [12]. For ultra-high efficient applications, where each MOSFET switches a low current, the Q_{oss}-related losses account for the largest amount of the losses. In [13] it can be seen that for $I_{\text{sw,avg}} = 6.5\,\text{A}$, which is the average switched current per switch for a 10 kW three-phase half-bridge with two parallel switches, the losses caused by Q_{oss} can account for up to 80 % of the total switching losses, depending on the utilized gate driver resistance. If the conduction losses are modelled as

$$P_{\text{cond}} = I_{\text{rms}}^2 R_{\text{ds,on}} / N \ , \tag{2}$$

with I_{rms} the RMS current of the switch and $R_{\text{ds,on}}$ its on-state resistance, the optimum number of parallel switches N for a symmetric half-bridge can be found [14]. Assuming $Q_{\text{oss}}(V_{\text{n}}) \gg Q_{\text{rr}}$, which is valid for GaN (no reverse recovery effect) and SiC devices switching low currents, leads to an optimum semiconductor loss of

$$P_{\text{sw}} \simeq P_{\text{cond}} \ . \tag{3}$$

Since a part of the total converter loss budget has to be reserved for additional power losses in the converter (P_{others}), such as control, PCB conduction and connectors, and these losses are estimated to be around 12 W [10,15], it is decided for the comparison to distribute the losses in such a way that P_{others} =12.5 W (25 %), $P_{\text{sw}} \geq P_{\text{cond}}$, where 75 °C junction temperature of the MOSFETs is assumed for the conduction losses, and the ratio between the semiconductor losses and the losses of the magnetics is varied to find the optimum loss distribution.

B. EMI Filter Stage

1) DM Filter: To define the filter inductance and capacitance values, the first constraint that the EMI filter has to comply with is the International Special Committee on Radio Interference (CISPR) 11 Class A standard, for which a minimum attenuation Att is required to fulfill the quasi-peak and average limits. Taking the same values of the filter components for all the filter stages in order to achieve maximum attenuation in a first step ($L = L_k$ and $C = C_k$ for both Differential Mode (DM) and Common Mode (CM) noise) [16], the asymptotic attenuation provided by an N_{f} stage filter is $Att = (\omega T_{\text{c}})^{(2N_{\text{f}})}$, where $T_{\text{c}} = \sqrt{LC}$ is the filter time constant of the individual stage. Additionally, a 6 dBµV margin is included to accommodate the CM noise, together with a 10 dBµV that considers the tolerances of the components. The second constraint that the EMI filter has to fulfill is to have resonance frequencies which are far from the switching frequency and its harmonics. For this, the filter cut-off frequency is chosen to be at maximum one fourth of the switching frequency, for which a minimum filter time constant remains, $T_{\text{c,min}} = 4/(2\pi f_{\text{sw}})$. If the value of T_{c} obtained from the EMI compliance requirement is smaller than $T_{\text{c,min}}$, then the filter time constant is set to $T_{\text{c}} = T_{\text{c,min}}$. For the topology comparison, the same filter time constant T_{c} is considered for all of the filter stages. To determine the number of filter stages, since the volume of capacitors and inductors are proportional to the stored energy, $\sum L$ and $\sum C$ should be minimized [16]. For filter stages limited by the cut-off frequency, a minimum number of filter stages is desired for minimum volume, and hence, the number of filter stages N_{f} is determined by selecting the lowest number of filter stages that fulfill the required attenuation.

For the design of the DM filter, since the reactive power Q that a converter should process is limited (here $Q_{\text{max}} = 5\% P_{\text{rated}}$ is considered), the total maximum DM capacitance value per phase is given by

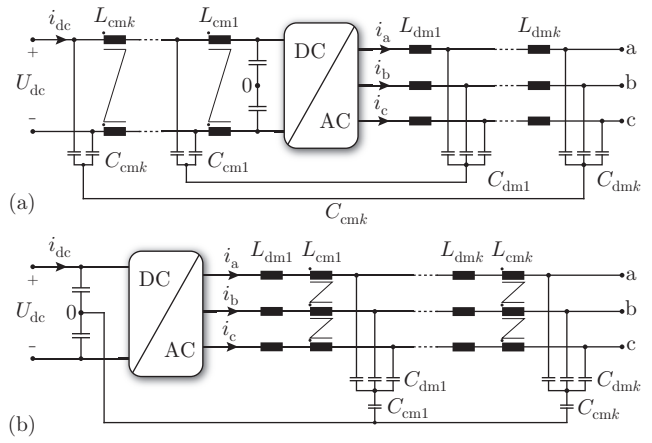

Fig. 3. DC-side CM filtering, with capacitive feedback from the star-point of the DM capacitors to the positive and negative rail of the DC-link (a), and AC-side CM filtering with capacitive feedback to the DC-link midpoint (b).

$$C_{\mathrm{dm,tot,max}} = \frac{Q_{\max}}{2\pi f_{\mathrm{mains}} U^2_{\mathrm{ac,ll,rms}}} \ , \tag{4}$$

which defines a minimum DM inductance value $L_{\mathrm{dm,min}}$. The output inductor L_{dm1} is then optimized for minimizing losses, with the constraint of achieving a minimum inductance value of $L_{\mathrm{dm,min}}$. For the inductor optimization, nanocrystalline cut-cores with helical windings are used, since they offer low core losses and high filling factor, and are suitable for applications with low current ripple [15,17]. The dimensions of a F3CC06.3 core are scaled linearly to calculate the losses until the allocated losses for the magnetic components are met.

2) CM Filter: To save losses, the CM choke is placed on the DC-side (cf. Fig. 3(a)) instead of the AC-side (cf. Fig. 3(b)). The magnetic core losses for both placements are equal, since the CM noise generated by the converter is the same, and hence, so is the applied voltage to the CM choke. However, the winding losses can be substantially reduced. By defining the modulation index as $M_1 = \frac{u_{\mathrm{ac,pk}}}{U_{\mathrm{dc}}/2}$, where $u_{\mathrm{ac,pk}}$ is the peak output phase voltage (325 V), the relationship between the DC input current I_{dc} and the output RMS phase current $I_{\mathrm{ac,rms}}$ is given by

$$I_{\mathrm{dc}} = \frac{3M_1}{2\sqrt{2}} I_{\mathrm{ac,rms}}. \tag{5}$$

(the DC current i_{dc} is assumed approximately constant, $i_{\mathrm{dc}} \approx I_{\mathrm{dc}}$, as filter capacitors are placed at the input of the switching stage). For the same CM choke core size, where the total copper conductor cross section and average turn length are assumed to be the same for both a DC- and AC-side CM choke placement, the ratio of the low-frequency winding losses is

$$\frac{P_{\mathrm{w,dc}}}{P_{\mathrm{w,ac}}} = \frac{M_1^2}{2} \ , \tag{6}$$

which for the nominal operating point of the converter ($M_1 = 0.904$) yields minimum winding loss savings of 60 %. Additionally, the eddy current and proximity losses are negligible for the DC-side choke placement, since in steady-state balanced operation the only high-frequency current flowing through the windings is the CM current, which is in the order of magnitude of the tens or low-hundreds of milliamperes. However, if the CM choke is placed on the AC-side, at least the first stage CM choke is going to have the same current ripple as the first stage DM output inductor L_{dm1}, leading to additional high frequency winding losses. For the design of the CM filter, the CM choke is also optimized for minimum losses. Finally, C_{cm} is adapted to satisfy the required attenuation for the CM noise.

C. Flying and DC-Link Capacitors

There are two additional sets of capacitors that have to be dimensioned. For the FCs, the minimum capacitance is defined by

$$C_{\mathrm{FC,min}} \geq \frac{I_{\mathrm{ac,pk}}}{(N_{\mathrm{levels}} - 1)\, f_{\mathrm{sw}}\, \Delta U_{\mathrm{fc,max}}} \ , \tag{7}$$

where $I_{\mathrm{ac,pk}}$ is the amplitude of the output phase current at maximum power output, and $\Delta U_{\mathrm{fc,max}}$ is the peak-to-peak switching frequency maximum voltage ripple of the FCs. For this work, $\Delta U_{\mathrm{fc,max}}$ is set to a maximum of 5 V, which allows a maximum switching frequency over-voltage on the switches to be of only 10 V during steady-state operation, which is low enough also for switches in the 200-250 V range that are operating in the vicinity of two thirds of their rated blocking voltage. Since the switching frequency imposed by the efficiency target is low, the required capacitance values are relatively large (tens of µF), hence rendering film capacitors as the most adequate option for the FCs. In [7] for instance, ceramic capacitors are used for the FCs, but the switching frequency of each device is one order of magnitude higher (120 kHz), and the power rating, and hence maximum peak current are lower (2 kW single-phase). For the case of the DC-link capacitors, only the capacitance needed to filter the switching frequency ripple current is taken into account in the comparison, since this has to be done by film capacitors due to the higher losses of aluminum-electrolyte capacitors. The minimum capacitance of the DC-link is determined by

$$C_{\mathrm{DC,min}} \geq \frac{I_{\mathrm{dc}}}{2 f_{\mathrm{sw}} \Delta U_{\mathrm{dc,max}}} \tag{8}$$

which is also limited for the comparison to $\Delta U_{\mathrm{dc,max}}$ =5 V. This limitation does not cover the low frequency (150 Hz) voltage ripple in the midpoint of the DC-link for the three-level T-type and the HANPC topologies, as this can be balanced by superimposing a third harmonic component to the modulation. Neither is any additional capacitance for potential grid unbalances considered.

D. Cooling and PCB Volume

To model the volume of the heat sink, a conservative Cooling System Performance Index (CSPI) of 3 W/(K·dm^3) is assumed [18]. For highly efficient systems, low CSPI values

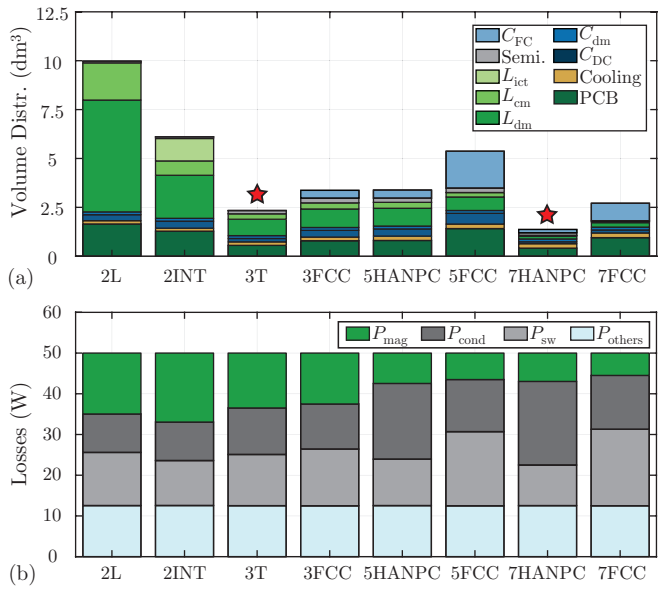

Fig. 4. Total volume distribution (a) and optimal power loss distribution for each topology resulting in a minimum converter volume (b). The number of switches, switching frequency, number of EMI filter stages and semiconductor technology of each converter is shown in Table III.

are obtained, firstly due to the large semiconductor area that has to be attached to the heat sinks (cf. Fig. 5), and secondly, because the selected fans are low power consumption fans, in the $<$1 W range. This CSPI value is additionally in accordance to the realized designs presented in Fig. 5. The maximum thermal resistance of the cooling system is set by the maximum temperature that the heat sink is allowed to reach. Taking 30 °C as the ambient temperature and 75 °C as the maximum allowable heat sink temperature (to limit MOSFET conduction losses) leads to the maximum thermal resistance from the heat sink to the air to be between 2.2 K/W for the two-level interleaved converter (with the lowest semiconductor losses) and 1.4 K/W for the seven-level HANPC converter (that has the maximum semiconductor losses). This finally yields the minimum volume of the cooling system to be between 0.15 dm^3 and 0.24 dm^3, which is assumed to be proportionally distributed over the semiconductor area for the volume computation of the comparison. When considering the boxed volume of converters, the volume of the PCB with all of its components on it (e.g. control board, current sensors and connectors) is taken into account, for which the surface of the main power components is modeled and a 15 mm height offset is included for calculating the PCB volume.

E. Comparison of Results

The results of the topology evaluation, with all of the converters designed to achieve a target efficiency of 99.5 % are presented in Fig. 4, where the total estimated minimum volume of the converters is shown together with the optimal loss distribution. The considered switches are given in Table II, and the number of paralleled devices, switching frequencies and the number of filter stages are presented in Table III.

TABLE II
SEMICONDUCTOR DEVICES USED FOR THE TOPOLOGY EVALUATION.

U_{rated}	Model	$R_{ds,on}$ (typ., 25 °C)	Technology
1200 V	C2M0025120D	25 mΩ	SiC
650 V	SCT3022AL	22 mΩ	SiC
250 V	IPB200N25N3	17.5 mΩ	Si
200 V	EPC2034	7 mΩ	GaN

For the two-level topology, the two-level voltage output and the low switching frequency lead to large inductor requirement. However, to understand the volume difference of the two-level conveter with respect to the rest of the converters, the scaling law between the power losses and the volume of an inductor have to be analyzed [14]. For a certain inductance value L, current ripple Δi_L, magnetic core cross section A_{core}, and number of turns N_t, the flux density ripple is given by

$$\Delta B = \frac{L\Delta i_L}{N_t A_{core}} \propto \frac{U_L}{f_{sw} A_{core}} \propto \frac{1}{A_{core}} \propto \frac{1}{l^2} \tag{9}$$

where l is the linear dimension. If this is then used for the Steinmetz equation, the core losses are

$$P_{core} \propto V_{core} \Delta B^{\beta} f_{sw}^{\alpha} \propto \frac{l^3}{l^{2\beta}} \propto\Big|_{\beta=2} \frac{1}{l}\ , \tag{10}$$

with V_{core} the volume of the magnetic core and α and β the Steinmetz paremeters. For the winding losses, neglecting the high frequency effects,

$$P_w = i_{L,rms}^2 R_w \propto i_{L,rms}^2 \frac{l}{\kappa A_w} \propto \frac{l}{l^2} \propto \frac{1}{l} \tag{11}$$

with $i_{L,rms}$ the RMS current of the inductor, R_w the resistance of the windings, A_w the cross section of the conductor, and κ the conductivity. Hence, it is seen that in a very rough approximation the losses of an inductor are inversely proportional to its linear dimension. This is further confirmed in the analysis done in [19], where it is shown that for sinusoidal currents and $\beta = 2$ an optimization for minimum power losses results in,

$$P_L \propto V_L^{-\frac{1}{3}} \propto \frac{1}{l}\ , \tag{12}$$

where V_L is the inductor volume. This means, that unless the output inductor L_{dm1} is limited by saturation (which in this comparison is not the case for the two- and three-level topologies), to half the inductor losses an $\approx$ 8x larger volume is needed. Hence, since the two-level converter exhibits the largest inductor requirement, Eq. (12) penalizes it the most, leading its total volume to be substantially larger than e.g. for the three-level converters.

In the case of the two-level interleaved converter, the CIs reduce the requirement on the first EMI filter stage by providing a three-level voltage output and higher effective switching frequency, however, the losses of the CIs have to be included into the available loss budget for the magnetics. For these two level bridge leg converters, the modulation scheme used was to clamp the lowest voltage to the negative DC-rail for one third

TABLE III

NUMBER OF SWITCHES OF EACH VOLTAGE RATING USED IN PARALLEL, THE SWITCHING FREQUENCY f_{sw}, THE EFFECTIVE SWITCHING FREQUENCY FOR THE FIRST STAGE EMI FILTER INDUCTORS $f_{sw,eff}$, AND THE NUMBER OF FILTER STAGES TO COMPLY WITH CISPR 11 CLASS A REGULATIONS.

	2L	2L-INT	3L-T-type	3L-FCC	5L-HANPC	5L-FCC	7L-HANPC	7L-FCC
N_{sw} 1200 V	2	2	2	-	-	-	-	-
N_{sw} 650 V	-	-	2	3	2 (S_3) & 1 (S_5)	-	2 (S_3) & 1 (S_5)	-
N_{sw} 250 V	-	-	-	-	4	5	-	-
N_{sw} 200 V	-	-	-	-	-	-	2	3
f_{sw}	17.2 kHz	14.5 kHz	30.4 kHz	15.2 kHz	14.2 kHz	9.5 kHz	54.9 kHz	34.4 kHz
$f_{sw,eff}$	17.2 kHz	29.0 kHz	30.4 kHz	30.4 kHz	28.4 kHz	37.9 kHz	164.7 kHz	206.7 kHz
# Filter Stages	2	2	2	2	2	2	3	3
Semicond. Technology	SiC	SiC	SiC	SiC	SiC & Si	Si	SiC & GaN	GaN

of the output period [20], i.e. two phases (instead of three) are switching simultaneously to save switching losses.

The three-level T-type converter offers good performance, since it provides a third output voltage level without inserting more passive energy storage components in the system, leading to a reduced size of the filter inductors compared to the two-level bridge leg variants, and without the need of inserting bulky film capacitors, as is the case for all of the FC-based topologies. This can be observed when comparing the three-level T-type to the three-level FCC, where the volume of the magnetics is similar, but the total volume difference is due to the additional FCs that are needed to create the three-level voltage output.

For the five-level converters, the volume of the FCs is large due to the low switching frequencies. The fact that the capacitance requirement for all FC voltage levels is the same and that higher voltage capacitors have larger volumes penalizes the five-level FCC, given that it needs FCs at 540 V, 360 V and 180 V, whereas the five-level HANPC converter only needs FCs at 180 V.

The seven-level converters offer a comparably higher switching frequency of each stage due to the high-performing low-voltage GaN semiconductors, and yield the highest effective switching frequency on the first filter stage (≈ 4x higher than the five-level converters). This reduces the volume of the magnetics drastically, however, for the seven-level FCC the volume of the capacitors is large, with five FC stages distributed equally between 600 V and 120 V.

In case the efficiency constraint would be relaxed from 99.5 % to 99.0 %, the two-level converter would be the one that gains most in performance, reducing its volume fivefold, compared to a threefold volume reduction of the two-level interleaved converter and a twofold reduction of the three- and five-level converters.

Finally, if the voltage ripple constraint of the FCs, $\Delta U_{fc,max}$, would be relaxed from 5 V to 10 V, which would mean a worst-case 20 V steady-state overvoltage on a FC switching stage, the volume of the FCs could be reduced by up to 50 %.

IV. DETAILED DESIGN OF THE SELECTED TOPOLOGIES

The analysis done in Section III serves the purpose of identifying the best performing topologies for the efficiency target at hand. In order to have a better understanding of the achievable power density, the converters have to be designed in more detail. Having identified the three-level T-type and the seven-level HANPC converters as suitable candidates, in a next step both of them are modeled with 3D CAD software, and presented in Fig. 5. The relevant component values of both designs can be found in Table IV.

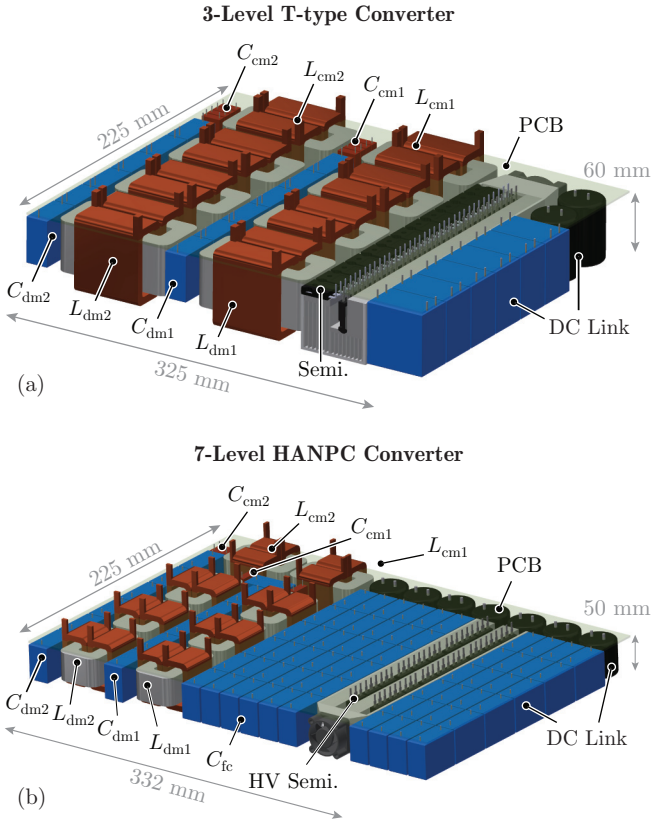

Fig. 5. 3D CAD illustrations of the three-level T-type converter (a) and seven-level HANPC converter (b).

The first step to design the converters is to account for additional switching losses, since the switching loss model presented in Section III-A only considers the minimum and unavoidable switching losses. Due to the channel of the semiconductor not closing infinitely fast, there are additional switching losses that will occur, and a sufficient margin of

TABLE IV
FINAL PARAMETERS OF THE TOPOLOGIES SHOWN IN FIG. 5.

	3-Level T-type	7-Level T-type
f_{sw}	20 kHz	20 kHz
$f_{sw,eff}$	20 kHz	60 kHz
L_{dm}	166.3 µH Nanocrystalline Core: F3CC0040 3 Distr. Airgaps in L_{dm1}	30.8 µH Nanocrystalline Core: F3CC06.3 1 Airgap in L_{dm1}
C_{dm}	6.6 µF	4.4 µF
C_{fc}	-	60 µF
C_{dc}	60 µF	60 µF

60 % has been added to the minimum losses [13,21]. Since the switching frequency is reduced by considering additional switching losses, for the seven-level HANPC to have an optimal semiconductor loss distribution (cf. Eq. (3)) a third low voltage MOSFET is introduced in parallel to reduce the conduction losses. Since both topologies have a midpoint connection, a 150 Hz ripple on the midpoint voltage arises. Although this effect can be avoided by employing third harmonic modulation, further capacitance is added to the DC-link, for which aluminum-electrolyte capacitors are placed in the available space of the DC current path of the converters, parallel to the foil capacitors and with a small inductance in series (bridged by a damping resistor) to avoid HF current losses. Note, that in the seven-level HANPC converter, the low voltage switches would be placed on the PCB area above the FCs.

The loss distributions presented in Fig. 6(a) for the final designs are in close accordance to the ones obtained from the topology comparison. Both of the designs have 15-16 % (7.5 W) of loss margin left for the PCB tracks and connectors amongst others. Due to the additional considered switching losses, for a 20 kHz operation of the seven-level HANPC converter a two-stage EMI filter is superior to the three-stage filter resulting from the topology comparison (Table III). In addition, for the seven-level HANPC converter the losses occurring in the foil capacitors cannot be neglected, as they account up to 5 % of the loss budget.

From the power density perspective, the seven-level HANPC converter is superior to the three-level T-type converter (2.7 kW/dm^3 vs. 2.2 kW/dm^3), however, the relative volume difference between both converters decreases from 70 % that results from the theoretical comparison to only 21 % in the 3D CAD design. This results mainly from the difference between the linear addition of the boxed volumes of individual components and the final 3D design of the converter. For the volume calculation, it is also assumed here that a space with a height of 15 mm above the PCB is required to accommodate the control board, the measurement devices, the auxiliary power circuitry and the connectors amongst others.

V. UPCOMING EMI LIMITS: 2 KHZ - 150 KHZ RANGE

Commonly used EMI emission limits for the frequency range from 150 kHz to 30 MHz are given in [22] for Industrial, Scientific and Medical (ISM) devices, however, there has been no clear standard that regulates the frequency range from 2 kHz

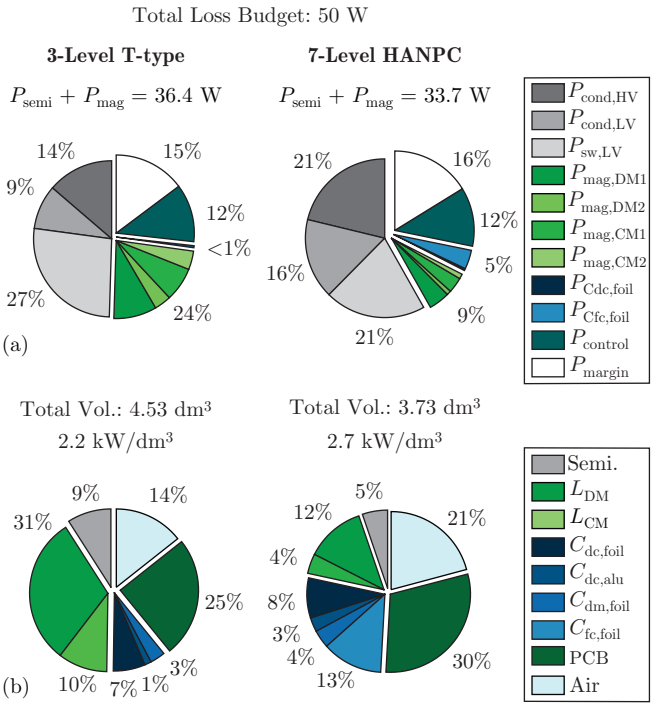

Fig. 6. Loss distribution (a) and volume distribution (b) of the three-level T-type converter (left) and seven-level HANPC converter (right).

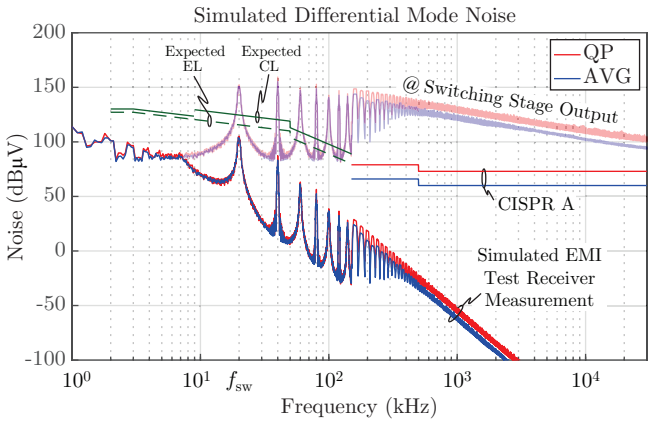

Fig. 7. Expected future Compatibility Level (CL) and Emission Level (EL) for the range from 2 kHz to 150 kHz, the CISPR 11 EMI Class A limits (150 kHz to 30 MHz), and the calculated unfiltered and filtered DM noise measurements (simulation of an EMI test receiver) of a three-level T-type converter switching at 20 kHz, with filter values specified in Table IV.

to 150 kHz [23]. The emissions that occur in this latter frequency range potentially affect amongst others the Power Line Communication (PLC), solid-state meters, and electronically controlled devices such as touch dimmer lamps [24,25].

Recently, the DM noise Compatibility Level (CL) for frequencies from 2 kHz to 30 kHz has been published in [26], and the CL for up to 150 kHz is expected soon [25]. However, a certain margin has to be included between the CL and the Emission Level (EL), the latter being the limit that the noise emitting system has to respect. This margin should be equal to or higher than 3 dBµV for the range from 2 kHz to 9 kHz,

and equal to or higher than 9 dBµV for the range from 9 kHz to 150 kHz [26]. In Fig. 7, the expected CL and EL that are presented in [25] are shown, together with the simulated DM noise of the three-level T-type converter (with the filter values presented in Table IV and without including parasitic effects of the filter), considering the worst-case of a 50 Ω test receiver. It has to be noted that due to the low switching frequency of 20 kHz, the filter design is constrained by the factor of four lower than switching frequency filter cut-off frequency limitation, see Section III-B. As it is finally seen in Fig. 7, the converter design successfully fulfills both the EMI limits below and above 150 kHz.

VI. Conclusion

In this paper, a quantitative multi-level topology evaluation is done to identify the most suitable three-phase inverter topologies to achieve a 99.5 % efficiency target. The low switching frequency imposed by the efficiency target leads to large passive (magnetic and capacitive) components. On the one hand, for the two-level bridge leg based converters, the size of the magnetics is very large due to a very tight loss budget, EMI and cut-off frequency filter requirements and the scaling laws of the switching stage output inductors (8x larger volume needed to halve the losses). On the other hand, creating a multi-level voltage output waveform comes at a cost of large capacitance volumes of the FCs. Hence, the two topologies that are offering the best power densities were designed in more detail, and the difference in power density from a conventional three-level T-type converter (2.2 kW/dm^3) and a seven-level HANPC converter (2.7 kW/dm^3) was identified to be approximately 20 % for the same efficiency. Finally, the upcoming EMI regulations were presented, and the three-level T-type converter was used as an example to analyze the low-frequency EMI limits. In the course of future research, hardware prototypes of the three-level T-type converter and the seven-level HANPC converter will be built, and the theoretical considerations presented in this paper will be comprehensively verified by measurements.

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