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Modeling and Multi-Objective Optimization of 2.5D Inductor-Based Fully Integrated Voltage Regulators for Microprocessor Applications

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***Abstract* – This work presents the modeling and the multi-objective optimization of a 2.5D inductor-based Fully Integrated Voltage Regulator (FIVR) with respect to efficiency η and/or chip area power density α, i.e. based on the η-α-Pareto-front, for microprocessor applications. The Voltage Regulator consists of a four-phase interleaved buck converter operated in Continuous Conduction Mode (CCM). The rated power of the considered converter is $1\,\mathrm{W}$, and input and output voltages are constant and equal to $V_{\mathrm{in}} = 1.7\,\mathrm{V}$ and $V_{\mathrm{out}} = 0.85\,\mathrm{V}$. The optimization employs analytical models for the switches, which reside on chip and are manufactured in a $32\,\mathrm{nm}$ CMOS SOI process, and for the passive components, i.e. racetrack inductors with magnetic core material and deep-trench capacitors that are fabricated in a silicon interposer. The optimization procedure considers thermal aspects and disregards solutions that lead to excessive component temperatures. According to the optimization results, either high efficiencies, greater than 90%, or high area power densities, with chip power densities greater than $20\,\mathrm{W/mm^2}$ and interposer power densities higher than $1.5\,\mathrm{W/mm^2}$ are achievable. The optimized design point, selected from the η-α-Pareto-front, features an efficiency of $90.1\,\%$, interposer power density of $0.309\,\mathrm{W/mm^2}$, and a chip power density of $27.4\,\mathrm{W/mm^2}$.**

***Keywords* – 2.5D Implementation, Buck Converter, Deep-Trench Capacitor, Racetrack Inductor, Optimization, Voltage Regulator.**

I. INTRODUCTION

Datacenters and telecom systems contain a myriad of high performance multi-core microprocessors that are characterized by high current demands ($> 100\,\mathrm{A}$ [1]), along with precise and fast regulation requirements to allow for energy savings using per-core Dynamic Voltage and Frequency Scaling (DVFS) [2]. This strategy requires real time power management and Point of Load (PoL) power converters to provide granular voltage domains depending on the load demand of each specific core or parts of a core. Inductor-based Fully Integrated Voltage Regulators (FIVRs) have been largely used to implement the PoL converters in the aforementioned applications due to their high efficiencies and accurate voltage regulation capabilities.

On-chip Voltage Regulator Modules (VRMs) are found in the literature in different levels of integration and this work distinguishes between 3D [3], 2D [4], and 2.5D structures [5], [6]. 3D structures employ at least two different active semiconductor dies: one for the microprocessor and one for the active power semiconductor components of the VRMs [3]. The dies form a chip stack with Through Silicon Vias (TSVs) as vertical interconnects. In 2D integrated structures [4], all power components are integrated onto the microprocessor (load) die, which means that only one active semiconductor die is required. 2.5D VRMs differ from 2D and 3D structures in having their power components split, usually the switches on the microprocessor die, and passives off-chip, either in a laminate [5] or in an interposer [6]. Compared to 2D integration, the 2.5D integration features passive components with lower losses at same footprint size of the passive components and allows for minimal loss of precious active silicon area [5]. In addition, the use of the highly efficient sub-nanometer transistors of the microprocessor die for the VRMs, cf. **Figure 1(a)**, allows for operation with switching frequencies greater than 100 MHz.

[6] presents a 2.5D buck converter implemented in 45 nm SOI technology using racetrack coupled inductors and deep-trench capacitors that is operated with switching frequencies up to 300 MHz. There, a peak efficiency of $\eta \approx 75\%$ at a power density of $\alpha \approx 1.5\,\mathrm{W/mm^2}$ is achieved. In [5], Intel presents the VRMs of its Haswell microprocessor with a peak efficiency of 90% and a vague estimation of the power density, determined from published data, of $\alpha \approx 1\,\mathrm{W/mm^2}$. Intel ultilizes Fin-FET transistors assembled in 22 nm and air-core inductors built-in the package are utilized.

The aim of this work is to identify the design parameters and trade-offs for high conversion efficiencies, i.e. greater than 90%, and high power densities, i.e. chip power density greater than $20\,\mathrm{W/mm^2}$ and interposer power density greater than $1.5\,\mathrm{W/mm^2}$, for a 2.5D implementation of an integrated buck converter, which is beyond the current state-of-the-

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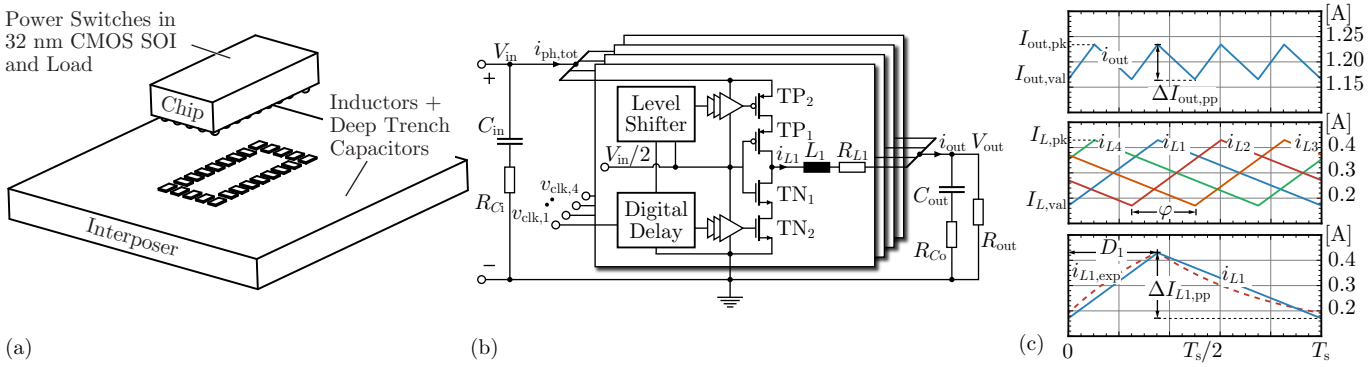

Fig. 1. **(a)** 2.5D FIVR with both, the active components and the load, being realized in the same die, i.e. the chip; the passive components are built into a separate silicon interposer; **(b)** four-phase interleaved buck converter with stacked transistors, to allow for operation with input voltages of up to twice the breakdown voltage of one 32 nm single transistor; **(c)** general waveforms of i_{out}, $i_{L1,2,3,4}$, and i_{L1} of the ideal four-phase buck converter for interleaved operation. The waveforms are generated for $L_{1,2,3,4} = L = 15\,\text{nH}$, $V_{\text{in}} = 1.7\,\text{V}$, $V_{\text{out}} = 0.85\,\text{V}$, $f_s = 100\,\text{MHz}$, and $\varphi = 90°$. The waveform $i_{L1,\text{exp}}$ is generated with $R_{\text{PMOS,on}} = 40\,\text{m}\Omega$, $R_{\text{NMOS,on}} = 50\,\text{m}\Omega$, and $R_L = 3\,\Omega$.

art presented in the literature. In order to achieve these performance figures, a multi-objective optimization, based on the calculation of the η-α-Pareto-front, is proposed to find the optimum design parameters for a 2.5D inductor-type FIVR, i.e. the four-phase interleaved buck converter, depicted in **Figure 1(b)**, for a given set of specifications and for the available component technologies. The investigated converter employs power switches implemented in the IBM's 32 nm SOI process, high quality microfabricated racetrack inductors (manufactured by Tyndall) and high capacitance density deep-trench capacitors (manufactured by IPDiA) and, thus, takes advantage of cutting edge technologies in order to push the FIVRs' limits with regard to efficiency and power density. This work provides the components' dimensions resulting from the optimization algorithm and the loss breakdown for the optimized design. **Section II** summarizes the main converter specifications. **Section III** describes inductor-based converter topologies suitable for the studied application and the main waveforms of the four-phase interleaved buck converter operated in Continuous Conduction Mode (CCM). **Section IV** describes the component models used to calculate losses and chip size areas for the power switches, the inductors, and the capacitors. A focus is given to detail the swithing process, which comprehension is necessary to generate the MOSFETs' switching loss models. The η-α-Pareto-optimization procedure is explained in **Section V**. Finally, **Section VI** discusses the calculated results for the four-phase converter using racetrack inductors with magnetic material, which demonstrate the feasibility of designs with efficiencies greater than 90%, chip power densities of more than $20\,\text{W/mm}^2$, and interposer power densities greater than $1.5\,\text{W/mm}^2$.

II. CONVERTER SPECIFICATIONS

The rated power of the considered converter is 1 W. The input and output voltage specifications are based on typical PoL VRMs in the industry that are designed to power microprocessors at dc voltages in the range of 0.6 V to 1.2 V depending on the workload [1]. Based on this, nominal input and output voltages of $V_{\text{in}} = 1.7\,\text{V}$ and $V_{\text{out}} = 0.85\,\text{V}$ are specified. A maximum output voltage ripple of 0.5% of V_{out} is assumed for dimensioning of the output capacitors.

III. SUITABLE CONVERTER TOPOLOGIES

In the standard single-phase buck converter, the transistors have to be able to block the full input voltage. In the considered application, the input voltage $V_{\text{in}} = 1.7\,\text{V}$ is greater than the 32 nm transistors' drain-to-source break-down voltage of $V_{\text{ds,max}} \approx 1.2\,\text{V}$. A possible approach to deal with the high input voltage employs series stacked transistors in replacement of the single high-side and low-side FETs as depicted in **Figure 1(b)** and implemented in [4] for a single-phase converter. This solution only marginally increases the converter area, in particular in comparison to a multilevel approach employing flying capacitor converters, since there is no need for additional passive components. The interleaved operation of multiple buck converters, i.e. parallel connection according to Figure 1(b) with gate signals phase-shifted by $\varphi = 2\pi/N_{\text{ph}}$ (cf. **Figure 1(c)**) [7], where N_{ph} is the number of converter phases, allows for a reduction of the output current ripple [8]. This paper investigates a four-phase interleaved buck converter with two stacked transistors to compose the high-side and low-side switches. As in [7], the equations for the switches' and inductors' instantaneous, mean, and rms currents equation consider piecewise linear current behavior, i.e. the implications of conduction, copper, and core losses on the current waveforms are neglected.

IV. COMPONENT MODELS

In order to perform the converter optimization, the main design parameters, i.e. inductance, output capacitance, and the corresponding losses and chip and interposer areas of the converter elements, are derived as functions of the converter operating conditions. This section outlines analytical models of the power switches manufactured in the 32 nm SOI process, the racetrack inductor with core material, and the deep trench-capacitors.

A. Power semiconductors

The FETs' conduction and switching losses are considered to be dependent on their channel widths[1] (T_{wP} and T_{wN}), instantaneous drain currents, and junction temperatures (T_{j}).

[1]Only the channel widths of the thin-oxide transistors are considered, since the transistor lengths are fixed by design rules in this technology.

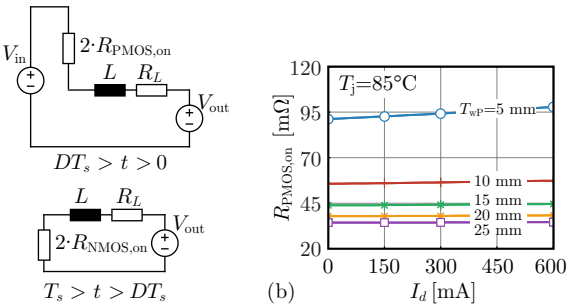

Fig. 2. **(a)** Phase equivalent circuits to calculate the switches' conduction losses. **(b)** Dependence of $R_{\mathrm{PMOS,on}}$ on the channel width for various drain current values.

Switching losses are also very dependent on the duration of the dead-time intervals ($t_{\mathrm{d,1}}$ and $t_{\mathrm{d,2}}$) that are used to avoid short circuits in the half-bridges during switching and allow for soft-switching.

According to the equivalent circuits depicted **Figure 2(a)**, the calculation of the conduction losses of the transistors requires their on-state resistances to be known: except for the small time intervals during switching, the buck converter resides in one of these two states. The values of the on-state resistances for p- and n-channel MOSFETs (PMOS and NMOS) have been determined by means of Cadence simulations. The obtained results reveal little dependency of the on-state resistances on the drain currents, cf. **Figure 2(b)** for $R_{\mathrm{on,PMOS}}$, (the figure depicts the interpolated values along with the marked basic values). The on-state resistances, however, greatly depend on the transistor channel widths, i.e. a great value of the transistor channel width enables a low value of the on-state channel resistance.

The total conduction losses of the multi-phase buck converter are calculated for the same channel widths for the stacked transistors of the same type, i.e. $T_{\mathrm{w,TP_1}} = T_{\mathrm{w,TP_2}} = T_{\mathrm{wP}}$ and $T_{\mathrm{w,TN_1}} = T_{\mathrm{w,TN_2}} = T_{\mathrm{wN}}$, which results in

$$P_{\mathrm{cond}} = 2N_{\mathrm{ph}} \left(R_{\mathrm{PMOS,on}} \cdot I^2_{\mathrm{PMOS,rms}} + R_{\mathrm{NMOS,on}} \cdot I^2_{\mathrm{NMOS,rms}} \right), \tag{1}$$

where $I_{\mathrm{PMOS,rms}}$ and $I_{\mathrm{NMOS,rms}}$ are the rms currents through the PMOS and NMOS switches.

Besides conduction losses, the switching losses amount to a significant part of the total losses of on-chip voltage regulators. Switching losses may be determined with analytical models [3], simulation results [9], or measurement results [10]. This work estimates the switching losses with a multi-variable interpolation algorithm that is parameterized with data obtained from a discrete number of Cadence simulations for one converter half-bridge, using the test configuration depicted in **Figure 3(a)**. In [11], a good match on the converter efficiency and power density is obtained comparing experimental results with Cadence simulations.

During a switching process, a significant amount of energy may be transferred from one switch to another, especially when the Zero Voltage Switching (ZVS) condition is fulfilled [10]. Therefore, the drain currents $i_{\mathrm{D,TP_1}}$, $i_{\mathrm{D,TP_2}}$, $i_{\mathrm{D,TN_1}}$, and $i_{\mathrm{D,TN_2}}$ and the blocking voltages $v_{\mathrm{SD,TP_1}}$, $v_{\mathrm{SD,TP_2}}$, $v_{\mathrm{DS,TN_1}}$, and $v_{\mathrm{DS,TN_2}}$ of the respective half-bridge need to be observed simultaneously in order to calculate the total dissipated energy. The energies dissipated by each switch of the half-bridge are calculated with

$$E_{\mathrm{TP}_k,\mathrm{sw}} = \int_{t_{\mathrm{begin}}}^{t_{\mathrm{end}}} v_{\mathrm{SD,TP}_k} \; i_{\mathrm{D,TP}_k} \mathrm{d}t, \; k = \{1,2\}, \tag{2}$$

for PMOS and

$$E_{\mathrm{TN}_k,\mathrm{sw}} = \int_{t_{\mathrm{begin}}}^{t_{\mathrm{end}}} v_{\mathrm{DS,TN}_k} \; i_{\mathrm{D,TN}_k} \mathrm{d}t, \; k = \{1,2\}, \tag{3}$$

for NMOS; the time instants t_{begin} and t_{end} correspond to the beginning and the end of the switching process. If the result of the integration is positive, the corresponding switch dissipates or stores energy. If the result of the integration is negative, the corresponding switch releases stored energy. The total switching loss energy generated by the half-bridge in one switching event is

$$E_{\mathrm{sw}} = E_{\mathrm{TN_1,sw}} + E_{\mathrm{TN_2,sw}} + E_{\mathrm{TP_1,sw}} + E_{\mathrm{TP_2,sw}}. \tag{4}$$

Three different switching situations can occur in the investigated buck converter with synchronous rectification, which, with respect to its microprocessor application, is only operated with unidirectional energy flow (from the supply to the load):

- case 1: positive inductor current ($I_{\mathrm{sw}} > 0$ in Figure 3(a)) and v_{x} switches from V_{in} to 0;
- case 2: positive or zero inductor current ($I_{\mathrm{sw}} \geq 0$ in Figure 3(a)) and v_{x} switches from 0 to V_{in};
- case 3: negative current ($I_{\mathrm{sw}} < 0$ in Figure 3(a)) and v_{x} switches from 0 to V_{in}.

In cases 1 and 3 the conditions to achieve ZVS are fulfilled, and it depends on the respective dead-time durations, whether lossless switching operations are achieved. Case 2 always leads to hard switching. Since this work considers peak-to-average (*PAR*) [12] ratios of the inductor current in the range from 1 to 2, only cases 1 and 2 occur.

Figure 3(b) shows the simplified waveforms of the Cadence simulations used to extract the switching loss energies of the half-bridge configuration depicted in Figure 3(a). The required instantaneous switching current is set to a constant value I_{sw} during the simulation. At $t = t_{\mathrm{1a}}$ the switching event of case 1 occurs with the theoretical condition for ZVS fulfilled. At $t = t_{\mathrm{2a}}$ the switching event of case 2 occurs with the condition for hard switching fulfilled. **Figures 3(c)** and **(d)** illustrate the main transient waveforms during $t_{\mathrm{1a}} \leq t \leq t_{\mathrm{1d}}$ and $t_{\mathrm{2a}} \leq t \leq t_{\mathrm{2d}}$, respectively. The transient processes during switching are detailed below.

1) $t_{1a} \leq t \leq t_{1d}$ *and case 1:* Before $t = t_{\mathrm{1a}}$ both PMOS transistors are in their on-states and conduct the switching current I_{sw}; both NMOS transistors are turned off. At $t = t_{\mathrm{1a}}$, $\mathrm{TP_2}$ is commanded to switch off and its source-to-drain voltage $v_{\mathrm{SD,TP_2}}$ increases. The increasing voltage $v_{\mathrm{SD,TP_2}}$ decreases the gate to source voltage of $\mathrm{TP_1}$ and, as a consequence, the turn-off of $\mathrm{TP_1}$ occurs immediately after the turn off of $\mathrm{TP_2}$. Since the rise of $v_{\mathrm{SD,TP_1}}$ is delayed with respect to $v_{\mathrm{SD,TP_2}}$, the converter input voltage is not equally shared between $\mathrm{TP_1}$ and $\mathrm{TP_2}$. Due to the increasing values of $v_{\mathrm{SD,TP_1}}$ and $v_{\mathrm{SD,TP_2}}$ and the constant input voltage V_{in}, the voltage between output and minus nodes of the half

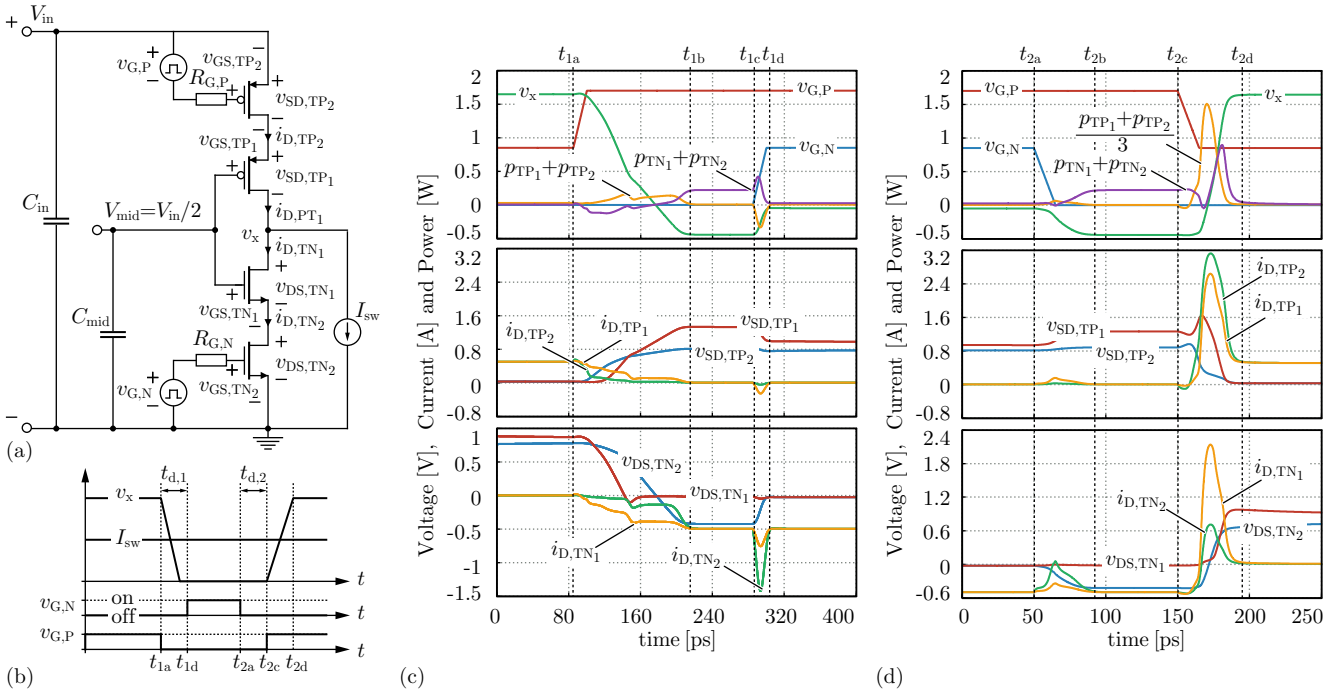

Fig. 3. **(a)** Test configuration of a single converter phase used to obtain the switches' switching loss parameters by means of Cadence simulations. **(b)** Simplified representation of the gate signals used in the simulations to extract the loss parameters of the considered switching cases 1 and 2 , which occur during $t_{1a} < t < t_{1d}$ and $t_{2a} < t < t_{2d}$, respectively. **(c)** Converter waveforms that describe the ZVS event of case 1 ($I_{sw} = 500\,\text{mA}$). **(d)** Converter waveforms that describe the hard-switching event of case 2 ($I_{sw} = 500\,\text{mA}$). The waveforms generated for $V_{in} = 1.7\,\text{V}$, $T_{wP} = T_{wN} = 12\,\text{mm}$, $R_{G,P} = R_{G,N} = 240\,\text{m}\Omega$, $t_{d,1} = 200\,\text{ps}$, $t_{d,2} = 100\,\text{ps}$. During changes of gate to source voltages, significant gate currents arise. For this reason, $i_{D,TP_1} \neq i_{D,TP_2}$ and $i_{D,TN_1} \neq i_{D,TP_2}$ are observed during the respective time intervals.

bridge, v_x, decreases and eventually becomes negative when the body diodes of the NMOS switches start to conduct. Since the gate of TN_1 is clamped to $V_{in}/2$, the decrease of v_x turns on TN_1. During $t_{1a} \leq t \leq t_{1b}$ the waveform $p_{TP_1} + p_{TP_2}$ is most of the time positive and the waveform $p_{TN_1} + p_{TN_2}$ is negative meaning that the PMOS transistors consume energy (switching losses, energy stored in the effective output capacitances) and the NMOS transistors release the energy stored in their effective output capacitances. The total energy lost during this time interval is obtained by integrating the instantaneous NMOS and PMOS power curves, which, in the depicted case, leads to almost no losses during $t_{1a} \leq t \leq t_{1b}$ (ZVS). At $t = t_{1b}$, v_x reaches its minimum value, which remains constant during $t_{1b} \leq t \leq t_{1c}$, when the channel of TN_1 and the body diode of TN_2 are conducting the full I_{sw}, which leads to increased conduction losses during this time interval. At $t = t_{1c}$, TN_2 is turned on and the output current I_{sw} starts to also flow through the channel of TN_2.

2) $t_{2a} \leq t \leq t_{2d}$ and case 2: Before $t = t_{2a}$ both NMOS transistors are in their on-states and conduct the switching current I_{sw}; both PMOS transistors are turned off. At $t = t_{2a}$, TN_2 is commanded to switch off forcing its body diode to conduct. At $t = t_{2b}$, v_x reaches its minimum value, which remains constant during $t_{2b} \leq t \leq t_{2c}$, when the channel of TN_1 and the body diode of TN_2 are conducting the full I_{sw}, which leads to increased conduction losses during this time interval. At $t = t_{2c}$, TP_2 is commanded to switch on and its source-to-drain voltage v_{DS,TP_2} starts to decrease. Since TN_1 is in the on-state and the body diode of TN_2 is subject to reverse recovery (this diode has been conducting the switching current I_{sw}), v_x does not change immediately and this leads to an unbalancing of the source-to-drain voltages of TP_2 and TP_1. After the body diode of TN_2 is recovered, v_{DS,TN_2} starts to increase and, as a consequence, v_x starts to increase with nearly constant slope until it reaches V_{in} at $t = t_{2d}$. Since the gate of TN_1 is clamped to $V_{in}/2$, the increase of v_x decreases the gate-to-source voltage of TN_1, turning it off with the same voltage slope, which results in an approximate voltage sharing of v_x between TN_1 and TN_2. During the time interval $t_{2c} \leq t \leq t_{2d}$, the reverse recovery current and the additional current flowing through the gate of TN_1 increases the instantaneous losses of all transistors (especially those of TP_1 due to the delayed turn-off). During the entire switching process, $t_{2a} \leq t \leq t_{2d}$ the waveforms $p_{TP_1} + p_{TP_2}$ and $p_{TN_1} + p_{TN_2}$ are almost only positive, meaning that both, NMOS and PMOS switches, dissipate energy.

The obtained results of **Figure 4(a)** show that the energy losses of the switching transition of case 2 always increase with the increasing of the switching currents, while the energy losses of case 1 present a minimum when the dead-time interval $t_{d,1}$ is just enough to charge and discharge the effective output capacitance of the PMOS and NMOS, not allowing the body diode of TN_2 to conduct. The total switching losses of the multi-phase buck converter are calculated also considering $T_{w,TP_1} = T_{w,TP_2} = T_{wP}$ and $T_{w,TN_1} = T_{w,TN_2} = T_{wN}$, which results in

$$P_{sw} = N_{ph}\left(E_{sw,case1}(I_{L,pk}) + E_{sw,case2}(I_{L,val})\right) f_s, \qquad (5)$$

The gate charge of the power switches also contribute to a significant part of the total power semiconductor losses.

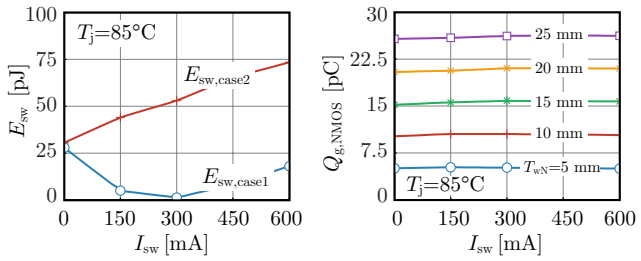

Fig. 4. **(a)** Total energy losses of case 1 and case 2 ($E_{\text{sw,case1}}$ and $E_{\text{sw,case2}}$) switching events for various drain current values. Plots generated using $T_{\text{w,TP}_1} = T_{\text{w,TP}_2} = 12\,\text{mm}$ and $t_{\text{d,1}} = t_{\text{d,2}} = 120\,\text{ps}$ **(b)** Dependence of $Q_{\text{g,NMOS}}$ on the channel width for various drain current values.

Results of **Figure 4(b)** show almost no dependence of $Q_{\text{g,NMOS}}$ on the switching currents. The gate charges, however, greatly depend on the transistor channel widths. The gate charge losses are calculated with

$$P_{\text{g}} = N_{\text{ph}} V_{\text{gs}} \left(Q_{\text{g,TP}_2}(I_{L,\text{val}}) + Q_{\text{g,TN}_2}(I_{L,\text{val}})\right) + Q_{\text{g,mid}}(I_{L,\text{val}}, I_{L,\text{pk}}) f_{\text{s}}, \qquad (6)$$

where $Q_{\text{g,TP}_2}$ and $Q_{\text{g,TN}_2}$ are the charge sourced by the gate supplies to completely turn off the PMOS and completely turn on the NMOS, respectively, $Q_{\text{g,mid}}$ is the sourced/absorbed charge by V_{mid} in one switching period, and $V_{\text{gs}} = 0.85\,\text{V}$ is the maximum value of the transistors gate voltage.

B. Power inductors

In this work, the converter optimization is performed for racetrack inductors using the same analytical equations, materials, and technology limitations as in [12], where the models have been verified with good accuracy against measurements from real inductors. The calculation of the copper losses of the inductors considers dc and ac winding losses, which are estimated using the methodology and (23)–(26) of [12]. The utilized core material is $Ni_{45}Fe_{55}$, which is considered to be linear and anisotropic with a relative permeability $\mu_{\text{c}} = 280$. The calculation of the total core losses considers hysteresis losses and eddy current losses. The hysteresis losses are calculated using (30) of [12] and the coefficients $K_{\text{h}} = 300$ and $b = 1.73$. The eddy currents in the core cause frequency dependent losses that are calculated with (31) of [12].

C. Output capacitors

The Passive Integration Connective Substrate (PICS) silicon based capacitor technology [13], developed by IPDIA, is employed in the proposed design. This technology is a combination of deep-trench and high temperature dielectric in Metal-Insulator-Metal (MIM) that allows for very high capacitance densities of up to $250\,\text{nF/mm}^2$, with low Equivalent Series Resistances (ESR $< 150\,\text{m}\Omega$ for $C > 50\,\text{nF}$) and low Equivalent Series Inductance (ESL $\approx 5-10\,\text{pH}$) in the switching frequency range of 10 MHz to 150 MHz. To obtain this low parasitic values, the capacitor design uses a large number of elementary capacitive cells, that are interconnected onto a parallel interconnection network [13]. For this specific implementation it is shown that the ESR is proportional to the inverse of the number of elementary cells, and as such can be adjusted by design. The interconnection network is optimized with respect to ESL, featuring interleaved structures that prevent local current loops, such as to increase the capacitor self-resonance frequency. In this work the ESR is modeled for five different types of capacitors, based on experimental data provided by IPDiA in the form $f(C) = k_1 10^{k_2 C}$. The calculation of the ESL assumes that the capacitor self-resonance is at $f_{\text{ress}} = 2 f_{\text{s}}$.

V. MULTI-OBJECTIVE CONVERTER OPTIMIZATION AND RESULTS

Figure 5(a) illustrates the flowchart of the implemented optimization procedure. The optimization algorithm starts with the definition of the converter specifications, summarized in **Section II**. Next, the design space $\boldsymbol{X} = \{x_1, x_2, ..., x_p\}$ is defined, where x_i is shown in Figure 5(a) and the parameter definitions, range of sweeps, and step sizes are shown in **Table I**. The geometrical parameters of the racetrack inductor with core material can be identified in Figure 4 of [12].

TABLE I
Buck converter variables' ranges and step sizes of the explored design space.

Parameters	Range	Step size	Unit
PAR	[1.2...2]	0.4	–
Number of turns, N	[1...5]	1	–
Winding width, t_{w}	[10...1200]	10 or 500	μm
Winding spacing, t_{s}	[10...50]	20	μm
Winding thickness, t_{t}	[10...50]	20	μm
Core length, c_{l}	[1...10]	3	mm
Core thickness, c_{t}	[1...10]	3	μm
NMOS channel width, T_{wN}	[5...15]	5	mm
PMOS channel width, T_{wP}	[5...15]	5	mm
Dead-time, $t_{\text{d,1}}$	[20...120]	50	ps
Dead-time, $t_{\text{d,2}}$	[20...70]	50	ps
Output capacitance, C_{out}	[0.1...500]	10.2	nF

The switches' loss parameters are extracted for the maximum temperature of 85 °C [11]. The output capacitor is optimized to require the minimum area possible and still fulfil the maximum output voltage ripple criterion. The optimization algorithm outputs the total converter efficiencies, the design parameters of all power components, and the calculated main parameters related to the converters' operating conditions, e.g. f_{s}, D, and $\Delta I_{L\text{pp}}$, for all designs in the considered design space. Designs with switches' loss density greater than $10\,\text{W/mm}^2$ and/or inductor peak flux densities above the saturation limit of $B_{\text{sat}} = 1.6\,\text{T}$ are excluded. For the given application, it is required to achieve 90% efficiency with maximal power density possible allowed by the employed technologies. **Figure 5(b)** depicts the optimization results and highlights the selected design with Peak-to-Average inductor current Ratio $PAR = 1.2$, $f_{\text{s}} = 70\,\text{MHz}$, $L = 51\,\text{nH}$, $C = 10.3\,\text{nF}$, $T_{\text{wP}} = 15\,\text{mm}$, $T_{\text{wN}} = 10\,\text{mm}$, $t_{\text{d,1}} = 120\,\text{ps}$ and $t_{\text{d,2}} = 70\,\text{ps}$. This design features $\eta = 90.1\,\%$ and $\alpha = 0.306\,\text{W/mm}^2$ (chip power density is $\alpha_{\text{PMIC}} = 27.4\,\text{W/mm}^2$ and interposer power density is $\alpha_{\text{inter}} = 0.309\,\text{W/mm}^2$).

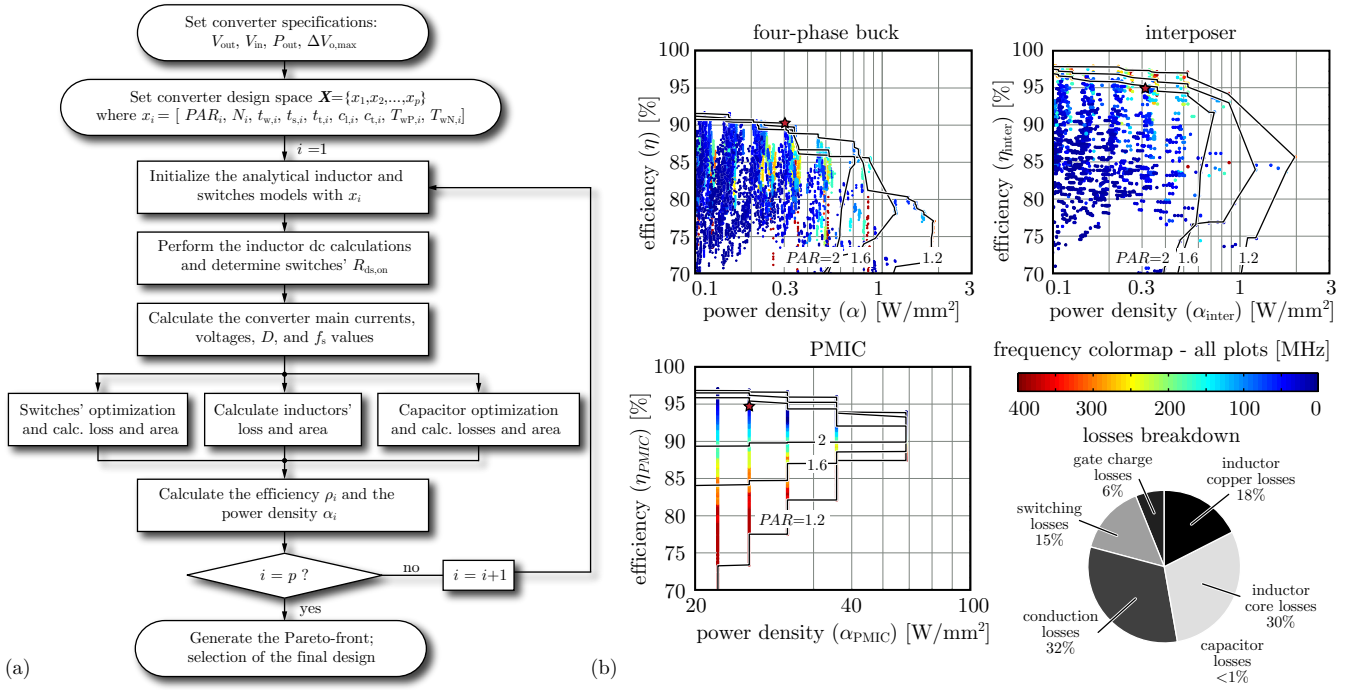

Fig. 5. Multi-objective optimization of the four-phase buck converter. **(a)** Flowchart of the optimization algorithm; **(b)** Plots of the $\eta-\alpha$ Pareto-fronts that result for the Power Management IC (PMIC), the interposer, and the complete four-phase buck converter; losses breakdown calculated for the selected Pareto-optimal design, showing that the inductor losses and the semiconductor losses of this design are $\approx 48\%$ and $\approx 53\%$ of the total losses, respectively. The Pareto-fronts show that either high efficiencies or high power densities are achievable.

VI. CONCLUSIONS

This work details the design procedure and the multi-objective Pareto-optimization of a 2.5D four-phase interleaved and inductor-based FIVR. For this purpose analytical models for 32 nm CMOS SOI power switches, racetrack inductors with core material, and deep-trench capacitors are summarized. The results demonstrate that optimal designs achieve efficiencies greater than 90% or power densities greater than $1.5\,\mathrm{W/mm^2}$, but not simultaneously. The selected design achieves an efficiency of 90.1 %, an interposer power density of $0.309\,\mathrm{W/mm^2}$, and a chip power density of $27.4\,\mathrm{W/mm^2}$.

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REFERENCES

[1] Intel Corporation Datasheet, *Intel® Xeon® Processor E5-1600 and E5-2600 v3 Product Families, Volume 1 of 2, Electrical*, 2014, URL: `http://www.intel.com`.

[2] J. Howard, *et al.*, "A 48-Core IA-32 Processor in 45 nm CMOS Using On-Die Message-Passing and DVFS for Performance and Power Scaling", *IEEE J on Solid-State Circuits*, vol. 46, no. 1, pp. 173–183, Jan. 2011.

[3] J. Rosenfeld, E. Friedman, "Linear and Switch-Mode Conversion in 3-D Circuits", *IEEE Trans Very Large Scale Integr (VLSI) Syst*, vol. 19, no. 11, pp. 2095–2108, Nov. 2011.

[4] M. Wens, M. Steyaert, "A Fully-Integrated 0.18 μm CMOS DC-DC Step-Down Converter, Using a Bondwire Spiral Inductor", *in Proc. IEEE CICC*, pp. 17–20, San Jose, CA, USA, Sep. 2008.

[5] E. Burton, *et al.*, "FIVR - Fully Integrated Voltage Regulators on 4th Generation Intel Core SoCs", *in Proc. 29th IEEE APEC*, pp. 432–439, Texas, Houston, USA, Mar. 2014.

[6] N. Sturcken, *et al.*, "A 2.5D Integrated Voltage Regulator Using Coupled-Magnetic-Core Inductors on Silicon Interposer", *IEEE J on Solid-State Circuits*, vol. 48, no. 1, pp. 244–254, 2013.

[7] M. Gerber, J. Ferreira, I. Hofsajer, N. Seliger, "Interleaving Optimization in Synchronous Rectified DC/DC Converters", *in Proc. 35th IEEE PESC*, Jun. 2004.

[8] J. Oliver, P. Zumel, O. Garcia, J. Cobos, J. Uceda, "Passive Component Analysis in Interleaved Buck Converters", *in Proc. 19th IEEE APEC*, Anaheim, California, USA, Feb. 2004.

[9] V. Svikovic, J. Cortes, P. Alou, J. Oliver, J. Cobos, G. Maderbacher, C. Sandner, "Energy-Based Switches Losses Model for the Optimization of PwrSoC Buck Converter", *in Proc IEEE 15th COMPEL*, pp. 1–7, Santander, Spain, Jun. 2014.

[10] F. Krismer, *Modeling and Optimization of Bidirectional Dual Active Bridge DC-DC Converter Topologies*, Ph.D. thesis, Federal Institute of Technology Zurich (ETH), Zurich, Switzerland, 2010.

[11] T. Andersen, *On-Chip Capacitor Voltage Regulators for Granular Microprocessor Power Delivery*, Ph.D. thesis, Federal Institute of Technology Zurich (ETH), Zurich, Switzerland, 2014.

[12] T. Andersen, C. Zingerli, F. Krismer, J. W. Kolar, N. Wang, C. Mathuna, "Modeling and Pareto Optimization of Microfabricated Inductors for Power Supply on Chip", *IEEE Trans on Power Electron*, vol. 28, no. 9, pp. 4422–4430, Sep. 2013.

[13] F. Lallemand, F. Voiron, "Silicon Interposers with Integrated Passive Devices, an Excellent Alternativ to Discrete Components", *in Proc. EMPC*, pp. 1–6, Grenoble, France, Sep. 2013.