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Comparative Evaluation of Y-Inverter against Three-Phase Two-Stage Buck-Boost DC-AC Converter Systems

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Comparative Evaluation of Y-Inverter against Three-Phase Two-Stage Buck-Boost DC-AC Converter Systems

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***Abstract*—Modern motor drives feature output filtering capability in order to protect the motor from high converter output voltage d*u*/d*t* rates and provide a sinusoidal current to the machine in order to minimize the rotor losses. The incorporation of such motor drive into a fuel-cell (FC) application is challenging since the power electronics converter has to cope with the power dependent variation of the FC voltage. In this paper three candidate converter concepts are comparatively evaluated i.e. a voltage source inverter with front-end DC-DC boost converter (boost VSI), a current source inverter with front-end DC-DC buck converter (buck CSI), and the recently proposed buck-boost Y-inverter topology. In a first step, the three implementations are assessed based on fundamental scaling laws, i.e. the semiconductor losses and/or the required chip area and the inductive components volume, which constitute a major part of the total system losses and volume, are analytically derived. In a second step, the exact performance of the different motor drive solutions in terms of efficiency η and power density ρ is quantified by means of a comprehensive multi-objective optimization. The optimization results reasonably mach the scaling-laws approach and hence further verify the practical value of the analytic calculations. Both the scaling-laws based analysis and the accurate optimization indicate a clear power density advantage in favor of the Y-inverter.**

***Index Terms*—High-speed drives, Scaling laws, Optimization, Modular Y-inverter**

I. Introduction

Drive systems typically comprise a voltage source inverter (VSI) powered from a stabilized DC energy source followed by a motor as visualized in **Fig. 1(a)**. In case of a fuel-cell (FC) powered drive system, however, the input voltage strongly drops with increasing output power (cf. **Fig. 1(b.i)**) which greatly impacts the achievable performance and/or design of the following power electronics stage and the motor. For example, under low power conditions, the high input voltage $U_{\text{FC,max}}$ imposes a high voltage stress on the converter components, whereas during rated power operation, the low input voltage $U_{\text{FC,min}}$ leads to a high current stress (cf. **Fig. 1(b.ii)**), thus the drive system has to be inevitably overdimensioned. Furthermore, since the machine voltage linearly increases with the rotational speed while the FC voltage drops, in certain cases the machine can no longer be directly driven by a VSI. An application of this type is considered in the followng (cf. **Tab. I**). At a nominal rotational speed of $300\,\text{krpm}$ [1], the motor of the underlying $1\,\text{kW}$ compressor drive system exhibits a back-EMF phase voltage of $\tilde{U}_{\text{M}} = 30\,\text{V}_{\text{RMS}}$, whereas at the same time the FC voltage drops from $U_{\text{FC,max}} = 120\,\text{V}$ down to $U_{\text{FC,min}} = 60\,\text{V}$ at its nominal output power. Hence, the direct VSI can no longer drive the permanent magnet synchronous motor (PMSM) at its nominal output power and rotational speed, since in this case a minimum DC-link voltage of $U_{\text{DC,min}} = 74\,\text{V}$ would be needed.

One possibility to raise the low FC voltage at rated power operation is to place a boost-type DC-DC converter in front of the VSI (boost VSI - cf. **Fig. 2(a)**), which generates an intermediate DC supply voltage $U_{\text{FC,min}} \leq U^*_{\text{DC}} \leq U_{\text{FC,max}}$, that in return offers flexibility with respect to the rated motor voltage and reduces the current stress of the inverter under full power operation. Beneficially, the additional component count is low and thus the drive system still stays simple. However, due to the two-stage voltage conversion and the bulky boost inductors, both the efficiency and the power density drop.

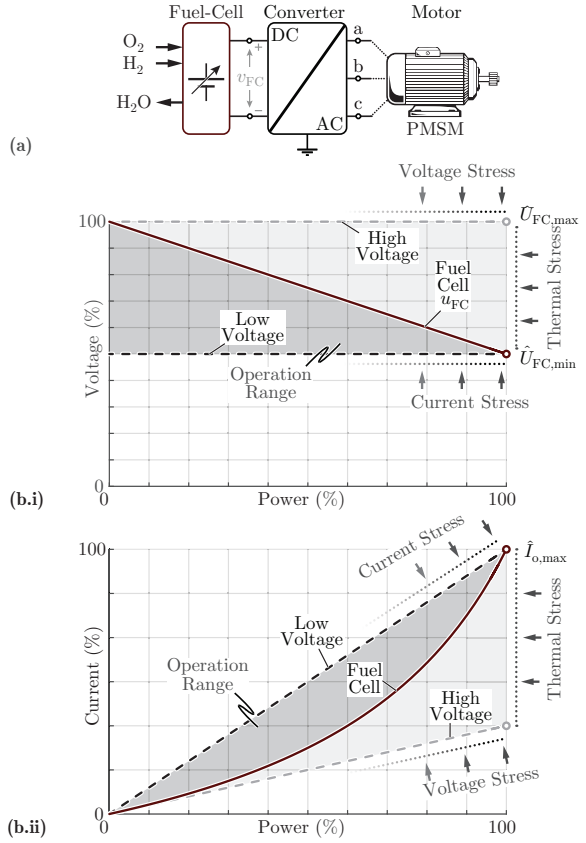

Fig. 1: (a) Fuel-cell (FC) powered motor drive employing a conventional voltage source inverter (VSI). The power dependent voltage variation of the FC is highlighted in **(b.i)** while the corresponding output current is plotted in **(b.ii)**.

Furthermore, as shown in **Fig. 2(a)**, an output filter is typically added to modern drive systems in order reduce down the high $\text{d}u/\text{d}t$ on the inverter output voltage resulting from today's wide bandgap semiconductor devices, which otherwise are directly applied to the motor windings [2]–[4], and to get smooth output voltages/currents which drastically reduce the radiated and conducted EMI noise, and thus also enables the use of unshielded motor cables (cost reduction) [5]–[7] and the reduction of rotor losses, that predominantly exist in high-speed motors [8], [9].

As an alternative to the boost VSI, a current source inverter (CSI) with integrated boost functionality can be used, which in addition benefits from an integrated output filter and therefore provides a continuous AC output voltage eliminating the need of a dedicated output filter. Moreover, as shown in **Fig. 2(b)**, the buck CSI incorporates only one inductive component which in addition is operated with a DC current, thus promises a compact overall design. As a drawback, however, the switches of the inverter stage have to be realized with

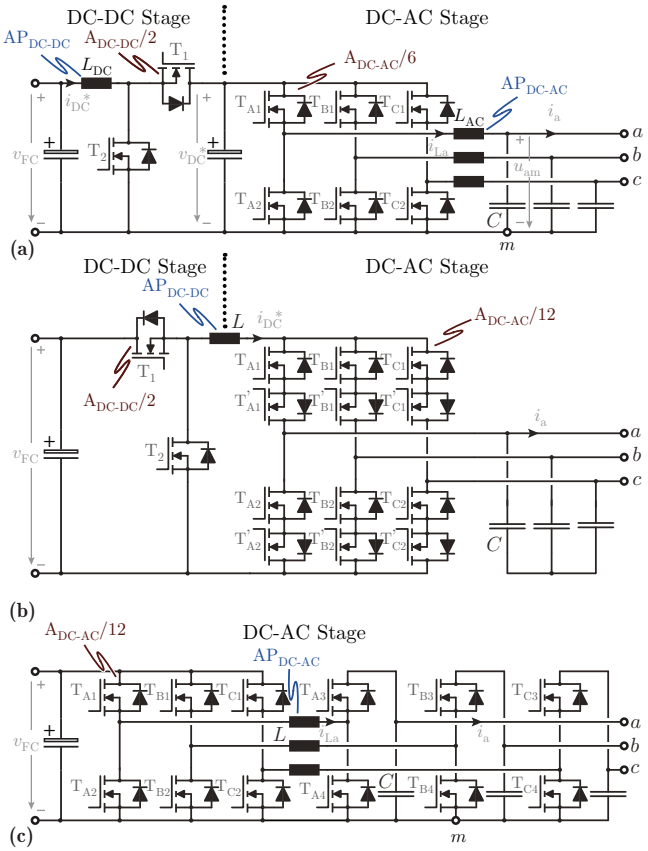

Fig. 2: Different fuel-cell (FC) powered motor drive implementations: **(a)** cascaded boost DC-DC converter with voltage source inverter (boost VSI), **(b)** current source inverter (CSI) based solution where a buck-type DC-DC converter precedes a CSI (buck CSI) and **(c)** Y-inverter, which enables wide input-output voltage range with single-stage energy conversion (i.e. no interface DC-DC converter required). In all converters the semiconductor chip areas A of each switch and the inductor area products $AP_{\mathrm{DC-DC}}$ and $AP_{\mathrm{DC-AC}}$ are highlighted.

e.g. two anti-series connected MOSFETs, which in consequence leads to higher conduction losses. Furthermore, due to the inherent boost functionality, the FC input voltage always has to be below the output voltage. Hence, at low output power, where the FC input voltage exceeds the needed machine voltage, the input voltage of the CSI has to be reduced by a precedent buck-stage (buck CSI), which can be bypassed at higher output power (T_1 is permanently on), hence only generates additional conduction losses at rated power.

The same buck-boost functionality with integrated output filter can also be achieved with the so-called Y-inverter (cf. **Fig. 2(c)**) as proposed by the authors in [10]. The Y-inverter represents an interesting alternative, since it manages to drive high EMF motors without any additional DC-DC converter. Furthermore, compared to the buck CSI, the Y-inverter features a phase-modular structure, i.e. three separate buck-boost DC-DC converters connected to a common ground, and doesn't need any anti-series connected switching devices, which results in a simpler converter and control structure as well as in lower conduction losses due to the reduced component count in the conduction path. Similarly to the buck CSI, depending on the input to output voltage ratio, either only the buck or the boost stage is switching while the high-side switch of the other stage is permanently on. Hence, compared to the boost VSI, the switching losses which

TABLE I: Fuel-cell powered motor drive specifications.

Parameter	Value
Motor Speed n	300 krpm
Motor EMF $\tilde{U}_{\mathrm{M}}$	30V (Phase, RMS)
Fundamental freq. f_{o}	5 kHz
Fuel-cell voltage U_{FC}	60V...120V
Power P	1 kW

especially occur at high switching frequencies can drastically be reduced.

Nevertheless, each converter topology shown in **Fig. 2** has its advantages and disadvantages which at first glance are difficult to assess and in consequence no topology can be immediately discarded. Therefore, in this paper a comprehensive comparison of the above mentioned candidate topologies is performed. Firstly, analytic models based on fundamental scaling laws are derived for the semiconductor devices and the inductive components which are the major drivers of losses and volume respectively in **Sec. II**. This analytic approach enables an intuitive and fair preliminary comparison of the three converter topologies in **Sec. III**. In **Sec. IV**, the performance of the various solutions, including all the converter components (in addition to the inductors and semiconductor devices), is evaluated in terms of efficiency η and power density ρ by means of a comprehensive multi-objective optimization. There, a performance benefit in favor of the Y-inverter is deduced for the given fuel-cell application case at hand. Finally, the conclusions are drawn in **Sec. V** and an outlook on the continuation of this research is given.

II. Analytic Comparison Approach

In order to identify the basic performance characteristics of the various converter concepts shown in **Fig. 2**, a comparison is performed based on fundamental scaling laws. Namely, the semiconductor devices and the inductive components, which are major drivers of losses and volume respectively, are modeled by analytic formulas. Subsequently, the derived models are applied to the considered converter concepts.

A. Chip Area and Losses of Semiconductor Devices

Typically different semiconductor devices must be selected in terms of voltage rating U_{r} and chip area A for the different converter implementations [11], [12]. In order to meaningfully compare the different converter options, a comprehensive and fair figure of merit (FOM) addressing the needs of industry (i.e. low cost) is required. To this end, the chip area based approach of [13], [14] is selected which determines the minimum required semiconductor chip area A_{min} and/or minimizes the semiconductor cost.

The chip area calculation algorithm is visualized in **Fig. 3(b)** and is described in the following. The chip is assumed to be mounted on a heatsink with a given surface temperature of $T_{\mathrm{h}} = 85^{\mathrm{o}}\mathrm{C}$ via a thermal pad (cf. **Fig. 3(a)**). In addition the semiconductor device is considered to be operated at its junction temperature limit $T_{\mathrm{j,max}} = 120^{\mathrm{o}}\mathrm{C}$, a value widely used in industry. Hence, depending on the thermal resistances $R_{\theta\mathrm{jc}}$ (junction-to-case) and $R_{\theta\mathrm{ch}}$ (case-to-heatsink), which scale with the chip area A, the maximum allowed semiconductor losses are

$$P_{\mathrm{max}}(A) = \frac{T_{\mathrm{j,max}} - T_{\mathrm{h}}}{R_{\theta\mathrm{jc}}(A) + R_{\theta\mathrm{ch}}(A)}. \quad (1)$$

If the chip area A is increased, the thermal resistance $R_{\theta\mathrm{jc}} + R_{\theta\mathrm{ch}}$ decreases as are the conduction losses because of the lower on-state resistance R_{ds}. In contrast, however, the switching losses which scale with the parasitic output capacitance C_{oss} and therefore with the

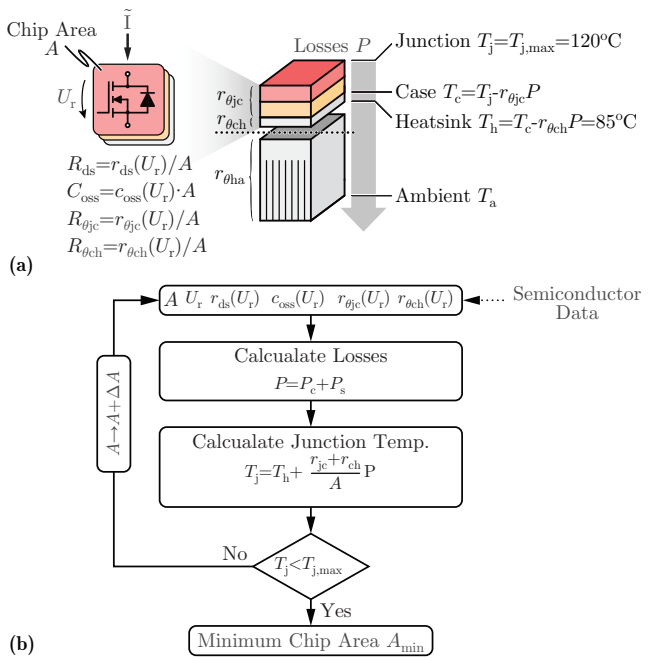

Fig. 3: **(a)** The employed MOSFET model is illustrated: The model is based on specific (i.e. normalized to the chip area A) electrical and thermal parameters $r_{dc}, c_{oss}, r_{\theta jc}, r_{\theta ch}$ and assumes a constant heatsink temperature of $T_h = 85°C$. The iterative chip area based semiconductor optimization algorithm is highlighted in **(b)**. There starting from a small chip area value A the chip area dependent converter losses are calculated. Afterwards, the chip area is gradually increased $A \rightarrow A + \Delta A$ until the losses can be thermally dissipated opposite the heatsink temperature $T_h = 85°C$ without exceeding the maximum junction temperature $T_j = 120°C$. Accordingly, the minimum chip area A_{min} is selected by the algorithm.

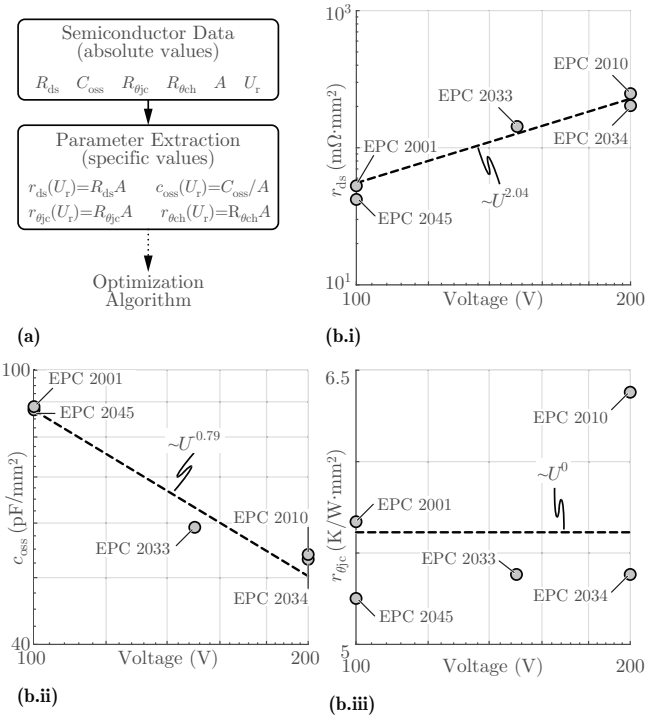

Fig. 4: **(a)** Extraction procedure of the specific (i.e. normalized to the chip area A) electrical and thermal parameters $r_{ds}, c_{oss}, r_{\theta jc}$ of GaN MOSFETs. The scaling of the specific on-state resistance r_{ds} for $T_j = 120°C$ junction temperature, the charge equivalent parasitic output capacitance c_{oss} and the thermal junction-to-case resistance $r_{\theta jc}$ with respect to the rated voltage U_r are plotted in **(b.i)-(b.iii)**, respectively.

chip area A would increase. Hence, with too small chip areas the conduction losses and the thermal resistances are too high, which means the chip area has to be increased until the chip temperature decreases to the $T_{j,max} = 120°C$. Thus optimum and/or minimum chip area A_{min} is defined as the chip area which satisfies the junction temperature sidecondition $T_j = T_{j,max}$. Further enlargement of the chip area above A_{min} would probably lead to lower losses (depending how the switching losses increase), however, the semiconductor costs would definitely increase. Therefore, the minimum chip area A_{min} is an intuitive FOM that enables comparison of fundamentally different converter topologies mainly concerning costs.

If the algorithm is applied to the example case of a buck DC-DC converter (where the total chip area $A_{DC\text{-}DC}$ is assumed to be equally shared among the high and the lows side switches, resulting in a single semiconductor device chip area $A = \frac{A_{DC\text{-}DC}}{2}$), a lower bound for the semiconductor losses described in [12] is

$$P_{DC\text{-}DC} = \underbrace{\frac{r_{ds}(U_r)}{A}\tilde{I}_o^{\,2}}_{\substack{\text{Conduction}\\ \text{losses}}} + \underbrace{A c_{oss}(U_r) U_{in}^2 f_s}_{\substack{\text{Switching}\\ \text{losses}}}, \tag{2}$$

where r_{ds} ($m\Omega\,mm^2$) is the specific on-state resistance, c_{oss} (pF/mm^2) is the specific parasitic output charge equivalent capacitance, U_{in} and $\tilde{I}_o$ are the input voltage and the RMS output current of the buck converter respectively, while $U_r = \frac{U_{in}}{0.7}$ is the rated voltage of the semiconductor devices. The thermal resistances are subsequently calculated based on the total semiconductor chip area $A_{DC\text{-}DC}$ (i.e. not only considering a single device) and the junction temperature is derived as

$$T_j = T_h + \frac{r_{\theta jc} + r_{\theta ch}}{A_{DC\text{-}DC}} P_{DC\text{-}DC}, \tag{3}$$

where $r_{\theta jc}$ and $r_{\theta ch}$ ($K\,mm^2\,W^{-1}$) are the specific junction-to-case and case-to-heatsink thermal resistances. As sown in **Fig. 3** the chip area $A_{DC\text{-}DC}$ is gradually increased until the junction temperature constraint $T_j < 120°C$ is satisfied.

The presented algorithm relies heavily on the accuracy of the specific electrical and thermal MOSFET's parameters r_{ds}, c_{oss}, $r_{\theta jc}$ which in turn scale with the semiconductor device rated voltage U_r, as well as the case-to-heatsink isolation material thermal properties $r_{\theta ch}$. Those parameters were carefully extracted based on the latest GaN devices with voltage ratings $U_r \in [100\,V, 200\,V]$. The parameter extraction algorithm is visualized in **Fig. 4(a)**, while the analytic models are plotted against the commercial semiconductor devices data in **Fig. 4(b)**. The MOSFET's parameters derived as a function of the rated voltage are

$$\begin{aligned} r_{ds} &= 4.54 \cdot 10^{-6} U_r^{2.04}\,m\Omega\,mm^2 \\ c_{oss} &= 3.3 \cdot 10^{3} U_r^{-0.79}\,pF\,mm^{-2} \\ r_{\theta jc} &= 5.61K\,mm^2\,W^{-1}\ r_{\theta ch} = 200K\,mm^2\,W^{-1}\ [15]. \end{aligned} \tag{4}$$

B. Area Product and Volume of Inductive Components

The minimum achievable volume of inductors is derived analytically considering the area product (AP). The area product $A_c A_w$ which depends on the electrical parameters (i.e. inductance value L, peak $\hat{I}_L$ and RMS inductor current $\tilde{I}_L$), the core and winding material properties (i.e. core saturation flux density $\hat{B}$, maximum allowable

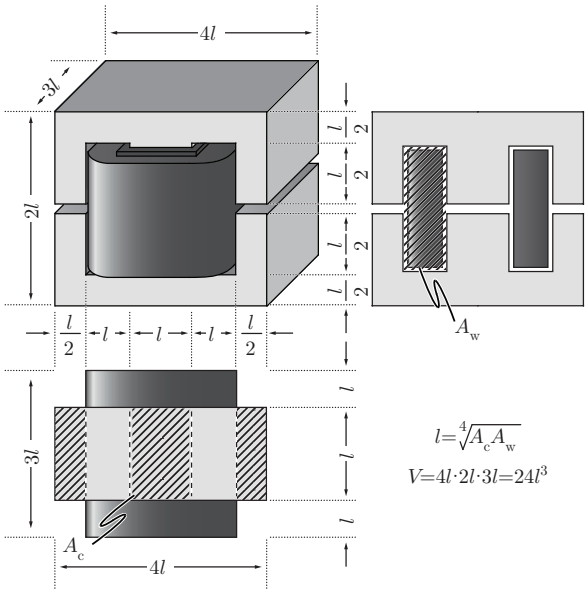

Fig. 5: Volume estimation model corresponding to an E core with area product $A_\mathrm{c}A_\mathrm{w}$. Assuming an E core according to the drawing with a characteristic core length $l = \sqrt[4]{A_\mathrm{c}A_\mathrm{w}}$ the total volume (i.e. including core and windings) can be approximated as $V = 24l^3$.

RMS current density $\tilde{J}$ and winding fill factor k) is

$$AP = A_\mathrm{c}A_\mathrm{w} = \frac{L\hat{I}_\mathrm{L}\tilde{I}_\mathrm{L}}{\hat{B}\tilde{J}k}. \tag{5}$$

Based on the AP (cm^4), which is independent of the core geometry, the characteristic core length $l = \sqrt[4]{A_\mathrm{c}A_\mathrm{w}}$ can be derived and subsequently utilized for the volume estimation of an E-core as $V \simeq 24l^3$ (cf. **Fig. 5**).

III. Comparison of Analytic Results

The presented semiconductor and inductor models are applied to the considered converter implementations. With reference to a permanent magnet synchronous machine (PMSM) a sinusoidal motor current $i_\mathrm{a} = \hat{I}_\mathrm{M}\sin(\omega_\mathrm{o}t)$ in phase with the motor AC voltage $u_\mathrm{an} = \hat{U}_\mathrm{M}\sin(\omega_\mathrm{o}t)$ (i.e. low motor reactive power consumption) is assumed, while the reactive power consumption of the different passive components (i.e. capacitors and inductors) is considered negligible for the sake of simplicity ($\hat{U}_\mathrm{o} = \hat{U}_\mathrm{M}$, $\hat{I}_\mathrm{o} = \hat{I}_\mathrm{M}$). A common switching frequency f_s is assumed for all the power semiconductor stages and a safety margin of $a_\mathrm{u} = 0.7$ is considered for the voltage rating U_r calculation of the semiconductor devices. A maximum allowed peak current ripple amplitude (i.e. half of the peak-to-peak value) to fundamental current ratio $a_\mathrm{i} = 0.25$ is considered for the inductive components analysis.

A. Boost VSI

The boost VSI solution utilizes a chip area $A_\text{DC-DC}$ for its interface boost DC-DC converter and a chip area $A_\text{DC-AC}$ for the inverter stage, while the total chip area is $A = A_\text{DC-DC} + A_\text{DC-AC}$. The DC-DC and DC-AC parts can be optimized independently according to the minimum chip area calculation algorithm of **Sec. II**. To this end, the loss dissipation equations specific to each converter stage are determined. In a first step, the losses of the DC-DC stage are derived as a function of its basic system operating parameters (cf. **Fig. 2**, DC-DC stage),

$$U_\mathrm{r} = \frac{U_\text{FC,max}}{a_\mathrm{u}},\ U = U^*_\text{DC},\ \tilde{I} = \frac{P}{U_\text{FC,min}},\ A = \frac{A_\text{DC-DC}}{2}, \tag{6}$$

where the inverter supply voltage is selected as $U^*_\text{DC} = 2\hat{U}_\mathrm{o} = 2\hat{U}_\mathrm{M}$. The losses are then calculated as

$$\begin{aligned} P_\text{DC-DC} &= \frac{r_\mathrm{ds}(U_\mathrm{r})}{A}\tilde{I}^2 + Ac_\mathrm{oss}(U_\mathrm{r})U^2 f_\mathrm{s} = \\ &\frac{2r_\mathrm{ds}(U_\mathrm{r})P^2}{A_\text{DC-DC}U^2_\text{FC,min}} + \frac{1}{2}c_\mathrm{oss}(U_\mathrm{r})A_\text{DC-DC}{U^*_\text{DC}}^2 f_\mathrm{s}. \end{aligned} \tag{7}$$

Subsequently, the losses of the DC-AC stage are derived (cf. **Fig. 2**, DC-AC stage) according to,

$$U_\mathrm{r} = \frac{U_\text{FC,max}}{a_\mathrm{u}},\ U = U^*_\text{DC},\ \tilde{I} = \frac{4P}{3\sqrt{2}U^*_\text{DC}},\ A = \frac{A_\text{DC-AC}}{6}, \tag{8}$$

as

$$\begin{aligned} P_\text{DC-AC} &= 3\left[\frac{r_\mathrm{ds}(U_\mathrm{r})}{A}\tilde{I}^2 + Ac_\mathrm{oss}(U_\mathrm{r})U^2 f_\mathrm{s}\right] = \\ &\frac{16r_\mathrm{ds}(U_\mathrm{r})P^2}{A_\text{DC-AC}{U^*_\text{DC}}^2} + \frac{1}{2}c_\mathrm{oss}(U_\mathrm{r})A_\text{DC-AC}{U^*_\text{DC}}^2 f_\mathrm{s}. \end{aligned} \tag{9}$$

The inductor volume of the DC-DC stage and the DC-AC stage are examined separately. First, the area product of the single DC-DC stage inductor is calculated based on

$$\hat{I}_\mathrm{L} = \tilde{I}_\mathrm{L} = \frac{P}{U_\text{FC,min}},\ L = \frac{U_\text{FC,min}(U^*_\text{DC} - U_\text{FC,min})}{2U^*_\text{DC}f_\mathrm{s}a_\mathrm{i}\hat{I}_\mathrm{L}}, \tag{10}$$

resulting in

$$AP_\text{DC-DC} = \frac{L\hat{I}_\mathrm{L}\tilde{I}_\mathrm{L}}{\hat{B}_\text{max}\tilde{J}_\text{max}k} = \frac{(U^*_\text{DC} - U_\text{FC,min})P}{2U^*_\text{DC}f_\mathrm{s}a_\mathrm{i}\hat{B}\tilde{J}k}, \tag{11}$$

and its volume $V_\text{DC-DC} = 24AP^{3/4}_\text{DC-DC}$ is estimated based on the model of **Fig. 5**. Afterwards, the area product of one out of three in total DC-AC stage inductors is derived considering

$$\hat{I}_\mathrm{L} = \frac{4P}{3U^*_\text{DC}},\ \tilde{I}_\mathrm{L} = \frac{4P}{3\sqrt{2}U^*_\text{DC}},\ L = \frac{{U_\text{DC}}^*}{8f_\mathrm{s}a_\mathrm{i}\hat{I}_\mathrm{L}}, \tag{12}$$

which gives

$$AP_\text{DC-AC} = \frac{L\hat{I}_\mathrm{L}\tilde{I}_\mathrm{L}}{\hat{B}_\text{max}\tilde{J}_\text{max}k} = \frac{\sqrt{2}P}{12f_\mathrm{s}a_\mathrm{i}\hat{B}\tilde{J}k}, \tag{13}$$

and the volume $V_\text{DC-AC} = 72AP^{3/4}_\text{DC-AC}$ is evaluated. Finally, the total inductors volume is calculated as $V = V_\text{DC-DC} + V_\text{DC-AC}$.

B. Buck CSI

The buck CSI solution utilizes a chip area $A_\text{DC-DC}$ for its front-end buck DC-DC converter and a chip area $A_\text{DC-AC}$ for the inverter stage, resulting in a total chip area $A = A_\text{DC-DC} + A_\text{DC-AC}$. The loss dissipation equation of the DC-DC stage (cf. **Fig. 2(b)**, DC-DC stage) follows considering

$$U_\mathrm{r} = \frac{U_\text{FC,max}}{a_\mathrm{u}},\ U = U_\text{FC,min},\ \tilde{I} = \frac{P}{U_\text{FC,min}},\ A = \frac{A_\text{DC-DC}}{2}, \tag{14}$$

as

$$\begin{aligned} P_\text{DC-DC} &= \frac{r_\mathrm{ds}(U_\mathrm{r})}{A}\tilde{I}^2 + Ac_\mathrm{oss}(U_\mathrm{r})U^2 f_\mathrm{s} = \\ &\frac{2r_\mathrm{ds}(U_\mathrm{r})P^2}{A_\text{DC-DC}U^2_\text{FC,min}} + \frac{1}{2}c_\mathrm{oss}(U_\mathrm{r})A_\text{DC-DC}U^2_\text{FC,min} f_\mathrm{s}. \end{aligned} \tag{15}$$

The CSI generates an AC current space vector (SV) by appropriately modulating the constant DC-link current I^*_DC, where the modulation

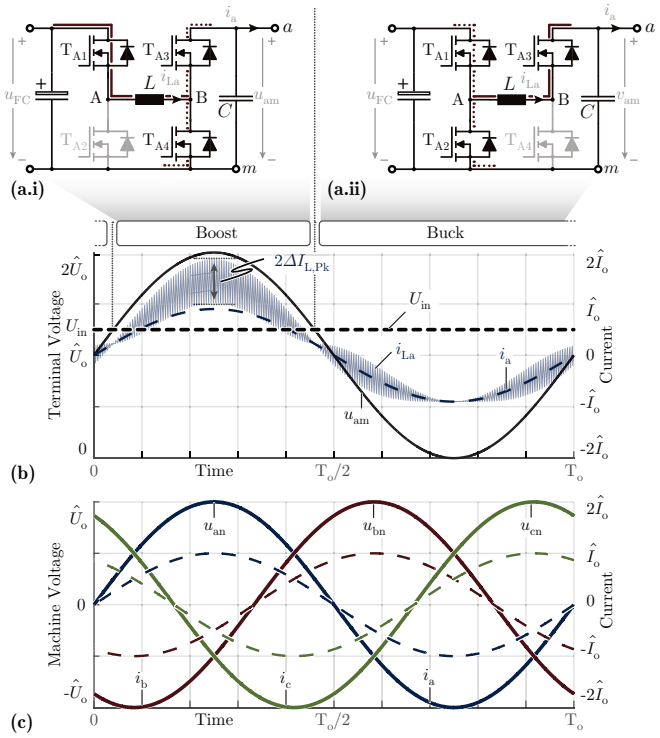

Fig. 6: Operating principle of a Y-inverter phase module and/or bridge-leg. In **(a.i)-(a.ii)**, the boost and buck operation are highlighted respectively. In **(b)** the generated voltage and current waveforms of phase-leg a are depicted, while the resulting sinusoidal motor currents and voltages are depicted in **(c)**.

depth of a CSI is defined as $M = \frac{\hat{I}_\mathrm{o}}{I^*_\mathrm{DC}} \in [0,1]$. To do so, the CSI semiconductor arrangement must provide bidirectional voltage blocking, i.e. has to be implemented using anti-series connected semiconductor devices which result in twice the conduction losses compared to a single semiconductor device (cf. **Fig. 2(b)**). The losses of the DC-AC stage are calculated considering

$$\begin{aligned} U_\mathrm{r} &= \frac{\sqrt{3}\hat{U}_\mathrm{o}}{a_\mathrm{u}},\ \tilde{I} = \frac{I^*_\mathrm{DC}}{\sqrt{3}} = \frac{P}{\sqrt{3}U_\mathrm{FC,min}},\ A = \frac{A_\mathrm{DC\text{-}AC}}{12} \\ U_1 &= \sqrt{\frac{3}{\pi}\int_{-\pi/6}^{+\pi/6}\left[\sqrt{3}\hat{U}_\mathrm{o}\cos(\phi)\right]^2 d\phi} = \hat{U}_\mathrm{o}\frac{\sqrt{3(2\pi+3\sqrt{3})}}{2\sqrt{\pi}} \\ U_2 &= \sqrt{\frac{3}{\pi}\int_{-\pi/6}^{+\pi/6}\left[\sqrt{3}\hat{U}_\mathrm{o}\sin(\phi)\right]^2 d\phi} = \hat{U}_\mathrm{o}\frac{\sqrt{3(2\pi-3\sqrt{3})}}{2\sqrt{\pi}}, \end{aligned} \tag{16}$$

which results in

$$\begin{aligned} P_\mathrm{DC\text{-}AC} &= 12\frac{r_\mathrm{ds}(U_\mathrm{r})}{A}\tilde{I}^2 + Ac_\mathrm{oss}(U_\mathrm{r})(U_1^2+U_2^2)f_\mathrm{s} = \\ &\frac{48r_\mathrm{ds}(U_\mathrm{r})P^2}{A_\mathrm{DC\text{-}AC}U^2_\mathrm{FC,min}} + \frac{1}{4}c_\mathrm{oss}(U_\mathrm{r})A_\mathrm{DC\text{-}AC}\hat{U}_\mathrm{o}^2 f_\mathrm{s}. \end{aligned} \tag{17}$$

The CSI approach benefits from a reduced number of passive components since only one DC side inductor is required. However, this inductor must maintain a low current ripple in order to ensure stable operation and reasonably low output voltage distortion. Namely, $a_\mathrm{i,CSI} = 7.5\%$ is considered as the upper bound of the peak current ripple to related DC inductor current ratio [16], which leads to a comparably large inductor volume. The area product inductor scaling is derived considering

$$\begin{aligned} \hat{I}_\mathrm{L} = \tilde{I}_\mathrm{L} = \frac{P}{U_\mathrm{FC,min}},\ M = \frac{\hat{I}_\mathrm{o}}{{I_\mathrm{DC}}^*} = \frac{2U_\mathrm{FC,min}}{3\hat{U}_\mathrm{o}} \\ L_\mathrm{DC} = \frac{U_\mathrm{FC,min}}{8f_\mathrm{s}a_\mathrm{i,CSI}\hat{I}_\mathrm{L}},\ L_\mathrm{AC} = \frac{U_\mathrm{FC,min}\left(1-\frac{\sqrt{3}}{2}M\right)}{2f_\mathrm{s}a_\mathrm{i,CSI}\hat{I}_\mathrm{L}}, \end{aligned} \tag{18}$$

and results as

$$AP_\mathrm{DC\text{-}DC} = \frac{(L_\mathrm{DC}+L_\mathrm{AC})\,\hat{I}_\mathrm{L}\tilde{I}_\mathrm{L}}{\hat{B}_\mathrm{max}\tilde{J}_\mathrm{max}k} = \frac{\left(\frac{5}{4}-\frac{\sqrt{3}}{2}M\right)P}{2f_\mathrm{s}a_\mathrm{i,CSI}\hat{B}\tilde{J}k}, \tag{19}$$

resulting in a volume $V = V_\mathrm{DC\text{-}DC} = 24AP^{3/4}_\mathrm{DC\text{-}DC}$.

C. Y-Inverter

The Y-inverter shows a modular structure and employs three identical buck-boost DC-DC converter modules connected to a common star point [17]–[20] i.e. attached to the negative DC-rail m (cf. **Fig. 2(c)**). This arrangement is ideal for fuel-cell powered high-speed motor drives thanks to two key features. Firstly, it provides a continuous AC output voltage which eliminates the need of a dedicated output filter. Secondly, due to its buck-boost characteristic, the DC input voltage can be higher or lower than the AC output voltage with a single energy conversion stage, i.e. without requiring a interface DC-DC converter.

Each phase is comprised of two half-bridges connected to the opposite terminals of an inductor L, and an output capacitance C placed between the corresponding AC output terminal a, b, c and the negative DC-rail m, which, as already mentioned forms a common star (Y) point among the three phases. In order to generate the sinusoidal phase a motor voltage $u_\mathrm{an} = \hat{U}_\mathrm{o}\sin(\omega t) = M\frac{U_\mathrm{FC,min}}{2}\sin(\omega t)$, the converter phase module generates a strictly positive terminal voltage $u_\mathrm{am} = \hat{U}_\mathrm{o}\sin(\omega t) + \hat{U}_\mathrm{o} = M\frac{U_\mathrm{FC,min}}{2}(1+\sin(\omega t))$, i.e. a sinusoidal voltage with a constant offset, where the modulation depth M can exceed value $M = 1$ (cf. **Fig. 6(b)**). The left half-bridge (T_A1, T_A2) of the phase module is dedicated to buck converter operation ($u_\mathrm{am} \leq U_\mathrm{FC}$, cf. **Fig. 6(a.ii)**), while the right hand side bridge (T_A3, T_A4) is exclusively used for boost operation ($u_\mathrm{am} > U_\mathrm{FC}$, cf. **Fig. 6(a.i)**). The buck and boost bridge-legs are operated in a mutually exclusive fashion, meaning that only one of the two bridge-legs is pulse width modulated (PWM) at a time, while the top side switch of the second bridge is clamped to an active on-state. Namely, the buck bridge-leg (T_A1,T_A2) is switched for the fraction $t_\mathrm{A} = \frac{2\pi-2\phi_\mathrm{o}}{2\pi}T_\mathrm{o}$ of the fundamental period T_o, while the boost bridge-leg (T_A3,T_A4) is switched for $t_\mathrm{B} = \frac{2\phi_\mathrm{o}}{2\pi}T_\mathrm{o}$, where $\phi_\mathrm{o} = \cos^{-1}\left(\frac{2}{M}-1\right)$. A detailed analysis and verification of the Y-inverter concept is given in [10].

The Y-inverter solution utilizes a total semiconductor chip area $A = A_\mathrm{DC\text{-}AC}$ which is assumed to be equally distributed to the buck and boost half-bridges. The semiconductor losses of the buck bridge-legs are calculated considering

$$U_\mathrm{r} = \frac{U_\mathrm{FC,max}}{a_\mathrm{u}},\ U = U_\mathrm{FC,min},\ \tilde{I} = \tilde{I}_\mathrm{L},\ A = \frac{A_\mathrm{DC\text{-}AC}}{12}, \tag{20}$$

and result in

$$\begin{aligned} P_\mathrm{DC\text{-}AC,1} &= 3\left[\frac{r_\mathrm{ds}(U_\mathrm{r})}{A}\tilde{I}^2 + Ac_\mathrm{oss}(U_\mathrm{r})U^2 f_\mathrm{s}\frac{2\pi-2\phi_0}{2\pi}\right] = \\ &\frac{36r_\mathrm{ds}(U_\mathrm{r})\tilde{I}_\mathrm{L}^2}{A_\mathrm{DC\text{-}AC}} + \frac{1}{4}c_\mathrm{oss}(U_\mathrm{r})A_\mathrm{DC\text{-}AC}U^2_\mathrm{FC,min}f_\mathrm{s}\frac{2\pi-2\phi_0}{2\pi}. \end{aligned} \tag{21}$$

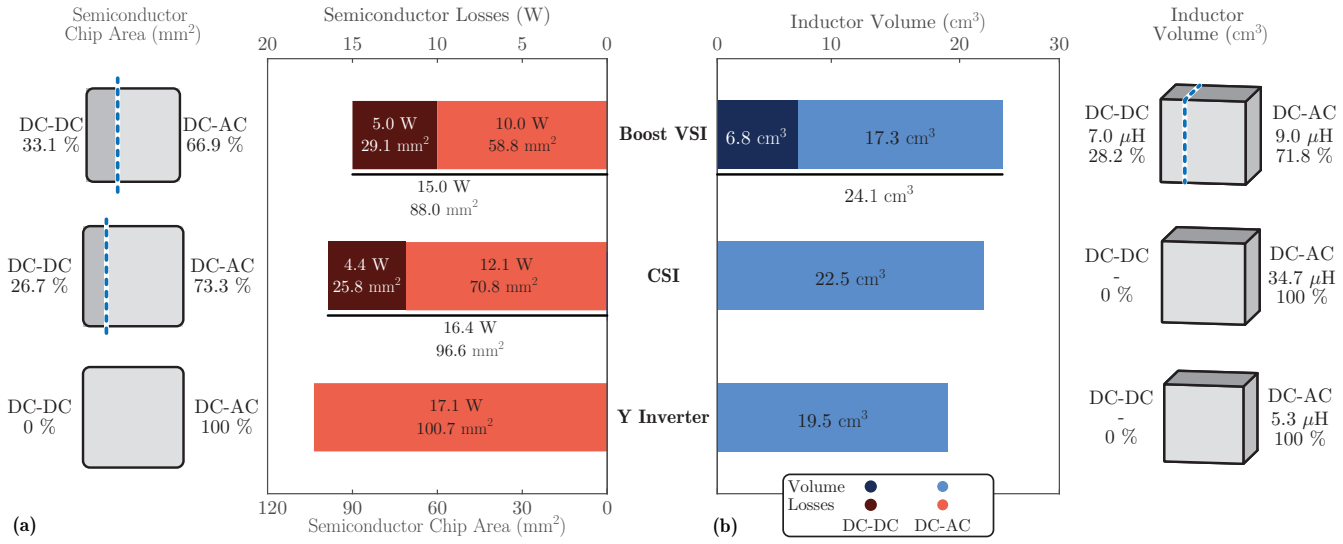

Fig. 7: Comparison of the conventional boost VSI and buck CSI motor drive implementations (cf. **Fig. 2(a)-(b)**) against the Y-inverter (cf. **Fig. 2(c)**) based on fundamental scaling laws of semiconductors and inductors. In **(a)** the minimum achievable semiconductor chip area of the different solution as well as the corresponding semiconductor losses are illustrated. In **(b)** the inductive components volume are shown. The parameter values $a_\mathrm{u} = 0.7$, $a_\mathrm{i} = 25\%$, $a_\mathrm{i,CSI} = 7.5\%$, $\hat{B} = 350\,\mathrm{mT}$, $\tilde{J} = 5\,\mathrm{A\,mm^{-2}}$, $k = 60\%$ are considered for the calculations.

The loss dissipation of the boost bridge-legs follows with

$$\begin{aligned} U_\mathrm{r} &= \frac{2\hat{U}_\mathrm{o}}{a_\mathrm{u}},\ \tilde{I} = \tilde{I}_\mathrm{L},\ A = \frac{A_\mathrm{DC\text{-}AC}}{12} \\ U &= \sqrt{\frac{1}{2\phi_0}\int_{-\phi_0}^{+\phi_0}\left[\hat{U}_\mathrm{o}(1+\cos(\phi))\right]^2 d\phi} = \\ &\hat{U}_\mathrm{o}\sqrt{\frac{3\phi_\mathrm{o}+\sin(\phi_\mathrm{o})(\cos(\phi_\mathrm{o})+4)}{2\phi_\mathrm{o}}} \end{aligned} \tag{22}$$

as

$$\begin{aligned} P_\mathrm{DC\text{-}AC,2} &= 3\left[\frac{r_\mathrm{ds}(U_\mathrm{r})}{A}\tilde{I}^2 + Ac_\mathrm{oss}(U_\mathrm{r})U^2 f_\mathrm{s}\frac{2\phi_0}{2\pi}\right] = \\ &\frac{36 r_\mathrm{ds}(U_\mathrm{r})\tilde{I}_\mathrm{L}^2}{A_\mathrm{DC\text{-}AC}} + \frac{1}{4}c_\mathrm{oss}(U_\mathrm{r})A_\mathrm{DC\text{-}AC}U^2 f_\mathrm{s}\frac{2\phi_0}{2\pi}. \end{aligned} \tag{23}$$

Finally, the total semiconductor losses are calculated as $P_\mathrm{DC\text{-}AC} = P_\mathrm{DC\text{-}AC,1} + P_\mathrm{DC\text{-}AC,2}$. The filter inductors scaling is afterwards derived considering

$$\begin{aligned} &\hat{I}_\mathrm{L} = M\hat{I}_\mathrm{o} = \frac{4P}{3U_\mathrm{FC,min}},\ \tilde{I}_\mathrm{L} \simeq M\tilde{I}_\mathrm{o} = \frac{4P}{3\sqrt{2}U_\mathrm{FC,min}}, \\ &L = \begin{cases} \dfrac{U_\mathrm{FC,min}}{8 f_\mathrm{s} a_\mathrm{i}\hat{I}_\mathrm{L}}, M < \dfrac{4}{3} \\ \dfrac{(M-1)U_\mathrm{FC,min}}{2M f_\mathrm{s} a_\mathrm{i}\hat{I}_\mathrm{L}}, M > \dfrac{4}{3} \end{cases}, \end{aligned} \tag{24}$$

as

$$AP_\mathrm{DC\text{-}AC} = \begin{cases} \dfrac{\sqrt{2}P}{12 f_\mathrm{s} a_\mathrm{i}\hat{B}\tilde{J}k}, M < \dfrac{4}{3} \\ \dfrac{\sqrt{2}(M-1)P}{3M f_\mathrm{s} a_\mathrm{i}\hat{B}\tilde{J}}k, M > \dfrac{4}{3}. \end{cases}, \tag{25}$$

where the modulation depth is defined as $M = \frac{\hat{U}_\mathrm{o}}{\frac{U_\mathrm{FC,min}}{2}}$. The inductor volume is hence $V = V_\mathrm{DC\text{-}AC} = 72AP_\mathrm{DC\text{-}AC}^{3/4}$

D. Comparison

The drive system implementations are compared for a switching frequency of $f_\mathrm{s} = 300\,\mathrm{kHz}$ and a relative peak current ripple of $a_\mathrm{i} = 25\%$ for all DC-DC and DC-AC converters except for the CSI where the peak current ripple has to be reduced to $a_\mathrm{i,CSI} = 7.5\%$ for the reasons stated above. Utilizing the expressions **(6)**-**(25)**, the semiconductor losses and the volume of the inductive components are resulting as visualized in **Fig. 7**. As can be noted, the boost stage of the boost VSI roughly increases both the semiconductor losses and the inductor volume by 30% compared to the VSI stage. In contrast, for the buck CSI, the already existing boost inductor can be used for the precedent buck stage and only the buck half-bridge has to be added to the CSI. Hence, only the semiconductor losses are slightly increased by around 25%, which means that the performance - mainly in terms of efficiency - is only slightly decreased compared to the conventional CSI.

Comparing the different topologies, it can be noted that based on the given assumptions the boost VSI results in the smallest chip area (-14% compared to the Y-inverter) and therefore the lowest semiconductor losses and costs are achieved. Surprisingly, the chip area of the buck CSI and the Y-inverter are quasi identical, even if the number of semiconductors in the conduction path is higher for the CSI than for the Y-inverter. This can be explained by the larger switching losses of the Y-inverter: Namely, three hard switching transition per switching period f_s occur for the Y-inverter instead of only two for the CSI, while on average the Y-inverter is switching a higher output voltage (sinusoidal with DC offset) compared to the buck CSI (line-to-line sinusoidal motor voltage). On the other hand, with the Y-inverter the smallest overall inductor volume is achieved, whereas the inductor of the buck CSI is slightly bigger ($+15\%$). The largest inductor is resulting for the boost VSI, which compared to the Y-inverter increases the volume by roughly $+24\%$.

The Y-inverter and the VSI stage of the boost VSI could be operated with phase clamping modulation where always only two out of three phases are switching and one phase remains in a continuous on-state. This mode of operation would reduce the switching losses but is not considered here for the sake of simplicity.

In general, it can be noticed that the Y-inverter and the buck CSI achieve similar performance concerning power density and efficiency,

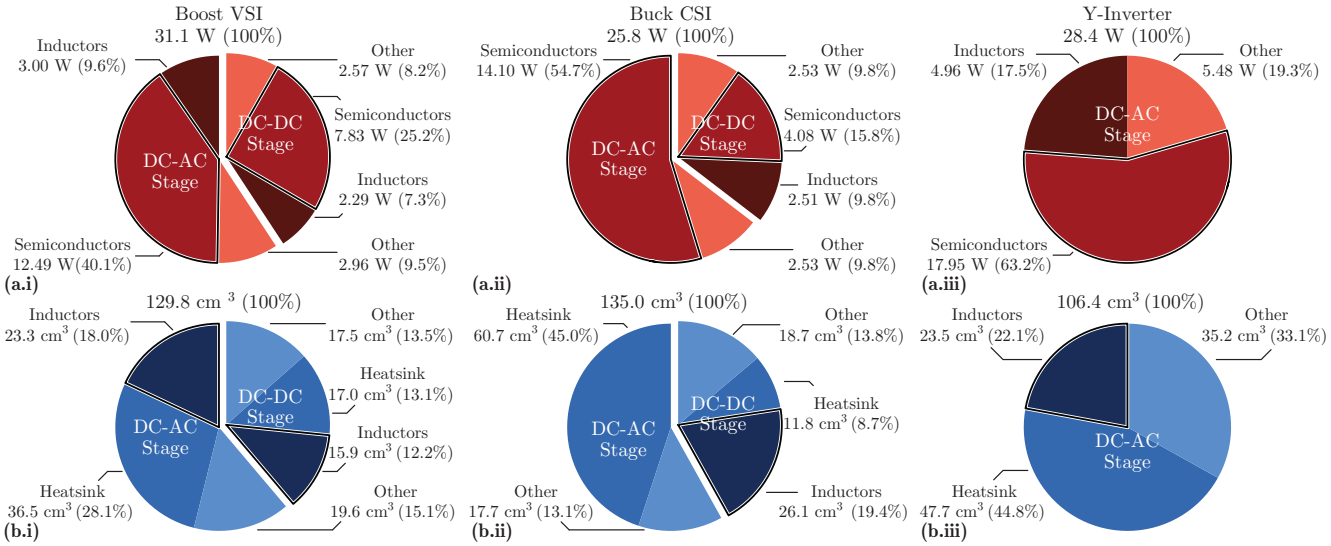

Fig. 8: Comparative break-down of **(a)** the volume and **(b)** the losses corresponding to the three converter approaches of **Fig. 2**.

which is not particularly surprising, since both topologies feature the same buck-boost structure with integrated output filter, whereas the Y-inverter basically only constitutes the phase modular approach of the buck CSI. Furthermore, also the boost VSI achieves a considerable high overall performance with highest efficiency, but lowest power density. Due to the fact that for the given criterion all topologies achieve similar performance, only general statements can be given, but no clear trend with the exclusion of one or several topologies is visible. Therefore, in a further step, the loss and volume calculations as well as the models of the semiconductors and inductors are refined, which means that e.g. also the high-frequency losses and the thermal aspects in the inductor winding and core are considered. Furthermore, also the additional circuit components like capacitors, control and measurement circuits, auxiliary supplies and heatsink are taken into account.

IV. Multi Objective Optimization Results

A. Minimum Chip Area, Area Product Optimization

As already discussed, the three converter topologies are optimized again for the same design criterion (i.e. minimum chip area, area product) and the same specifications (e.g. $f_s = 300\,\text{kHz}$), whereas for the dimensioning of the individual components on the one hand all electric (e.g. high-frequency effects), magnetic (e.g. flux densities), mechanical (e.g. heatsink dimensions, interconnections, spacings between components or design rules) and thermal constraints (e.g. junction, core and winding temperatures) are considered [21], [22] and on the other hand only real and commercially available components (semiconductor devices with discrete voltage and current ratings, discrete core sizes and core types, solid and litz wire diameters with discrete numbers of strands, capacitors with discrete voltage and capacitance values) are used.

The comparative loss and volume breakdowns of the three designs are presented in **Fig. 8(a),(b)**.

At first glance it can be noted that the major part $(63 - 70\%)$ of the overall losses is really generated in the semiconductors. The reason for this lies also in fact that the converters are optimized concerning a minimum chip area and therefore the optimization leads to a design with maximum allowable semiconductor losses per chip. In analogy to the analytical scaling laws, the total semiconductor losses of the Y-inverter and the buck CSI are practically identical $(18\,\text{W})$ and the losses generated in the buck stage of the buck CSI constitute approximately one quarter of the total semiconductor losses. The slight mismatch in the absolute values can be explained by the more detailed calculation of the switching losses, where the switching losses also scale with the switched current. Surprisingly, the highest semiconductor losses of around $20\,\text{W}$ are found in the boost VSI, since the scaling laws predicted the lowest semiconductor losses for this topology. The reason for this is given by the fact that now in the accurate design only semiconductor components with discrete chip size can be used and therefore the investigated converters cannot reach their theoretically calculated chip area (cf. **Fig. 7**). The CSI for example employs 12 semiconductor devices with $150\,\text{V}$ rating: The smallest commercially available $150\,\text{V}$ MOSFET is the EPC2033 with chip area of $12\,\text{mm}^2$. Therefore the smallest possible total CSI chip area is $A_{\text{DC-AC}} = 12 \cdot 12 = 144\,\text{mm}^2$ which is twice the theoretical value of $70.8\,\text{mm}^2$ (cf. **Fig. 7**). The larger chip area allows for lower conduction and therefore lower overall semiconductor losses for the buck CSI concept. In contrast the VSI employs 6 EPC2034 $200\,\text{V}$ rated switches with total chip area $A_{\text{DC-AC}} = 6 \cdot 12 = 72\,\text{mm}^2$ which is much closer to the theoretically derived value of $58.8\,\text{mm}^2$ (cf. **Fig. 7**). Therefore, the commercial devices chip area discretization artificially favors the buck CSI (as well as the Y-inverter) in terms of losses.

The relatively high semiconductor losses in all topologies are also reflected in the volume distribution, since for the cooling of the switching devices a relatively large heatsink is needed, which in all designs roughly consumes $1/3$ of the overall volume. The equal share of the heatsink volume confirms that it is permissible to neglect this component in the first calculation with the scaling laws. However, the heatsink volume could also be easily considered with a defined cooling system performance index (CSPI) [23].

The comparison of the precise calculation with the simple scaling laws also reveal that the inductor volume of the Y-inverter is the smallest, whereas the one of the buck CSI is around 11% larger. The largest inductor volume ($+66\%$ compared to the Y-inverter) is still consumed by the boost VSI, where 40% instead of 30% is accounted to the boost inductor. Nevertheless, it can be shown that these relative comparisons nicely match with the scaling laws. For the

given case, this is also true concerning the absolute inductor volumes, which means that the different inductor volumes calculated with the scaling laws only differ by $-15...-25\%$ compared to the accurate calculation (expect the boost inductor deviates by -50%). There the major challenge of the inductor area product is to select a reasonable current density $\tilde{J}$, since there are no thermal constraints and thus the current density can be arbitrarily chosen. Hence, the area product only gives a reliable statement concerning the relative inductor volumes, however, to get a prediction of the correct absolute inductor volumes is difficult and therefore these results should be treated with caution.

In general, the accurate calculation also reveals that for the considered output power of $1\,\mathrm{kW}$ in all converter topologies 20% of losses are generated by additional components like measurement and control circuits, auxiliary supplies, PCB and capacitors. Hence, in the analytic calculation based on the scaling laws, these losses can be neglected, since they only result in an offset in the loss balance. The same can be applied to the volume consumed by these components, which in all designs is roughly 35% of the overall volume.

In summary, with all topologies similar overall efficiencies and power densities are achieved. Interestingly, the buck CSI exhibits the highest efficiency (97.4%), while the Y-inverter is only slightly worse (97.2%). The difference is found in the inductor losses, because the inductor of the buck CSI only conducts a DC current and the inductors of the Y-inverter are excited with a sinusoidal current. The lowest efficiency (96.9%) is resulting for the boost VSI, but it has to be mentioned again that GaN devices with larger chip size had to be used. On the other hand, the Y-inverter features the highest power density ($9.3\,\mathrm{kW/dm^3}$). Compared to this, the volume of the buck CSI is around 30% larger ($7.4\,\mathrm{kW/dm^3}$) and even exceeds the volume of the boost VSI by 4% ($7.7\,\mathrm{kW/dm^3}$).

B. $\eta\rho$-Pareto Front Optimization

The previously discussed optimization concerning minimum chip area and area product fits the low cost needs of industry applications and hence the converter designs derived from such optimization are from now on denoted as industrial designs. The industrial designs of **Fig. 8** exhibit similar performances in terms of converter efficiency η and power density ρ. Now, the question arises how much these performance indexes can be increased compared to the industrial designs if further degrees of freedom (i.e. arbitrary chip size, switching frequency $f_\mathrm{s} \in [200\,\mathrm{kHz}, 600\,\mathrm{kHz}]$, passive component values L,C) are considered. Therefore, a multi-objective optimization routine with respect to converter efficiency η and power density ρ is examined. The η-ρ Pareto limits of the different converter candidates are depicted in **Fig. 9**, whereas the following performance trends can be identified: The boost VSI quickly reaches a power density threshold because of the volume contribution related to the DC-DC stage. At the nominal operating point, where the boost stage must step-up the FC voltage to the greatest degree, the semiconductors are switching the DC voltage U_DC^* and the boost inductor is exposed to large voltage-time-areas resulting in high losses. Therefore, the boost VSI is outperformed by the two other solutions. Compared to the industrial design with minimum chip area, the efficiency can be increased by around 0.5% for the same power density. On the other hand, for the same efficiency the power density could be increased by 23%.

The buck CSI achieves a high efficiency by paralleling several MOSFETs per switch, which mitigate the conduction losses. Hence, the efficiency can be raised to roughly 98.3%, i.e. almost $+1\%$, compared to an industrial design. However, this low loss profile is achieved at the expense of substantially increased semiconductor cost, which might be impractical for industry. Furthermore, the low DC-link current ripple condition ($a_\mathrm{i,CSI} = 7.6\%$) leads to a bulky inductor design which compromises the overall power density.

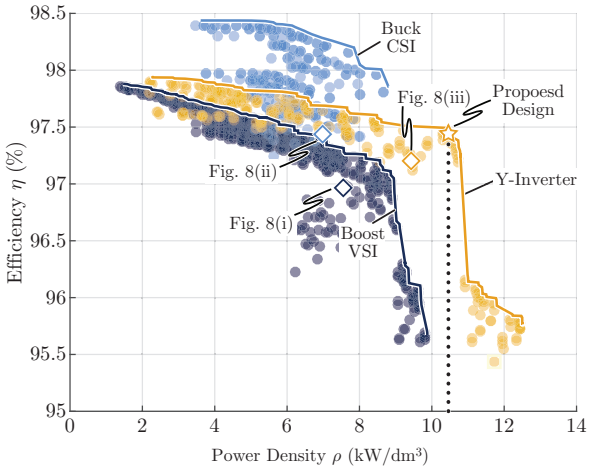

Fig. 9: The efficiency (η) power density (ρ) Pareto optimization results for the different candidate converter concepts of **Fig. 2**.

Finally, the Y-inverter breaks through the power density barriers of the other systems, while a high efficiency can be maintained. At the same power density as the industrial design, the efficiency can be increased to around 97.5%. A reasonable Y-inverter benchmark design would achieve an efficiency of $\eta = 97.2\%$ and a power density of $\rho = 10.5\,\mathrm{kW/dm^3}$ as highlighted in **Fig. 9**. It should be mentioned that this performance is achieved with conventional PWM, which results in hard-switching. In a future step, a trapezoidal current modulation (TCM) as proposed in [24] could be implemented, which enables soft-switching operation at constant switching frequency and further reduces the needed volume of the inductors. Hence, besides the advantages of modularity, scalability and high power density also a high efficiency, comparable to the buck CSI, can be achieved.

V. Conclusions

A comparative evaluation of different converter concepts is performed within the context of a fuel-cell powered motor drive application. Namely, the recently proposed Y-inverter is compared against traditional voltage source (boost VSI) and current source inverter based (buck CSI) approaches. First, a preliminary analysis is performed based on fundamental scaling laws of semiconductor devices and inductive components, which are the main contributors of losses and volume respectively. The analytic nature of the underlying semiconductor and inductor models enables a fair and intuitive relative comparison of the investigated converters, however, the absolute volume and losses calculation have limited accuracy. For this reason, in order to identify the exact efficiency (η) vs. power density (ρ) Pareto limits of the investigated converter implementations (including the remaining system components in addition to semiconductor devices and inductors) a comprehensive converter optimization routine is employed. Both the analytic calculations and the precise Pareto optimization indicate a considerable power density gain in favor of the Y-inverter with a small decrease in efficiency compared to the traditional solutions. The reason behind the low Y-inverter volume is its integrated filter structure (with minimal inductive components number) and the buck-boost modular approach it follows. A trapezoidal current modulation (TCM) would be an effective measure for efficiency improvement of the Y-inverter that should be carefully analyzed in future research.

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