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***Abstract*—Integrated Voltage Regulators (IVRs) have become a viable solution for microprocessor's power delivery. The active parts of the most recent IVRs are built in deep-submicron CMOS technologies and use stacked transistors to allow for the use of advanced low voltage devices with superior switching performance compared to the higher voltage long-channel devices. This paper evaluates three different topologies of CMOS half-bridge converters with respect to efficiency, implementation effort, suitability for on-chip integration, and multiphase applications: the conventional half-bridge converter, the half-bridge converter with conventional Active Neutral Point Clamping (ANPC), and a half-bridge converter with a modified circuit to achieve ANPC. In-depth analysis of the transient processes during switching for all three converters, based on Cadence simulations, reveal that both half-bridge converters with ANPC achieve proper balancing of the blocking voltages of the main transistors and are capable to attain similar efficiencies of 93% at an output power of 200 mW, input and output voltages of 1.6 V and 0.8 V, respectively, and a switching frequency of 150 MHz, which is 1% higher than the one attained with the conventional half-bridge converter. Of the two ANPC half-bridge converters, however, the proposed topology allows to completely turn off its entire power stage or parts of it, features less efficiency sensitivity to variations of dead-time, and achieves the peak efficiency at relatively higher dead-time values. These qualities render the proposed topology particularly suitable for multiphase systems and low load operation.**

***Index Terms*—IVR, CMOS, Stacked Transistors, Half-Bridge, Multiphase, 14 nm Technology**

I. Introduction

VRMs built fully on-chip, or with a combination of components residing on-chip, on-package and/or soldered on a PCB are denoted Integrated Voltage Regulators (IVRs). These Voltage Regulators (VR) became an attractive solution in microprocessor applications due to their very high achievable power density compared to off-chip VR and efficiency compared to linear regulators. These power converters use a single high voltage domain, commonly greater than the transistor's short channel device breakdown voltage available in the chip technology node, to power all the necessary voltage domains of the microprocessor. The IVRs allow for simplification and cost reduction of the motherboard, and improvements of the transient responses on output load and reference voltage changes. The active parts of the IVR's power stage are normally implemented using complementary transistors and can be composed of high voltage long-channel devices or of stacked short-channel devices (cf. **Fig. 1 (a)**). Compared to the realizations with long-channel devices, the stacked configuration allows the use of the low voltage transistors of the technology node that features better Figure of Merit FOM ($Q_{\mathrm{g}} \cdot R_{\mathrm{ds,on}}$) [1]. Moreover, the charge recycling mechanism, explained in [2], reduces the gate drive losses, which is beneficial with regard to high conversion efficiency at high switching frequencies.

To reduce high currents flowing from the motherboard to the microprocessor's package, it is desirable to use the highest input voltage possible that does not violate the maximum transistor's threshold voltage and ensure equal voltage distribution among the series-connected devices. The two-level Half-Bridge with Stacked Transistors (HBST) configuration of Fig. 1 (a), proposed in [2], has been employed successfully in many of Intel's IVRs using FinFet 22 nm technology [3], [4]. Most recently, Intel also proposed a fully integrated voltage regulator with power transistors, decoupling capacitors, and inductors in the same die [5] using the HBST of Fig. 1 (a), but using 14 nm technology. This configuration, however, does not assure equal voltage distribution among the devices and voltage spikes might occur during and after the switching transient [6], which reduces system reliability, efficiency, and lifetime. To avoid voltage unbalancing, clamping transistors can be added to the conventional CMOS HBST to actively clamp the potential between two stacked transistors to the middle potential [7] (cf. **Fig. 1 (b)**). In this approach, denoted conventional Active Neutral Point Clamping (ANPC) HBST, still only two gate drivers are required, since same gate potentials apply to the main switches and their respective clamping switches. Compared to the conventional HBST, the conventional ANPC HBST generates additional switching losses since the clamping switches conduct the load current during the dead-time interval, which can increase the total losses if large dead-time values are used, as explained in Sec. III-A of this paper. Furthermore, by reason of the gates of main and clamping switches being connected, soft-switching of the main switches cannot be utilized and, during the turn-off transients, additional switching losses are generated on the clamping switches. Finally, the conventional ANPC HBST does not allow complete turn-off in on-line operation, therefore it is not suitable for multiphase systems that employ phase-shedding.

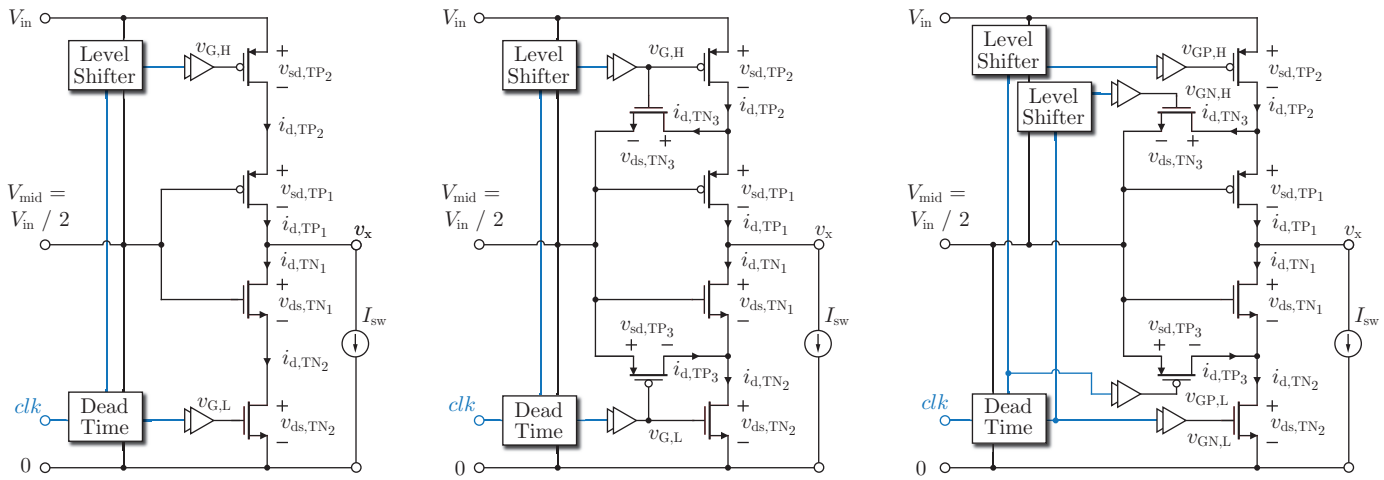

Fig. 1: Schematic representations of two-level HB power stages of IVRs in stacked configurations, including the dead-time controller and level-shifters. **(a)** Conventional HB with Stacked Transistors (Conventional HBST). **(b)** Conventional Neutral Point clamped HB with Stacked Transistors (Conventional ANPC HBST). **(c)** Proposed Neutral Point clamped HB with Stacked Transistors (Proposed ANPC HBST).

This Paper proposes a modified ANPC HBST (**Fig. 1 (c)**) built using FinFet CMOS technology, which allows for soft-switching of the main switches and features voltage balancing among the devices and phase-shedding capability. **Section II** summarizes the specifications of the investigated converters and describes a versatile on-chip implementation of the power stage, which enables the emulation of all three considered topologies. The switching transients are explained in **Section III** to gain in-depth understanding of the present switching operations. Finally, in **Section IV**, the three converters (conventional HBST, conventional ANPC HBST, and proposed ANPC HBST) are evaluated in the scope of efficiency and losses breakdown comparison. According to Cadence simulation results, using a 14 nm CMOS process environment, the conventional and the proposed ANPC power stages achieve similar efficiencies of 93% at optimum dead-times (simulated for a switching frequency of 150 MHz, an input voltage of 1.6 V, a duty-cycle of 50%, and a turn-on dead-time of 40 ps) which is 1% higher than for the conventional HBST at same conditions. However, the proposed ANPC HBST is suitable for multiphase systems and low load operation, since its entire power stage (or parts of it) can be completely turned off. Compared to the conventional ANPC HBST, a flatter and less sensitive to dead-time variations efficiency curve is obtained.

II. Specifications and Power Stage Layout

The considered IVR is composed of a four-phase buck converter. Each phase of this buck converter employs a power stage, which is formed by slices that can be replicated in order to achieve the desired output power, to assure a symmetrical design, and to obtain a compact and scalable layout. **Tab. I** lists the specifications of a single phase of the considered IVR.

Fig. 2 (a) depicts the chip layout of the designed power stage of one phase, using 14 nm technology. The power stage is designed to operate with switching frequencies up to 250 MHz.

Tab. I: Specifications of a single phase of the considered IVR.

Parameters	Symbol	Value
Input voltage	V_{in}	1.6 V
Output voltage	V_{in}	0.8 V
Output power	P_{out}	200 mW
Max. output voltage	$V_{\text{out,max}}$	1.0 V
Min. output voltage	$V_{\text{out,min}}$	0.6 V
System overall min. efficiency	η	$> 90\%$
System overall min. power density	ρ	$> 1\,\text{W/mm}^2$

Fig. 2 (b) shows the corresponding schematic drawing with main transistors ① and ⑤, clamping transistors ② and ⑥, multi-stage tapered gate drivers ③, ④, ⑦, ⑧, ⑨, and level shifter ⑨. According to Fig. 2 (a) the gate driver is located very close to main and clamping transistors to achieve the required high peak currents by reason of comparably high input capacitances of the power transistors. The presented design employs four stages of gate drivers, which is found to offer a reasonable compromise between the maximum achievable switching speed of the main transistors and the total power consumption of all gate driver stages. The addition of the clamping transistors and their respective gate-drivers corresponds to approximately 20% area increase compared to the conventional HBST topology. To implement the proposed ANPC HBST from the conventional ANPC HBST, the gate-driver stage is splited into two, i.e. no additional area is required for gate-drivers, and another level-shifter is added.

III. Waveforms During Switching Transients

The investigated IVR is expected to generate substantial switching losses, due to the considered very high switching frequencies. Hence, in order to attain in-depth understanding of the switching operations and clarify topology-dependent limitations related to switching (e.g. unbalanced blocking voltages in case of the conventional HBST, efficiency-optimal dead-time values), this Section details the transient processes

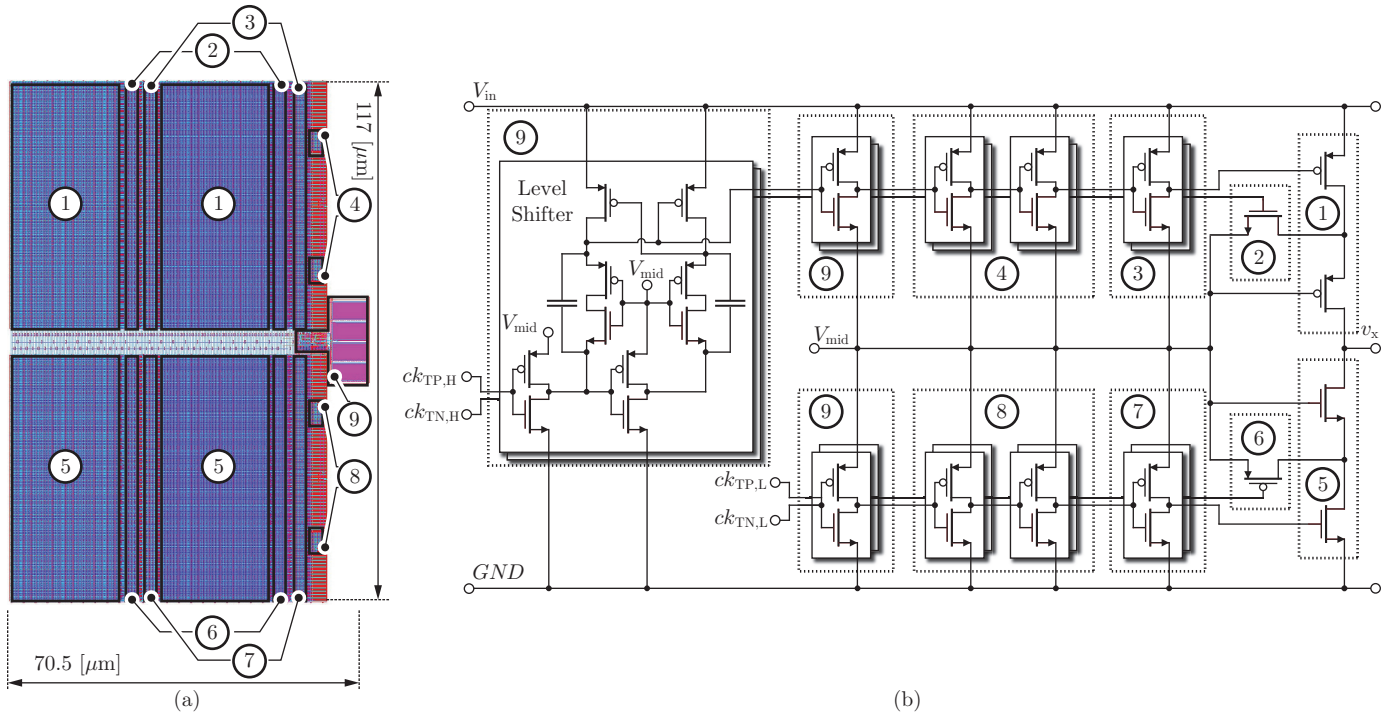

Fig. 2: (a) Layout picture of the designed the ANPC HBST power stage. **(b)** Schematic representation of the layout picture of Fig. 2 (a)).

that take place during switching. The presented discussion is based on simulation results obtained with the Cadence software tool.[1]

Fig. 3 depicts the investigated converter topologies with the body diodes of the power switches being included – only the transistors' parasitic capacitances have not been included for the sake of clarity. This equivalent circuit serves for explaining technology-specific details that appear in the presented switching waveforms. Two body diodes, which connect each transistors drain and source potentials to the substrate, are present for each MOSFET and the substrates of all PMOS and NMOS transistors are connected to V_{in} and 0, respectively, in order to assure that the diodes block during steady-state operation. Furthermore, all transistors are symmetric with regard to drain and source, i.e., gate-source and gate-drain voltages can control the MOSFET channel. Thus, same values for gate-source and gate-drain capacitances, $C_{gs} = C_{gd}$, apply. The drain-source capacitance, C_{ds}, is different and much less than C_{gs} and C_{gd}. For the main transistors, TP_1, TP_2, TN_1, and TN_2, equal chip areas apply. The chip area of each clamping transistor, TP_3 and TN_3, is 10% of the area of a main transistor, due to significantly lower current stresses. Thus, the clamping transistors' on-state resistances are approximately ten times higher than those of the main transistors.

Depending on the slope of the output voltage, $v_x(t)$, two entirely different switching operations are observed. For this reason, the explanation given in this Section distinguishes between case 1 (v_x changes from V_{in} to 0) and case 2 (v_x changes from 0 to V_{in}). Constant output current of 250 mA applies during the switching transients.

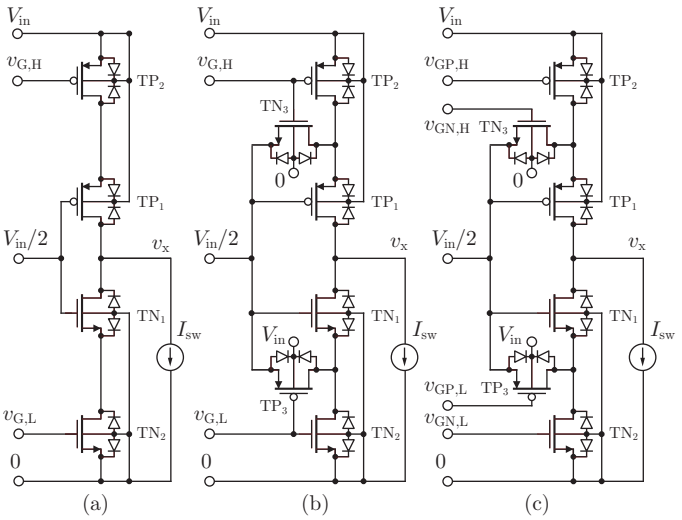

Fig. 3: Illustration of the converters' equivalent circuits, where two opposite series connected diodes are present in parallel to each transistor: **(a)** conventional HBST, **(b)** conventional ANPC HBST, and **(c)** proposed ANPC HBST.

A. Case 1: v_x changes from V_{in} to 0

Fig. 4 presents the simulated transient waveforms of all control voltages in Ⓘ, all drain-source voltages in Ⓘ to Ⓘ, the gate-source voltages of the main transistors in Ⓥ and the instantaneous power values, i.e., the products of drain currents times corresponding drain-source voltages, in Ⓥ.

The results for the conventional HBST are shown in **Fig. 4 (a)**. At the instant t_a the switch TP_2 is commanded to turn off and, after the delay time $t_1 - t_0$, the load current

[1] All the simulation results shown in this work consider equal transistors' gate widths for the main switches $T_{w,TP_{1,2}} = T_{w,TN_{1,2}} = T_w$ ($\propto$ transistor area) and the clamping switches $T_{w,TP_3} = T_{w,TN_3} = T_w/10$. The gate drivers of the main switches are two-stage tapered inverters, which use transistors with gate widths of $T_{w,GDm_1} = T_w/10$ for the first stage and $T_{w,GDm_2} = T_w/50$ for the second stage. The gate drivers of the clamping switches use transistors with same gate widths for first and second stages, $T_{w,GDc_{1,2}} = T_w/50$. Low voltage transistors of a 14 nm CMOS technology node realize main and clamping switches.

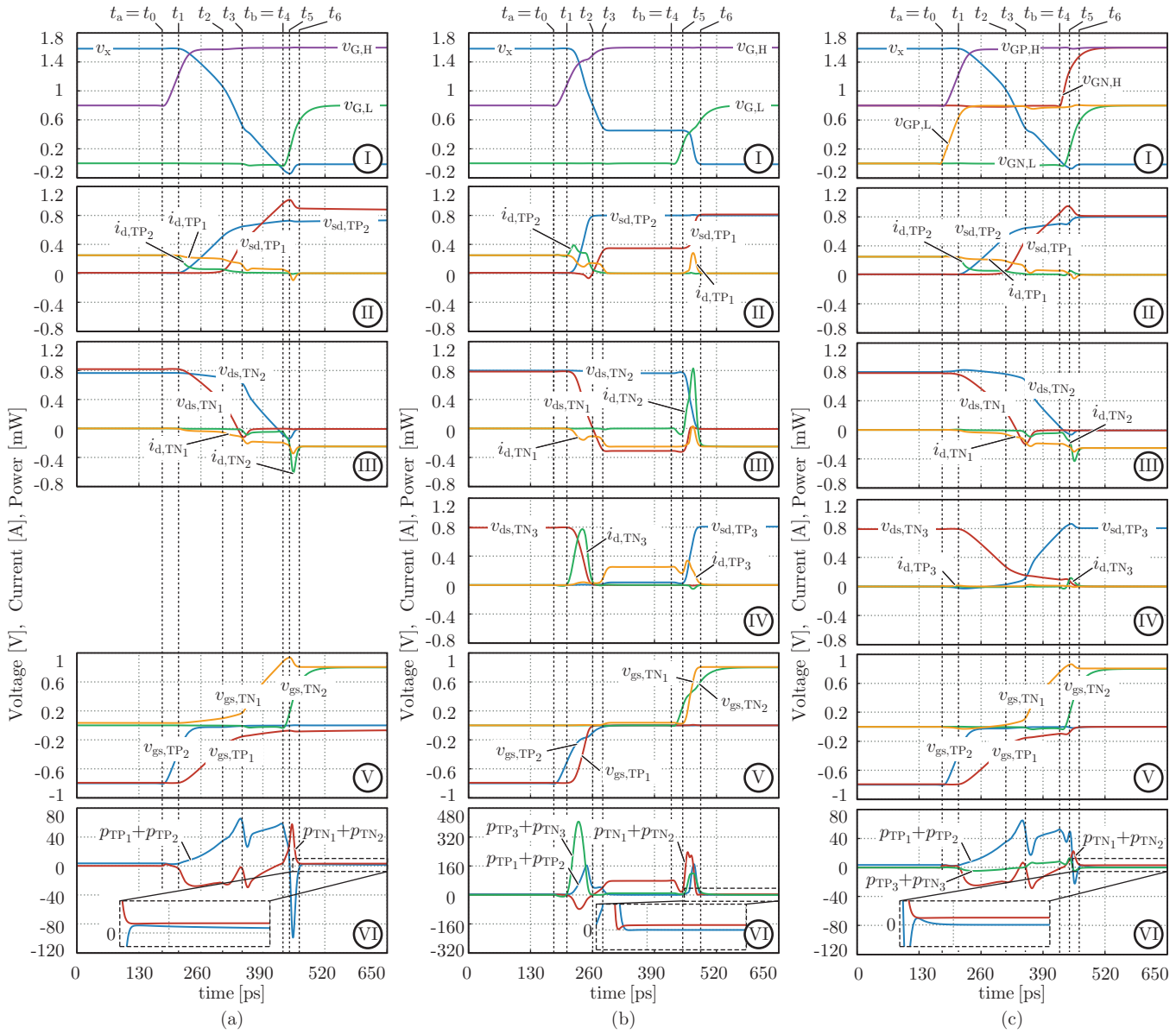

Fig. 4: Main waveforms, obtained from Cadence simulations[1], of the three power stages of Fig. 1 during a transient change of v_x from V_{in} to 0 with positive current, I_{sw}. **(a)** Conventional HBST **(b)** Conventional ANPC HBST **(c)** Proposed ANPC HBST. The waveforms were generated considering $V_{in} = 1.6\,\text{V}$ and $I_{sw} = 250\,\text{mA}$.

charges the effective output capacitances of TP_2 and TP_1 and discharges those of TN_1 and TN_2 and thus, low switching losses (ZVS) are achieved. A detailed examination of all currents during switching reveals that, because of $C_{gd} = C_{gs} \gg C_{ds}$, the drain current of TP_2 is less than the drain current of TP_1 during $t_1 < t < t_5$ and the same applies to TN_2 and TN_1, i.e., $|i_{d,TP_2}| < |i_{d,TP_1}|$ and $|i_{d,TN_2}| < |i_{d,TN_1}|$. Due to $|i_{d,TN_2}| < |i_{d,TN_1}|$, first almost only v_{ds,TN_1} decreases during $t_1 < t < t_3$ and thereafter v_{ds,TN_2} decreases to zero. However, even though $|i_{d,TP_2}| < |i_{d,TP_1}|$ applies, only v_{sd,TP_2} increases during $t_1 < t < t_2$, since TP_2 is turned off at $t = t_1$ and the gate current of TP_1, $i_{d,TP_1} - i_{d,TP_2}$, first needs to discharge the effective input capacitance of TP_1 in order to turn off TP_1 at $t = t_2$. The dead-time is adjusted such that after the dead-time, at $t = t_b$, v_{ds,TN_2} is close to zero and the switch TN_2 is turned on with low losses. The conventional HBST does not assure voltage balancing of the stacked transistors and $v_{sd,TP_1} \neq v_{sd,TP_2}$ occurs for $t > t_6$ in Fig. 4 (a) Ⅱ, which causes additional leakage losses.

In case of the conventional ANPC HBST the waveforms shown in **Fig. 4 (b)** result. At $t = t_a$ the high-side gate driver simultaneously turns off TP_2 and turns on TN_3, which forces v_{ds,TN_3} to decrease to zero during $t_1 < t < t_2$ and causes turn-on losses in TN_3. Accordingly, v_{sd,TP_2} is forced to increase to $V_{in} - V_{mid}$ and, due to $v_{gs,TP_1} = -v_{ds,TN_3}$, TP_1 is turned off. The drain source voltage of TN_2 remains at 0.8 V during this time interval since TP_3 is still in its on-state. Hence, v_{ds,TN_1} decreases and reaches zero at $t = t_2$. However, the load current continues to provide charge to the effective output capacitances of TN_1 and TP_1 during $t_2 < t < t_3$ and the voltages v_x and v_{ds,TN_1} continue to decrease. With decreasing v_x, $v_x < V_{mid}$, the gate of TN_1 being tied to V_{mid}, and TP_3 being switched on, the gate-drain voltage of TN_1 increases until the transistor is operated in its saturation region, controlled via the gate-

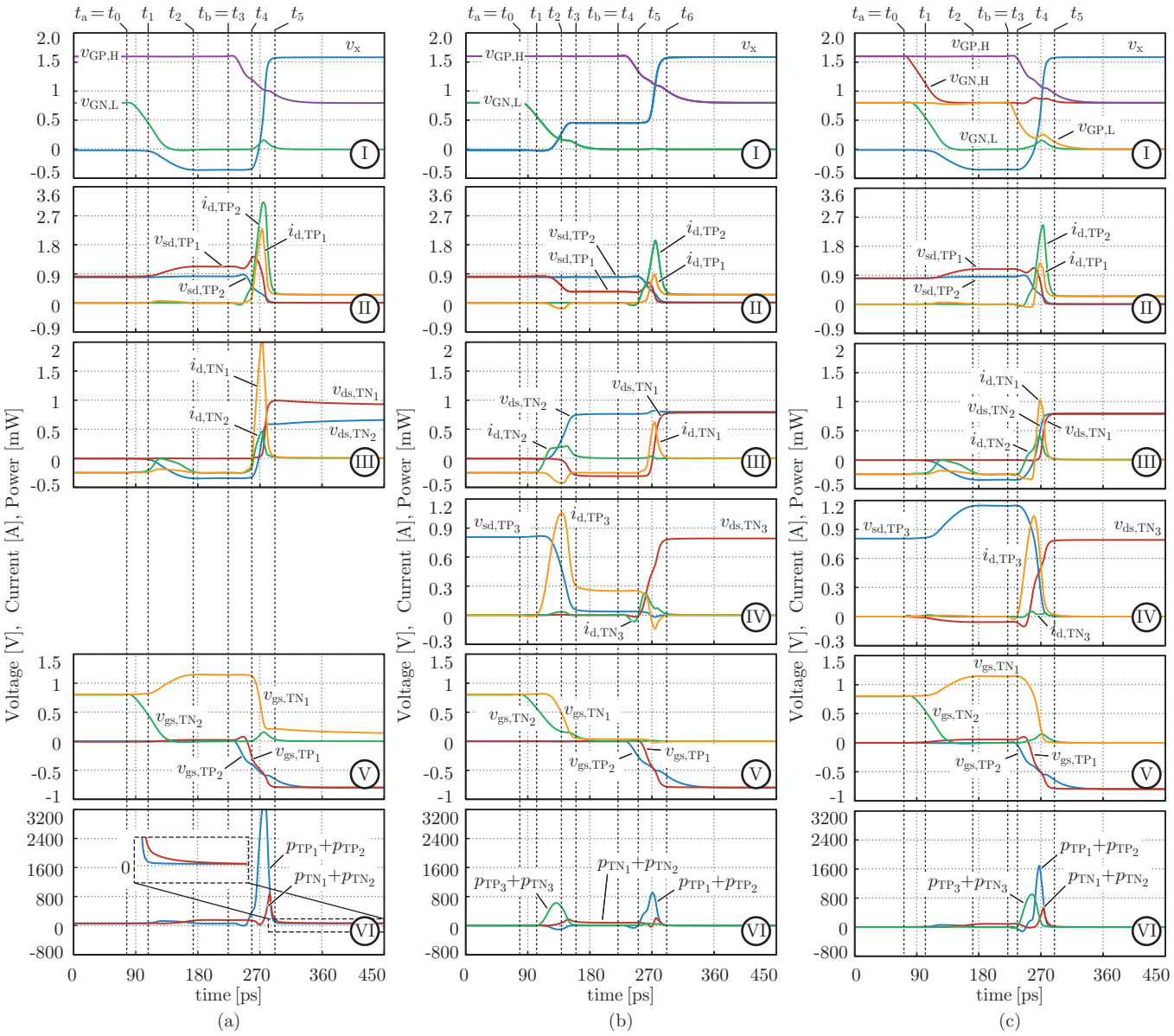

Fig. 5: Main waveforms, obtained from Cadence simulations[1], of the three power stages of Fig. 1 during a transient change of V_x from 0 to V_{in} with positive current, I_{sw}. **(a)** Conventional HBST **(b)** Conventional ANPC HBST **(c)** Proposed ANPC HBST. The waveforms were generated considering $V_{in} = 1.6\,V$, $I_{sw} = 250\,mA$.

drain voltage instead of the gate-source voltage, during the corresponding time interval, $t_3 < t < t_5$, which causes substantial losses.[2] Finally, at $t = t_b$, TN_2 and TP_3 are commanded to turn on and off respectively, and considerable turn-on losses in TN_2 are observed. The clamping switches TN_3 and TP_3, thus, enforce balanced blocking voltages of the transistors. For this, however, soft-switching is sacrificed and increased switching losses result.

With regard to the proposed ANPC HBST both clamping switches, TN_3 and TP_3, are turned off during the dead-time interval, $t_a < t < t_b$, cf. **Fig. 4 (c)**. For this reason, similar current and voltage waveforms result for the proposed ANPC HBST and the conventional HBST. At $t = t_b$ the clamping switch TP_3 is turned on to balance the blocking voltages of TP_1 and TP_2. This concept simultaneously achieves both, low switching losses (ZVS) and balanced voltages at the transistor terminals in steady-state.

[2]N.B.: the body diodes of TN_1 do not conduct during $t_3 < t < t_4$, due to the present wiring of the body diodes, cf. Fig. 3, and $v_x > 0$.

B. Case 2: v_x changes from 0 to V_{in}

Fig. 5 presents the simulated waveforms during a switching transient for case 2 and for the different investigated converter topologies. In case 2, TN_2 is switched off at $t = t_a$ and TP_2 is switched on at $t = t_b$.

Fig. 5 (a) shows the waveforms simulated for the conventional HBST. The switch TN_2 turns off at t_1 when the gate-source voltage of TN_2 falls below the threshold voltage. Since TN_1 remains in the on-state, the load current provides charge to the drain-source and gate-drain capacitances of TN_2 during $t_1 < t < t_2$. Hence, v_{ds,TN_2} decreases and the gate-drain voltage of TN_2 increases until TN_2 enters the saturation region at $t = t_2$. Subsequently, during $t_2 < t < t_4$, negative drain-source voltage and negative drain current are present in TN_2.

At $t = t_4$ the negative gate-source voltages of both PMOS transistors, TP_1 and TP_2, exceed the transistor's (negative) threshold voltages, which causes TP_1 and TP_2 to turn on and forces v_x to increase to V_{in} during $t_4 < t < t_5$. Very high instantaneous drain currents are present in TP_1, TP_2, and TN_1 and comparably high turn-on losses result. Furthermore, unbalanced transistor voltages are observed for $t > t_5$.

The waveforms for the conventional ANPC HBST are depicted in **Fig. 5 (b)**. At $t = t_a$, TN_2 and TP_3 are commanded to turn off and on, respectively, which, during $t_1 < t < t_3$, causes v_{ds,TP_3} to decrease to a value close to zero and v_{ds,TN_2} to increase to V_{mid}. Furthermore, the load current provides charge to the effective output capacitances of TP_1 and TN_1, so v_{sd,TP_1} and v_{ds,TN_1} decrease during $t_2 < t < t_3$. Thus, positive gate-drain voltage is applied to TN_1, since TP_3 is switched on for $t > t_3$, and TN_1 is operated in the saturation region during $t_3 < t < t_5$ with the drain current being equal to the load current. During the subsequent time interval, $t_5 < t < t_6$, the transistors TP_1 and TP_2 are turned on, which forces their drain-source voltages to decrease to zero. At the same time TN_3 is turned off and v_{ds,TN_3} increases to V_{mid}. In comparison to the conventional HBST lower instantaneous losses are simulated, cf. Fig. 5 (b) ⑥.

The transient waveforms during switching and case 2 for the proposed ANPC HBST are given in **Fig. 5 (c)**. During the dead-time interval, both clamping switches, TN_3 and TP_3, are turned off and, for this reason, similar waveforms compared to Fig. 5 (a) result. During $t_4 < t < t_5$, however, TP_3 ensures that the drain-source voltage of TN_1 does not exceed V_{mid}. The charging of the parasitic capacitances of TN_1 and TN_2 is, thus, partly achieved by means of TP_3 which leads to lower instantaneous losses than for the conventional HBST.

C. Discussion

According to the details presented in the previous Sections III-A and III-B, both, the conventional and the proposed ANPC HBST converters, feature balanced blocking voltages of the main transistors. The conventional ANPC HBST converter is found to generate higher losses in presence of case 1, cf. Sec. III-A, since it fails to provide soft-switching. In addition, this converter is found to generate additional losses in the clamping transistor TP_3 and is, thus, expected to provide lower switching losses when operated with a very small dead-time. Both examined ANPC HBST converters generate similar and comparably high switching losses during turn-on in case 2, which leads to similar total switching losses for both converters. In comparison to both ANPC HBST converters even higher turn-on losses result for the conventional HBST converter. Furthermore, in presence of case 2, short durations of the dead-time intervals need to be considered for the conventional HBST and the proposed ANPC HBST to avoid over-voltages across TP_1 and TP_3.

IV. Simulation Results and Performance Comparison

This work estimates the transistors' conduction, leakage, gate-charge, and switching losses using energy based models similarly to the approach described in [6]. The total losses estimation using the proposed methodology varies in less than 9% (in the majority of the cases is less than 5%) from the total losses calculated in Cadence for all the simulated operating points, which, in general, is accurate enough for the purpose of design and optimization of power management systems. The Cadence simulated efficiencies may differ from final measurement results, by reason of neglected parasitics of the wiring metals and chip interconnects, which affects the actually present switching losses. However, due to the mainly capacitive nature of the switching losses for this application, the error between the simulations and the measurements is expected to be small.

Conduction losses of any power transistor TP_k and TN_k of the system are calculated with

$$P_{\text{cond,TP}_k} = \frac{1}{T_{\text{sw}}} \int_{t_{\text{begin,cond}}}^{t_{\text{end,cond}}} v_{\text{sd,TP}_k}\ i_{\text{d,TP}_k} \mathrm{d}t,\ k = \{1,2,3\}, \quad (1)$$

and

$$P_{\text{cond,TN}_k} = \frac{1}{T_{\text{sw}}} \int_{t_{\text{begin,cond}}}^{t_{\text{end,cond}}} v_{\text{ds,TN}_k}\ i_{\text{d,TN}_k} \mathrm{d}t,\ k = \{1,2,3\}, \quad (2)$$

respectively, where T_{sw} is the switching period, $t_{\text{begin,cond}}$ is the instant when the transistor is fully on and $t_{\text{end,cond}}$ is the instant when the transistor is commanded to turn off. The leakage losses, $P_{\text{leak,TN}_k}$ and $P_{\text{leak,TP}_k}$, are similarly calculated, but the integration interval corresponds to the period starting from the time instant in which the transistor is fully off to the time instant in which it is commanded to turn on.

The switching energies dissipated by the transistors of the half-bridges are calculated with

$$E_{\text{sw,TP}_k} = \int_{t_{\text{sw,begin}}}^{t_{\text{sw,end}}} v_{\text{sd,TP}_k}\ i_{\text{d,TP}_k} \mathrm{d}t,\ k = \{1,2,3\}, \quad (3)$$

for PMOS and

$$E_{\text{sw,TN}_k} = \int_{t_{\text{sw,begin}}}^{t_{\text{sw,end}}} v_{\text{ds,TN}_k}\ i_{\text{d,TN}_k} \mathrm{d}t,\ k = \{1,2,3\}, \quad (4)$$

for NMOS. The instant $t_{\text{sw,begin}}$ is the time the transistor is commanded to switch on or off and $t_{\text{sw,end}}$ denotes the end of the switching process, i.e., there are no charge changes among the components present and v_x is nearly constant.

The gate-charges of the power transistors TP_k and TN_k of the system are calculated with

$$Q_{\text{g,TP}_k} = \int_{t_{\text{sw,begin}}}^{t_{\text{sw,end}}} i_{\text{g,TP}_k} \mathrm{d}t,\ k = \{1,2,3\}, \quad (5)$$

for PMOS and

$$Q_{\text{g,TN}_k} = \int_{t_{\text{sw,begin}}}^{t_{\text{sw,end}}} i_{\text{g,TN}_k} \mathrm{d}t,\ k = \{1,2,3\}, \quad (6)$$

for NMOS respectively.

The total losses of the HBs are estimated by summing up the total conduction, leakage, gate-charge, and switching losses of all transistors

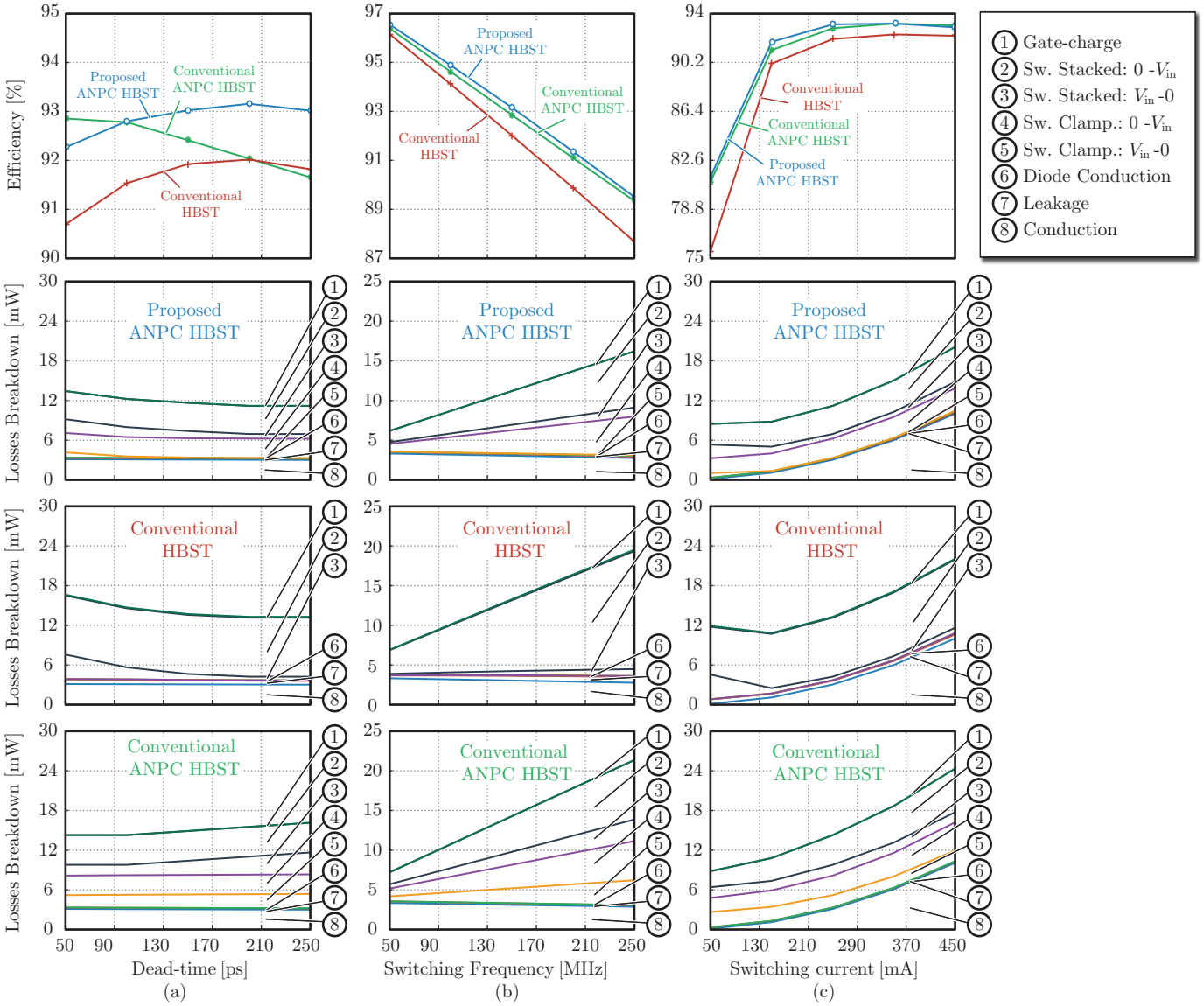

Fig. 6: Losses and efficiencies determined with Cadence simulations[1] for the topologies depicted in Fig. 1 at $V_{\text{in}} = 1.6\,\text{V}$ and duty-cycle $D = 0.5$; the dead-time interval of case 2 is kept constant, $dt_{\text{ab,case2}} = 40\,\text{ps}$. **(a)** HBs' efficiencies for varying dead-time interval of the turn-off transient of case 1, dt_{ab}, (cf. Fig. 4) at $f_{\text{sw}} = 150\,\text{MHz}$ and $I_{\text{sw}} = 250\,\text{mA}$. **(b)** HBs' efficiencies for varying switching frequency at operation with optimal dead-time and $I_{\text{sw}} = 250\,\text{mA}$. **(c)** Comparison of the HBs' efficiencies for varying switching frequency at operation with optimal dead-time and $f_{\text{sw}} = 150\,\text{MHz}$.

$$P_{\text{tot}} = \sum_{k=1}^{3}(P_{\text{cond,TN}_k} + P_{\text{cond,TP}_k} + P_{\text{leak,TN}_k} + P_{\text{leak,TP}_k} + (E_{\text{sw}_{\text{case1}},\text{TP}_k} + E_{\text{sw}_{\text{case2}},\text{TP}_k} + E_{\text{sw}_{\text{case1}},\text{TN}_k} + E_{\text{sw}_{\text{case2}},\text{TN}_k} + (Q_{\text{g}_{\text{case1}},\text{TP}_k} + Q_{\text{g}_{\text{case2}},\text{TP}_k} + Q_{\text{g}_{\text{case1}},\text{TN}_k} + Q_{\text{g}_{\text{case2}},\text{TN}_k})V_{\text{in}}/2)f_{\text{sw}}, \tag{7}$$

Fig. 6 presents a comparison of the achievable efficiencies and losses breakdown of the studied HBSTs when the dead-time interval of case 1, switching frequency, and load current are varied. In **Fig. 6 (a)** the dead-time interval for the turn-off transient of case 1, t_{ab}, is varied from 50 ps to 250 ps while the switching frequency and the load current are maintained constant at 150 MHz and 250 mA, respectively. The efficiency curves of the proposed ANPC HBST and the conventional HBST are very similar in shape and have their peaks at the same dead-time value of 200 ps. The difference in offset of the efficiency results is due to the increased switching losses in the PMOS transistors for the switching transient of case 2 for the conventional HBST, as explained in Sec. III-B and quantified in Fig. 6 ②. If the dead-time is decreased to values below the optimal value, i.e., the value of $dt_{\text{ab,case1}}$ that yields best efficiency, incomplete discharging and charging of the transistors' effective output capacitances results, which leads to increased switching losses due to turn-on losses. The decrease of the switching losses during the case 1 interval for small dead-times $dt_{\text{ab,case1}} < 210\,\text{ps}$, can be seen in the losses breakdown of the proposed ANPC HBST and the conventional HBST, cf. Fig. 6 (a) ③. Dead-times larger than the optimal value only generates more conduction losses due to the conduction of the load current through TN_1 which operates in the saturation region when v_{x} reaches values close to zero. It is also observed from Fig. 6 (a) that the efficiency of the conventional ANPC HBSC only drops with the increase of the dead-time interval above a very small value of 50 ps.

This behavior is caused by the additional conduction losses that are generated during the dead-time interval when TN_1 conducts in the saturation mode, cf. Fig. 6 (a) ③. When the optimum dead-time is implemented (at switching frequency $f_{sw} = 150\,\mathrm{MHz}$, input voltage $V_{in} = 1.6\,\mathrm{V}$, duty-cycle $D = 0.5$, and given dead-time during the switching transient of case 2, $dt_{ab,case2} = 40\,\mathrm{ps}$), the proposed power stage achieves improvements in efficiency of approximately 1% compared to the conventional HBST.

To obtain a fair performance comparison, the optimal dead-times are selected in order to maximize the efficiency for the cases where switching frequency and load current are varied, cf. Fig. 6 (b) and (c). From **Fig. 6 (b)** it can be seen that the difference in efficiency between the conventional and proposed ANPC HBST to the conventional HBST increases with increase of the switching frequency. This trend is explained due to the increased value of switching losses during the switching transient of case 2, cf. Fig. 6 (b) ②, for the conventional HBST. At a switching frequency of $250\,\mathrm{MHz}$, the proposed and ANPC HBSTs can achieve efficiency gains of approximately 2% compared to the conventional HBST.

From **Fig. 6 (c)**, it can be verified that the the load change mainly affects the total conduction losses of the HBs when the optimal dead-time is employed.

Some general features and trends are observed for the HBs from the losses breakdown independently of the implemented dead-times, switching frequencies, and load currents:

- According to Fig. 6 ⑦, the conventional HBST is subject to increased leakage losses due to the unbalancing of the voltages after the transients.
- Switching losses of clamping transistors are higher for the conventional ANPC HBST topology due to the discharge of the gate capacitances of the PMOS main transistors during the dead-time interval of case 1, cf. Fig. 6 ⑤.
- Very small values of gate-charge losses are expected for all analyzed HBs, cf. Fig. 6 ①, due to the gate charge recycle mechanisms of HBSTs [2], which allow the considered circuits to achieve higher efficiencies than the conventional HBs at very high switching frequencies.
- With respect to dead-time, the proposed ANPC HBST features a flatter efficiency curve and achieves the maximum efficiency for a considerably higher dead-time. This is an advantage since very small and accurate dead-times requires more careful design of the dead-time controller and can be limited by the technology node.

V. Conclusion

This paper presents a comparative evaluation of three different topologies for buck converters using stacked transistors for IVRs. The evaluation is based on in-depth examinations of the internal processes in the power transistors of the considered converters, in particular with regard to the switching transients, using Cadence simulations.

The first considered topology, the conventional HBST, features lowest implementation effort, however, considerably unbalanced blocking voltages appear for the main switches after the switching transients, which lead to overvoltages and reduce the reliability, lifetime and efficiency of the converter ($\eta = 92\%$ at $f_{sw} = 150\,\mathrm{MHz}$, $I_{sw} = 250\,\mathrm{mA}$, and $dt_{ab,case2} = 40\,\mathrm{ps}$). The second topology, the conventional ANPC HBST, requires two additional clamping switches and, with this, achieves balanced blocking voltages. Compared to the first topology an increased efficiency of 92.9% ($f_{sw} = 150\,\mathrm{MHz}$, $I_{sw} = 250\,\mathrm{mA}$, $D = 0.5$, $dt_{ab,case2} = 40\,\mathrm{ps}$) is obtained, at a very short dead-time of $50\,\mathrm{ps}$. Due to its internal structure, however, the conventional ANPC HBST cannot turn off the power stage. Also the third topology, the proposed ANPC HBST, balances the blocking voltages and, in addition, is capable to turn off its power stage. The proposed ANPC HBST maintains soft switching, for this reason maximum efficiency of 93.1% results at a dead-time that is greater than for the conventional ANPC HBST ($dt_{ab,opt} = 200\,\mathrm{ps}$ at $f_{sw} = 150\,\mathrm{MHz}$, $I_{sw} = 250\,\mathrm{mA}$). In order to take advantage of these benefits, two clamping switches, one more level-shifter and two more gate drivers are required, which increase the total area size of the active part by approximately 20% compared to the conventional HBST.

In summary, both, the conventional and the proposed ANPC HBST, feature balanced blocking voltages of the main transistors and are expected to be capable of providing similar efficiencies. Of these two, however, only the proposed ANPC HBST is suitable for multiphase converters since it can turn off its power stage. Currently, a versatile on-chip hardware implementation, which allows for the emulation of all three converter topologies, is realized in order to enable experimental verification in a next step.

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