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# Comparative Evaluation of Overload Capability and Rated Power Efficiency of $200\,\mathrm{V}$ Si/GaN 7-Level FC 3-$\Phi$ Variable Speed Drive Inverter Systems

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***Abstract*—Variable speed drive systems in e.g. robotics applications are challenged with discontinuous operation cycles and short-time overload current requirements of 2-3 times nominal load. As the motor itself constitutes a large thermal time constant compared to the semiconductor devices in the inverter, latter create a bottleneck for the increased losses during overload operation. Hence, special focus has to be laid on the inverter overload capability, preferably without overdimensioning the system. In this paper a transient thermal model of optimized cooling approaches for $200\,\mathrm{V}$ GaN and Si packages is empirically deduced. The model is then used to design a 7-Level Flying Capacitor inverter (7L FCi) aiming for $99\,\%$ efficiency at nominal load for facilitated motor integration and 3 times overload capability. Consequently, the number of parallel switches, switching frequencies and the volume of passive components such as the flying capacitors and the output filter inductor is considered. In order to omit oversizing the inverter and the output inductor for overload operation, an unorthodox way of increasing the switching frequency during overload is proposed. It is concluded, that the small chip size of the $200\,\mathrm{V}$ GaN devices compared the $200\,\mathrm{V}$ Si devices poses additional challenges when dealing with overload operation.**

## I. Introduction

In many applications, Variable Speed Drive (VSD) system are operated under application-specific mission profiles, where e.g. during an acceleration phase or even at standstill large transient overload torques can be demanded, which e.g. in automated robot systems exceed their continuous/nominal operation limits by a factor of 2-3 [1]–[3]. As a consequence, the generation of these short-time overload torques leads to a high transient current stress in the inverter and therefore to temporarily high conduction and switching losses in the semiconductor devices. Since the thermal time constant of the semiconductor devices is much smaller than the one of the electric motor, the inverter constitutes as bottleneck and mainly defines the overload capability of the overall VSD system. Especially in inverter systems employing wide-bandgap (WBG) semiconductor devices, which have a much smaller chip area than their Si-counterparts, the appropriate cooling and overload handling can become even more challenging. Hence, in order to properly design the inverter, which means that on the one hand during overload intervals the maximum allowed junction temperature of the semiconductors should not be exceeded, but on the other hand an overdimensioning of the semiconductor chip size should be avoided, a detailed transient thermal model with thermal resistances and capacitances of the inverter power stage is essentially needed [4]–[6].

To model the cooling properties through a stack of different materials, as e.g. found for power modules, through hole components or Surface-Mounted Devices (SMD) featuring a large exposed cooling pad, in the literature [7]–[10], the thermal resistances and capacitances of each material are mostly determined by assuming a simplified unidirectional heat flow where a certain lateral heat spreading is considered. For low-voltage GaN device, which e.g. are available as a passivated die form with solder bumps [11], however, the cooling capabilities are clearly overestimated with these simplified models, since e.g. due to the narrow ball grid array package with alternating source and drain contacts only few thermal vias can be placed below the chip, which strongly limits its cooling capability. For SMD components with exposed cooling pad [12], this also can become true if e.g. due to electrical constraints, i.e. a needed low inductive and coplanar commutation loop, only a small number of thermal vias/copper inlays can be placed below the exposed pad. In this case, the thermal vias even have to be placed next to the exposed pad, which means that the lateral thermal resistance can strongly increase or even dominate the total thermal resistance. Furthermore, also interface resistances between different materials are difficult to estimate because e.g. the heat conduction of thermal interface materials (TIM) also depends on the applied pressure [13], but must be considered, since for high overload capabilities for SMD components a maximum total thermal resistance of around $0.5 - 2\mathrm{K/W}$ per semiconductor device should be ensured.

As another important point, mostly the thermal capacitances are either neglected or are considered as lumped components which are calculated based on the layer dimensions and the according material properties [14], [15]. However, for an inhomogeneous heat flow, especially in areas surrounding the SMD components, an accurate thermal modeling is crucial to properly design the converter concerning its short-time overload capability with durations of around a few seconds. Therefore, in the project planning of VSD systems often a conservative system design is followed in order to avoid unacceptable thermal overloading. For motor integrated in-

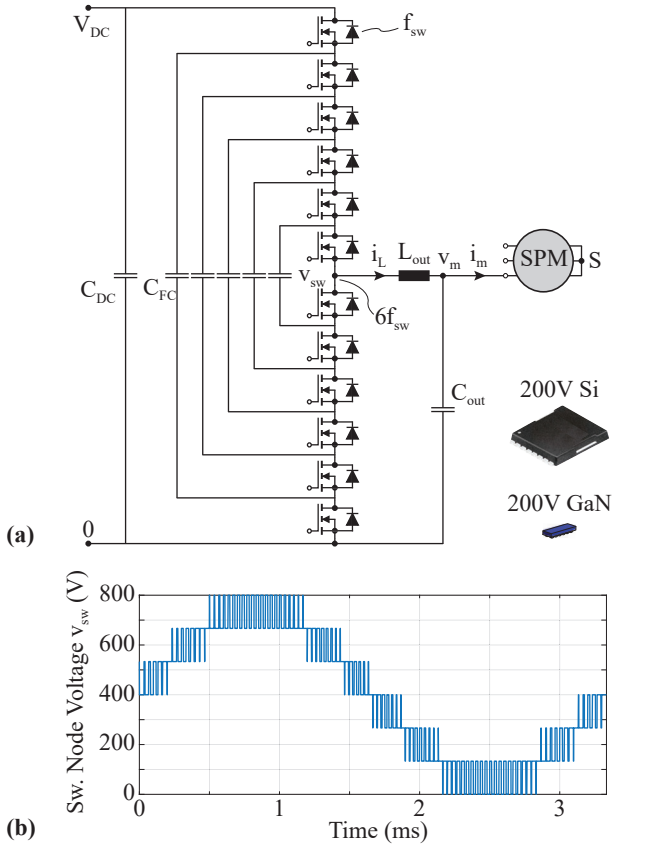


**Fig. 1: (a)** Single bridge-leg of a 7-Level flying capacitor inverter driving a three-phase SPM servo motor. The considered 200 V power devices are a 11.1 mΩ Si MOSFET with $A_{\text{chip,Si}} = 29\,\text{mm}^2$ [12] and a 10 mΩ GaN EPC2034$C$ switch with $A_{\text{chip,GaN}} = 12\,\text{mm}^2$ [11]. **(b)** Multilevel voltage waveform at the switching node with respect to the negative DC link rail.

verter systems, however, the limited space condition does not allow an overdimensioning of the inverter, which means that in a first step an accurate *transient* thermal model of the applied semiconductor cooling concept is needed to afterwards optimally design the inverter for different load conditions and mission profiles.

In the kW-range, VSD systems employing two-level inverter topologies are typically built with 1200 V IGBTs, which are continuously superseded by 1200 V SiC-MOSFETs [16]–[18], since these have developed to a robust and matured technology. However, one key challenge are the high voltage transients ($dv/dt$) of these 1200 V SiC-MOSFETs, which in motor applications can lead to overvoltages due to reflections on long motor cables, partial discharge in motor windings, high-frequency bearing currents and elevated EMI noise emissions [19]–[21]. For these reasons, and also due to better integration into the motor, multi-level inverter topologies are analyzed in the literature [22], [23], which can mitigate the mentioned problems. For the given specifications in **Table I**, one option constitutes a 7-Level Flying Capacitor inverter (7L FCi) employing either 200 V Si-MOSFETs oder 200 V GaN-HEMT devices. As already stated in the literature [24], [25],

**TABLE I:** 7L FCi Specifications.

| | |
|---|---|
| DC Link Voltage $V_{\text{DC}}$ | 800 V |
| Nominal Output Power $P_{\text{nom}}$ | $3 \cdot 2.5$ kW |
| Nominal Target Efficiency $\eta_{\text{nom}}$ | $> 99\,\%$ |
| Nominal Phase Current $\hat{i}_{\text{m,nom}}$ | 15 A |
| Overload Phase Current $\hat{i}_{\text{m,ol}}$ | (i.e. 3 x Nom. Torque) 45 A |
| Overload Duration $t_{\text{ol}}$ | 3 s |
| Ambient Temperature $T_{\text{amb}}$ | 90 °C |

with this converter topology a high nominal load efficiency in a compact converter design can be achieved, especially when GaN devices are used. However, in the literature no comprehensive analysis of Si versus GaN devices concerning overload capability is performed, which for motor applications is essentially needed. Furthermore, no design procedure for VSD inverters is given which allows to achieve a certain minimum efficiency at nominal load, while during short-time overload a maximum junction temperature is not exceeded.

Therefore, in this paper, a comprehensive comparison of 200 V Si and GaN devices concerning their overload capability is performed. In **Section II**, different cooling strategies of 200 V Si-MOSFET and 200 V GaN-HEMT devices employed in a 7L FCi are analyzed (cf. **Fig. 1**), which due to the different chip sizes and packaging technologies lead to different empirically determined transient thermal models. Afterwards, based on the obtained transient thermal models in combination with already determined switching losses of 200 V GaN-HEMT and 200 V Si-MOSFET devices [23], in **Section III** a 7.5 kW 7L FCi achieving a $> 99\,\%$ efficiency at nominal load to facilitate the integration of the inverter into a naturally cooled motor, and providing an overload capability of 3 times the nominal load is designed for the specifications given in **Table I**. After selecting the proper number of parallel semiconductor devices per switch and defining the maximum achievable switching frequency during nominal and overload operation, which also determines the needed volume of passive components like the flying capacitors or the optional LC output filter, in **Section IV** the transient thermal behavior of the 7L FCi is analyzed depending on the selected output frequency, i.e. the speed, where it is shown that the maximum junction temperature drops with increasing output frequency, since the current stress is more evenly distributed to all three inverter phases and the junction temperature cycling due to the pulsating semiconductor losses is more and more smoothed out. The paper concludes with a comprehensive comparison of the achieved performances of 200 V GaN-HEMT and 200 V Si-MOSFET concerning thermal and mechanical design as well as overload capability in the context of a motor-integrated 7.5 kW 7L FCi.

## II. Transient Thermal Models of Power Semiconductor Cooling Concepts

In this section, possible cooling concepts of best-in-class 200 V GaN-HEMT (EPC2034C, 10 mΩ, EPC Co. [11]) and 200 V Si-MOSFET (IPT111N20NFD, Optimos 3 Fast Diode (FD), 11.1 mΩ, Infineon [12]) devices are discussed, which

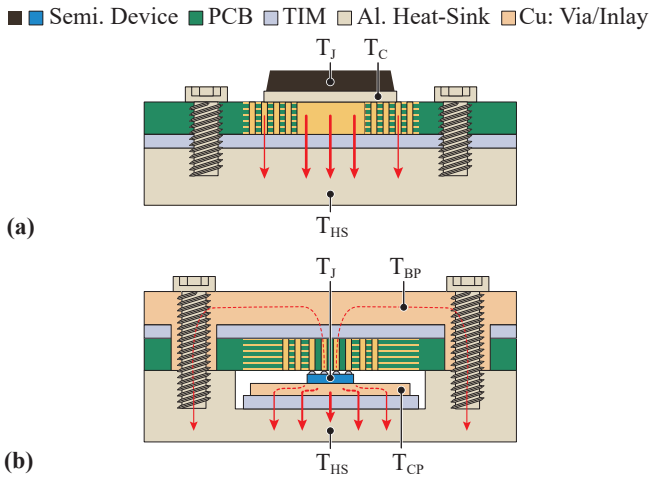


**Fig. 2:** Schematic drawing of proposed cooling concepts of **(a)** a molded SMD package with bottom-side exposed cooling pad used for 200 V Si-MOSFETs, which is cooled through the PCB with either a large number of thermal vias or a copper inlay inside the PCB and **(b)** a passivated die form with solder bumps, which is soldered to the bottom side of the PCB and where a copper piece is directly attached to the GaN device. The PCBs and copper piece are electrically insulated from the bottom-side heatsink/top-side copper plate with a thermal interface material (TIM).

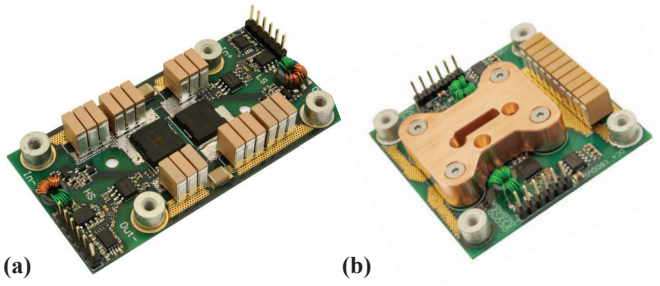


**Fig. 3:** Realized printed circuit boards (PCBs) of one FC cell employing **(a)** 200 V Si-MOSFETs (IPT111N20NFD, Optimos 3 Fast Diode (FD), Infineon [12]) and **(b)** 200 V GaN-HEMT devices (EPC2034C, EPC Co. [11]). The PCBs are used to determine the transient thermal model of the semiconductor devices.

currently feature the lowest $R_{\mathrm{ds,on}}$-ratings among state-of-the-art 200 V Si and GaN power semiconductors.

The Si-MOSFET is provided in a molded SMD package ($10\,\mathrm{mm} \times 12\,\mathrm{mm}$) with a large exposed cooling pad ($6.5\,\mathrm{mm} \times 7.5\,\mathrm{mm}$), and therefore must be cooled through the PCB as schematically shown in **Fig. 2 (a)**. In order to minimize the thermal resistance of the PCB, the two possibilities of placing either as many thermal vias as possible or a large copper inlay inside the PCB below the exposed pad are followed. On the bottom side, the PCB must be electrically insulated with a thermal interface material (TIM) and is screwed to a heatsink, where washers guarantee a defined pressure and insulation distance of $0.3\,\mathrm{mm}$ for the selected TIM (cf. Table II). The realized PCB of one FC cell employing Si-MOSFETs, which is used to determine the transient thermal model of one Si-MOSFET, is shown in **Fig. 3 (a)**.

In contrast, the GaN device is available as a passivated die form (4.6 mm x 2.6 mm) with solder bumps. Due to the alternating arrangement of the source and drain contacts - beneficial for the electrical design to minimize the commutation inductance - and the small creepage distance between the pads, almost no thermal vias can be placed below the chip, which strongly limits the cooling capability of this device through the PCB to the heatsink. Furthermore, since the junction-to-case resistance to the bottom side of the chip is relatively high ($4\,\mathrm{K/W}$), additional cooling over the top side of the chip is absolutely necessary. One option is to directly cover the GaN devices soldered to the PCB top side with the TIM and to press a heatsink from the top side. However, due to the tiny chip size, the contact area of the GaN device to the TIM is small and the resulting thermal resistance through the TIM is relatively high. Hence, in order to enlarge the contact area to the TIM, it is also possible to first attach a copper piece directly to the top side of the GaN die, which acts as heat spreader, and then to electrically insulate it from the heatsink with a TIM. The copper piece actually emulates the base plate or exposed pad of a molded package as e.g. the one of the considered Si-counterpart. As a further advantage, the copper piece also increases the thermal capacitance of the chip, and thus enables a higher overload capability, if a good thermal contact between copper piece and GaN top side can be guaranteed.

A flipped version of this GaN cooling concept is schematically illustrated in **Fig. 2 (b)**, where the GaN device is mounted on the bottom side of the PCB and the chip is directly attached to the copper piece lying underneath, which in turn is electrically insulated from the heatsink with the TIM. This sandwich structure is pressed with a second copper plate screwed from the top side of the PCB. Advantageously, this fixture provides an additional cooling path upwards through the PCB and then through the copper plate and screws back to the bottom-side heatsink, which however is clearly worse than the main cooling path. **Fig. 3 (b)** shows the realized PCB of the GaN half-bridge to determine the corresponding transient thermal model, where first the mentioned copper piece with half the size of the Si-MOSFET ($6\,\mathrm{mm} \times 10\,\mathrm{mm}$ with a thickness of $2.5\,\mathrm{mm}$) is attached to a single GaN switch (not visible), and then a copper heatsink which is insulated with a TIM is screwed from the top side to this sandwich arrangement. In a first attempt, the contact resistance between chip and copper piece was improved with heat paste, however, finally, to really figure out the minimum achievable contact resistance e.g. similar to the case when the GaN chip would be sintered to a thermal pad, a liquid metal with a much higher thermal conductivity (Conductonaut with $73\,\mathrm{W/mK}$ [26]) was used.

To extract the dynamic thermal models of the Si and GaN half-bridges with their thermal resistances and capacitances, a constant power is injected into the continuously turned-on semiconductor devices, while the transient temperature response of the chip ($T_{\mathrm{J}}$), the copper piece ($T_{\mathrm{CP}}$), the copper plate ($T_{\mathrm{PL}}$) and aluminum heatsink ($T_{\mathrm{ALU}}$) are measured (cf. **Fig. 4**). Except from the junction temperature, which is de-

**TABLE II:** Used heat conducting materials.

| | Name | Thermal Conductivity (W/mK) |
|---|---|---|
| TIM | Sarcon XR-m 0.5 mm [13], | 17 |
| HP | S606P-30 [27] | 8 |
| LM | Conductonaut [26] | 73 |
| Solder | SMD291AX10 (Sn63/Pb37) [28] | 50 |

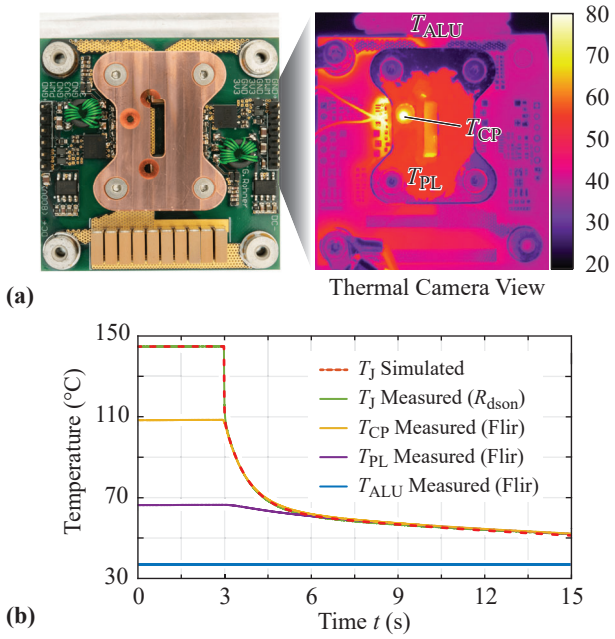


**Fig. 4:** Temperature measurement of the GaN PCB to extract the transient thermal model. The junction temperature is determined from the temperature-dependent $R_{ds,on}$. **(a)** PCB top-view with corresponding thermal image and **(b)** measured temperature profile during a power step. These results are used to determine the thermal network parameters from Fig. 5. The simulated junction temperature ($T_J$ Simulated) nicely matches the measured temperature profile.

termined from the temperature-dependent semiconductor on-state resistance $R_{ds,on}(T)$ [29], all temperatures are captured with a precision high speed infrared camera A655sc from Flir [30] with a frame rate of 40 ms, a temperature resolution of $< 30$ mK where a close-up IR lens with a resolution of 100 µm is attached. The close-up lens is required to accurately measure $T_{CP}$ through a 1.5 mm spy hole in the copper plate.

In a first step, the total thermal resistance of each half-bridge for different cooling concepts is determined by measuring the total temperature difference from junction to heatsink at steady state. For the Si half-bridge actually both cooling concepts with either approximately 200 thermal vias (hole diameter 0.3 mm filled with solder (see **Table II**) or a copper inlay inside the PCB with a diameter of 8.5 mm below the exposed cooling pad are compared. The thermal vias result in an about 20 % higher total thermal resistance compared to $R_{th,tot,inlay} = 0.91\,K/W$ achieved with the copper inlay (junction to aluminum heatsink), and therefore only the inlay is further considered in this paper. A further reason for choosing the inlay is that in analogy to the copper piece used for the GaN half-bridge, the copper inlay increases the thermal capacitance of the Si package and therefore enables a higher overload capability.

For the GaN half-bridge, first only the cooling through the PCB and TIM is measured, which as expected results in a high $R_{th,tot,bottom} = 11\,K/W$, and thus underpins the need of an additional cooling path. As a first approach, the GaN stage (without copper piece) is directly covered with the TIM and screwed to the heatsink leading still to a high total thermal resistance of $R_{th,tot,TIM} = 3\,K/W$. To further improve the heat spreading and to increase the contact surface to the TIM, the copper piece is inserted between chip and TIM. The copper piece is attached to the chip with either heat paste (HP) or liquid metal (LM) (see **Table II**), where the liquid metal leads to minimum total thermal resistance of $R_{th,tot,LM} = 1.81\,K/W$, while the heat paste showed a very poor performance. Even though the liquid metal doesn't constitute an industrial solution, it provides an indication what could be achieved if e.g. the GaN die is directly sintered to a exposed pad, and therefore is further considered in the paper as a benchmark solution for GaN device cooling. In general it can be noted that even though a great effort is made to cool the GaN device, the lowest total thermal resistance is still twice as big as the one achieved with the Si-MOSFET; this emphasizes the need of an improved thermal packaging of low-voltage GaN devices.

In a second step, the transient thermal responses of the two selected Si and GaN cooling concepts are evaluated, where in a post-processing step the thermal transients measured at the junction, case and heatsink are matched to thermal circuit simulations, which result in the two lumped thermal network models shown in **Fig. 5**. The corresponding thermal resistances and capacitances are given in **Table III**. It should be mentioned that based on the three measurement points not all resistances and capacitances can be assigned to a defined material as e.g. the PCB or TIM, since especially in the PCB and areas around the chip the non-uniform lateral heat spreading leads to a strong deviation from simple calculations considering only vertical heat flow. However, with the deduced transient thermal models, the thermal step responses of the Si and GaN junction temperatures can be simulated for a per unit power step as illustrated in **Fig. 6**. This already provides general information about the overload capability of the power semiconductor itself, which is actually completely independent of the finally used converter topology.

As can be noticed, both step responses show a quasi instantaneous temperature increase, i.e. a small time constant of around 0.002 s for Si and 0.01 s for GaN, due to the low thermal capacitance of the chip itself $C_{semi,1}$, which is charged until almost the complete power flows through the first thermal resistance $R_{semi,1}$ (and additionally $R_{LM}$ for GaN). For Si, the initial temperature step is roughly 20 %, while for GaN it is even 50 %. Thus, to reduce this step height, the contact resistances $R_{semi,1}$, $R_{semi,2}$ and $R_{LM}$ (for GaN) should be minimized. Afterwards, both junction temperatures increase quasi exponentially with a much slower equivalent RC time

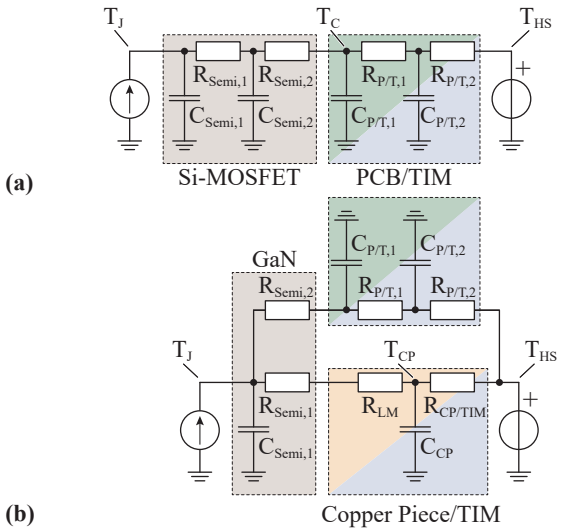


**Fig. 5:** Transient thermal models of **(a)** a 200 V Si-MOSFET embedded in a molded SMD package and **(b)** a 200 V GaN-HEMT die, which are cooled as schematically shown in Fig. 5 (a) and (b), respectively. The corresponding thermal resistances and capacitances listed in Table III are deduced from thermal measurements performed with the setups shown in Fig. 3 (a) and (b), respectively.

**TABLE III:** Experimentally determined thermal parameters per device.

| Resistors | Si (K/W) | GaN (K/W) | Capacitors | Si (J/K) | GaN (J/K) |
|---|---|---|---|---|---|
| $R_{\mathrm{semi},1}$ | 0.17 | 0.30 | $C_{\mathrm{semi},1}$ | 0.008 | 0.008 |
| $R_{\mathrm{semi},2}$ | 0.23 | 4.00 | $C_{\mathrm{semi},2}$ | 0.28 | – |
| $R_{\mathrm{P/T},1}$ | 0.31 | 4.20 | $C_{\mathrm{P/T},1}$ | 0.42 | 0.01 |
| $R_{\mathrm{P/T},2}$ | 0.20 | 2.80 | $C_{\mathrm{P/T},2}$ | 3.00 | 0.20 |
| $R_{\mathrm{LM}}$ | – | 0.73 | $C_{\mathrm{CP}}$ | – | 0.60 |
| $R_{\mathrm{CP/TIM}}$ | – | 1.14 | | | |
| $R_{\mathrm{th,total}}$ | 0.91 | 1.81 | | | |

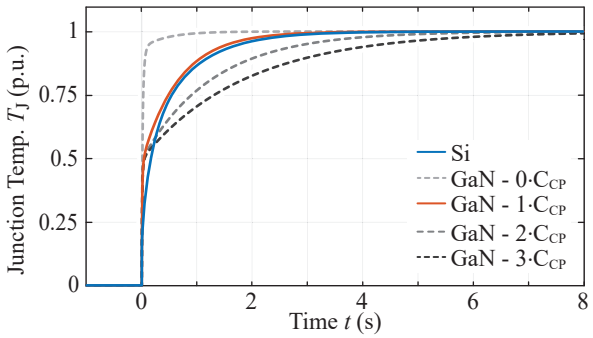


**Fig. 6:** Simulated thermal step responses of the Si and GaN junction temperatures for a per unit power step based on the deduced thermal model given in Fig. 5. In addition, the influence of the copper piece on the resulting thermal time constant is highlighted, where either no copper piece ($0 \cdot C_{\mathrm{CP}}$) or a copper piece with up to 3 times the original thickness, i.e. thermal capacitance ($3 \cdot C_{\mathrm{CP}}$), is considered.

constant $\tau_{\mathrm{semi}}$ of approximately $\tau_{\mathrm{Si}} = 0.4\,\mathrm{s}$ and $\tau_{\mathrm{GaN}} = 0.65\,\mathrm{s}$.

In addition, since for the GaN cooling concept, the top cooling path with the thermal capacitance $C_{\mathrm{CP}}$ actually coincides with the physical properties of the copper piece, its influence on the step response can also be analyzed. As can be noticed, with increasing copper piece thickness, i.e. increasing $C_{\mathrm{CP}}$, the thermal transient is slowed down, thus the copper piece thickness can be adapted depending on the overload demands of the underlying application. The same behavior could be achieved with a thicker/bigger copper inlay for the Si-MOSFET or even for top-side cooled devices employing an exposed pad, where an additional copper piece first adds thermal capacitance before it is insulated with the TIM from the heatsink. However, based on the obtained time constants $\tau_{\mathrm{Si}}$ and $\tau_{\mathrm{GaN}}$ of the realized Si and GaN bridge-legs, it already can be concluded that if the overload duration of one semiconductor device is more than around $4 \cdot \tau_{\mathrm{semi}}$, the device can be considered as if it would be operated continuously in overload. However, as shown in Section IV, the maximum overload duration of one semiconductor device only coincides with the maximum system overload duration if the motor is operated at standstill. As soon as the motor is rotating, the effective overload duration of a single semiconductor device is strongly reduced, which means that even if the system overload duration is much longer than $4 \cdot \tau_{\mathrm{semi}}$, the junction temperature of each chip can be kept below the steady state junction temperature obtained at standstill.

For the sake of completeness, it should be mentioned that top-side cooling is preferable to bottom-side cooling, since in this case the thermal and electrical circuits are also physically separated (as e.g. also utilized in IGBT or SiC modules, for 650V GaN devices or even through hole components) and therefore can be designed independently, while with bottom-side cooling e.g. the thermal vias or copper inlay inhibit a coplanar and low inductive PCB layout resulting in a higher commutation loop inductance and in turn in a worse switching behavior with larger voltage overshoot and ringing. This again only can be mitigated with e.g. a high gate resistance to slow down the switching transient or by adding snubbers to the switches. Finally, this means higher switching losses and increased cooling effort, and overall lower system performance.

## III. 200 V Si/GaN based 7-Level FC Inverter Design

Based on the obtained transient thermal models together with the switching losses of 200 V Si-MOSFET and 200 V GaN-HEMT devices determined in [23], a 7.5 kW 7L FCi with the specifications given in **Table I** can be properly designed. As already mentioned, in order to facilitate integration into a naturally cooled motor, the inverter should achieve an efficiency of $> 99\,\%$ at nominal load. Furthermore, an overload capability of three times the nominal load for three seconds is defined. In the following design procedure both the nominal load and the overload operation are considered such that an overdimensioning of the inverter, i.e. the semiconductor devices (in Section III-A) and the passive components (in Section III-B), is avoided.

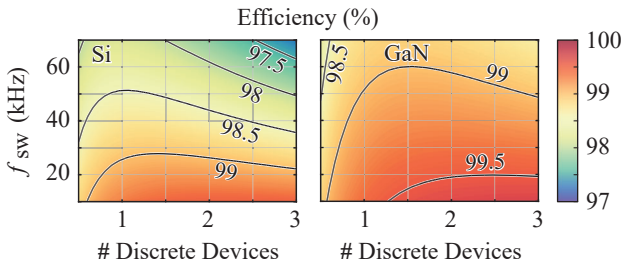


**Fig. 7:** Nominal (rated) load efficiency of the 7L FCi, where a nominal output voltage amplitude of $\hat{V}_{\mathrm{out}} = 340\,\mathrm{V}$ and an electrical output frequency of $f_{\mathrm{out}} = 200\,\mathrm{Hz}$ are assumed.

### A. Design of Power Semiconductor Stage

For the Si and GaN power semiconductors a proper inverter design means that on the one hand the number of parallel semiconductor devices per switch $N_{\mathrm{par}}$ and the switching frequency $f_{\mathrm{sw}}$ are selected in such a way that at nominal load the demanded efficiency of $> 99\,\%$ is achieved, and on the other hand during overload intervals the maximum specified junction temperature ($175\,^{\circ}\mathrm{C}$ for Si and $150\,^{\circ}\mathrm{C}$ for GaN) is not exceeded. Thus, to get a first insight of possible switching frequencies $f_{\mathrm{sw}}$ and number of parallel devices per switch $N_{\mathrm{par}}$, the nominal load efficiency is calculated for a switching frequency range of $10\,\mathrm{kHz} - 70\,\mathrm{kHz}$, while up to three discrete devices per switch are considered. It should be mentioned that the temperature-dependent on-state resistance $R_{\mathrm{ds,on}}$ is determined based on the resulting semiconductor junction temperatures $T_{\mathrm{J}}$ deduced from the thermal models given in **Fig. 5**. Furthermore, in all cases a constant ambient temperature of $90\,^{\circ}\mathrm{C}$ and a relatively small current ripple of maximal $10\,\%$ (worst case for switching losses) is assumed, which typically is in this range when no LC output filter but a motor with a large inductance is used. The resulting nominal efficiencies for different $N_{\mathrm{par}}$ and $f_{\mathrm{sw}}$ for a Si and GaN power stage are shown in **Fig. 7**, where for Si-MOSFETs a maximum switching frequency of roughly $f_{\mathrm{sw}} = 25\,\mathrm{kHz}$ with one Si device per switch (i.e. $N_{\mathrm{par}} = 1$) and for GaN-HEMT devices the highest switching frequency of around $f_{\mathrm{sw}} = 60\,\mathrm{kHz}$ for two chips per switch (i.e. $N_{\mathrm{par}} = 2$) is achieved. However, as also listed in **Table IV**, the performance difference with respect to other $N_{\mathrm{par}}$ is relatively small, which means that for the proper selection of $N_{\mathrm{par}}$ also the overload capability must be considered.

As already discussed in Section II, since the inverter must be able to provide the overload torque during $3\,\mathrm{s}$ also at standstill, i.e. $> 4 \cdot \tau_{\mathrm{semi}}$, for the selection of $N_{\mathrm{par}}$ the worst case scenario can be assumed, where one inverter bridge-leg is permanently conducting the peak overload current of $45\,\mathrm{A}$. At the same time the semiconductors of this bridge-leg should not exceed their maximum specified operating junction temperatures, which in steady state are only defined by the thermal resistances. Hence, from the given motor case temperature of $90\,^{\circ}\mathrm{C}$ and the maximum junction temperatures of $175\,^{\circ}\mathrm{C}$ for Si and $150\,^{\circ}\mathrm{C}$ for GaN, the maximum allowed thermal resistance $R_{\mathrm{th,tot,max}}$ per semiconductor device depending on $N_{\mathrm{par}}$ can be calculated for different switching frequency at overload $f_{\mathrm{sw,ol}}$, as shown in **Fig. 8**. Consequently, as long as $R_{\mathrm{th,tot,max}}$ is larger than the measured total thermal resistances $R_{\mathrm{th,tot,Si}} = 0.91\,\mathrm{K/W}$ or $R_{\mathrm{th,tot,GaN}} = 1.81\,\mathrm{K/W}$ of the realized Si and GaN half-bridges (indicated with horizontal lines), a valid semiconductor design is obtained. It should be noted that for $N_{\mathrm{par}} > 1$ the current and thus also the losses per semiconductor device reduce, which means that for $N_{\mathrm{par}} > 1$ a higher $R_{\mathrm{th,tot,max}}$ can be accepted. The intersection of $R_{\mathrm{th,tot,max}}(f_{\mathrm{sw,ol}})$ with $R_{\mathrm{th,tot,Si}} = 0.91\,\mathrm{K/W}$ or $R_{\mathrm{th,tot,GaN}} = 1.81\,\mathrm{K/W}$ actually defines the maximum allowable $f_{\mathrm{sw,ol,max}}$ during overload operation. As an example, for a single Si device per switch, a maximum switching frequency of $f_{\mathrm{sw,ol,max}} = 225\,\mathrm{kHz}$ can be selected until the maximum junction temperature is reached, while for two GaN devices per switch, the switching frequency boundary at overload is around $f_{\mathrm{sw,ol,max}} = 280\,\mathrm{kHz}$. A complete list of all configurations is found in **Table IV**, where also the efficiency at overload (for nominal speed) as well as the maximum switching frequencies at nominal load and overload are given, which are finally important for the proper design of the passive components, i.e. the flying capacitors as well as the optional LC output filter.

### B. Design of Passive Components

Besides the semiconductor devices, also the passive components, i.e. the flying capacitors (FCs) as well as the optional LC output filter, have to be designed for the overload operation. In contrast to the semiconductors, a short overload doesn't primarily pose a thermal but - especially for motor integrated drives - more a volumetric problem. For example, the voltage ripple of the FCs as well as the flux density in the output inductor increase proportionally with the output current, which means that the FC capacitance and the inductor core cross-section have to be increased, thus the passive components have to be designed for overload conditions. In order to counteract this increase in volume, it would be possible to increase the switching frequency during overload, since e.g. the FC volume also scales inversely proportional with the selected switching frequency. However, a higher switching frequency during overload is somehow counter-intuitive and typically the opposite is done, since at overload the switches are already highly stressed with a much larger current and higher conduction losses (e.g. at least 9 times higher losses for 3 times larger current), but concerning passive component volume an increase in frequency would be even beneficial as explained in the following.

For the FC capacitance $C_{\mathrm{FC}}$, a proportional increase of the switching frequency with the overload would be optimal, since in this case the required capacitance $C_{\mathrm{FC}}$ to keep the voltage ripple within the same bounds is independent from the output current. In the considered case this means that the switching frequency has to be increased by a factor of three ($f_{\mathrm{sw,ol}} = 3 \cdot f_{\mathrm{sw,nom}}$). As shown in **Table IV**, $3 \cdot f_{\mathrm{sw,nom}}$ is perfectly feasible with already one Si or two GaN devices per switch,

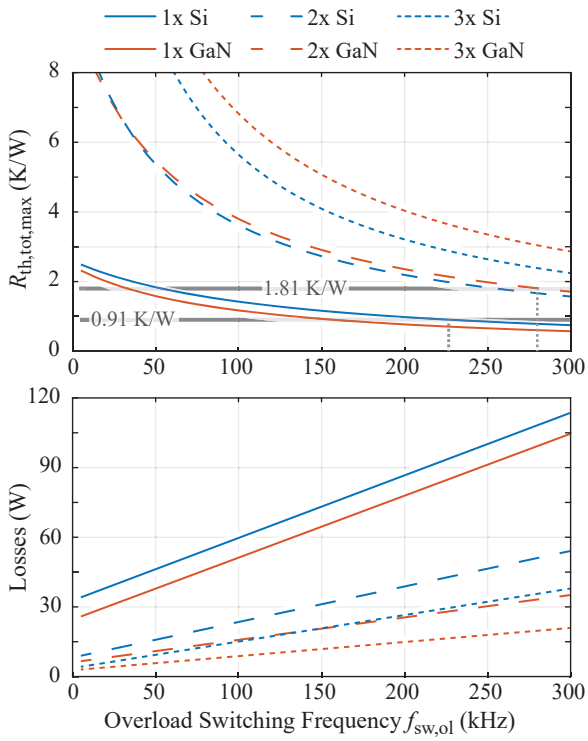


**Fig. 8:** Maximum allowed total thermal resistance depending on the selected switching frequency $f_{\mathrm{sw,ol}}$ at overload for different number of parallel semiconductor devices per switch $N_{\mathrm{par}}$. The horizontal lines correspond to the measured total thermal resistances $R_{\mathrm{th,tot,Si}} = 0.91\,\mathrm{K/W}$ and $R_{\mathrm{th,tot,GaN}} = 1.81\,\mathrm{K/W}$ of the realized Si and GaN half-bridges (cf. **Table III**). The intersection of these curves determines the maximum allowable overload switching frequency $f_{\mathrm{sw,ol,max}}$ for each configuration.

**TABLE IV:** Compilation of number of parallel devices for Si and GaN with their respective switching frequencies and overload efficiencies at nominal speed.

| | **Npar** | $\mathbf{f_{sw,nom}}$ (kHz) | $\mathbf{f_{sw,ol,max}}$ (kHz) | $\mathbf{3 \cdot f_{sw,nom}}$ (kHz) | $\eta(\mathbf{3 \cdot f_{sw,nom}})$ % |
|---|---|---|---|---|---|
| Si | 1 | 25 | 225 | 75 | 97.4 |
| Si | 2 | 23 | $> 400$ | 69 | 98.1 |
| Si | 3 | 19 | $> 400$ | 57 | 98.4 |
| GaN | 1 | 50 | 30 | 150 | 96.7 |
| GaN | 2 | 60 | 280 | 180 | 97.6 |
| GaN | 3 | 50 | $> 400$ | 150 | 98.1 |

since $3 \cdot f_{\mathrm{sw,nom}}$ is still well below $f_{\mathrm{sw,ol,max}}$, which also means that the resulting junction temperature is well below its maximum rating. Consequently, the FC capacitance can be designed for nominal load and to still achieve an efficiency of $> 99\,\%$, with two parallel GaN devices per switch a 2.4 times higher $f_{\mathrm{sw,nom}}$ can be selected compared to one Si device. Accordingly, thus for a given FC voltage ripple, the needed FC capacitance $C_{\mathrm{FC}}$ is by the same factor smaller for GaN compared to Si.

With an increase in switching frequency also the needed volume of an optional LC output filter can be limited, which especially in motor integrated drives is problematic. Nevertheless, independently from integration, an LC output filter helps to mitigate EMI emissions, partial discharge in the motor winding insulation or bearing currents. There, the filter inductor volume also scales with the output current [31], since it is typically dimensioned in such a way that magnetic saturation is avoided, i.e. also for the maximum current at overload [32]. However, since in the considered case the switching frequency at overload $f_{\mathrm{sw,ol}}$ could be increased by a factor of three (due to $C_{\mathrm{FC}}$), the filter inductance $L_{\mathrm{out}}$ could theoretically drop by the same amount without changing the output current ripple during overload. This means that the filter inductor is not designed magnetically for the overload, but is consciously operated in partial saturation with only $1/3$ of the nominal inductance. This clearly results in elevated core losses, but since the thermal capacitances of magnetic components are much larger than the ones of semiconductors, an overload of a few seconds can easily be handled.

For the realization of such an inductor, an iron powder instead of the typically used ferrite core could be employed, since it shows a much smoother reduction of the permeability with increasing flux density compared to ferrite materials whose permeability drastically drops above saturation. However, to find a proper inductor design where at both operating points, i.e. nominal load and overload, the desired inductances are obtained, is challenging. This means, if the inductor is designed for nominal load, it cannot be guaranteed that at overload the inductance drops by the desired amount. If e.g. the inductance reduction is less, this means that with $f_{\mathrm{sw,ol}} = 3 \cdot f_{\mathrm{sw,nom}}$ the current ripple for overload is even less than for nominal load. Consequently, concerning inductor optimization, an increase in frequency of $3 \cdot f_{\mathrm{sw,nom}}$ would not be needed. The larger current ripple during overload could even be beneficial, since this typically reduces the switching losses. In contrast, however, the increasing conduction losses due to a higher effective current or the larger output voltage ripple at the filter capacitor $C_{\mathrm{out}}$ also have to be considered. As a consequence, a proportional increase of the switching frequency (assumed due to $C_{\mathrm{FC}}$ and $C_{\mathrm{out}}$) must not be optimal for all components. Hence, in a further study a detailed converter-level Pareto optimization is required, where all different influences on the optimal switching frequency are considered. In general, however, it can be stated that an increase in switching frequency during overload is a further degree of freedom to minimize the needed volume of passive components.

## IV. 7-Level Inverter Overload Capability

As mentioned in the previous chapter, the increase of a factor of three (best case for FCs) probably defines an upper bound and thus coincides with the worst case overload scenario for the power semiconductors. Therefore, for the following analysis where the overload capability of the 7L FCi depending on the output frequency, i.e. speed, is investigated, an overload switching frequency of $f_{\mathrm{sw,ol}} = 3 \cdot f_{\mathrm{sw,nom}}$ is assumed. As mentioned, for this increase in frequency at minimum one Si and two parallel GaN devices per switch have to be selected, which is used in the following analysis.

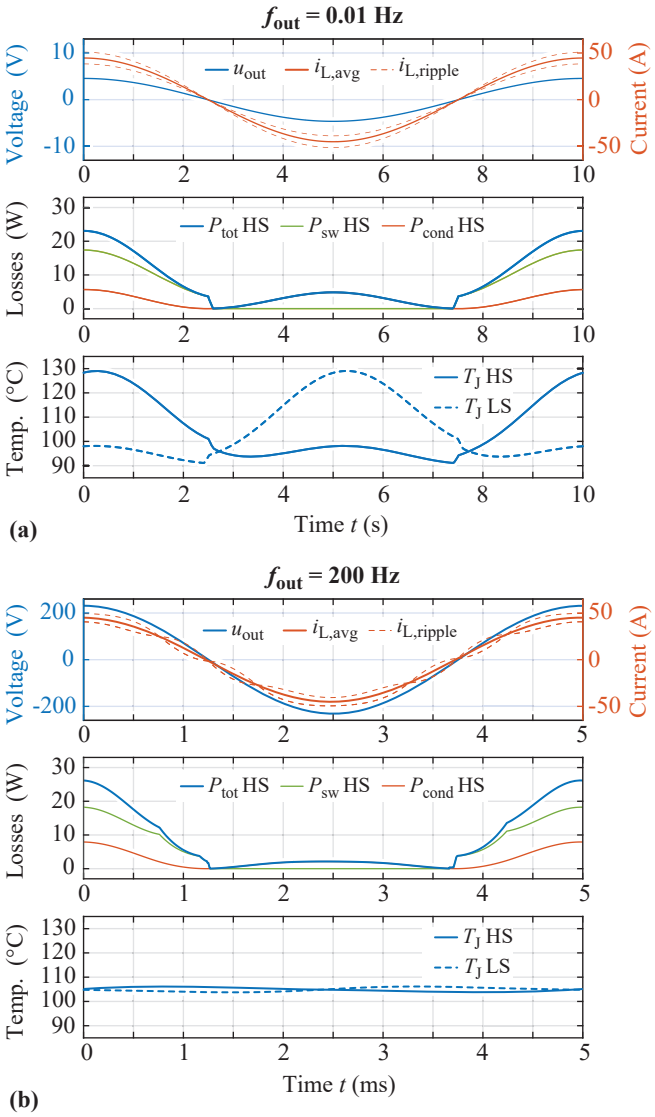


**Fig. 9:** Simulated semiconductor losses and junction temperature profiles of two parallel high-side (HS) and low-side (LS) GaN devices at overload and a switching frequency of $f_{sw,ol} = 180\,\text{kHz}$ for **(a)** a very low electrical output frequency of $f_{out} = 0.01\,\text{Hz}$ and **(b)** the nominal output frequency $f_{out} = 200\,\text{Hz}$ to illustrate the drop in junction temperature variation with increasing $f_{out}$.

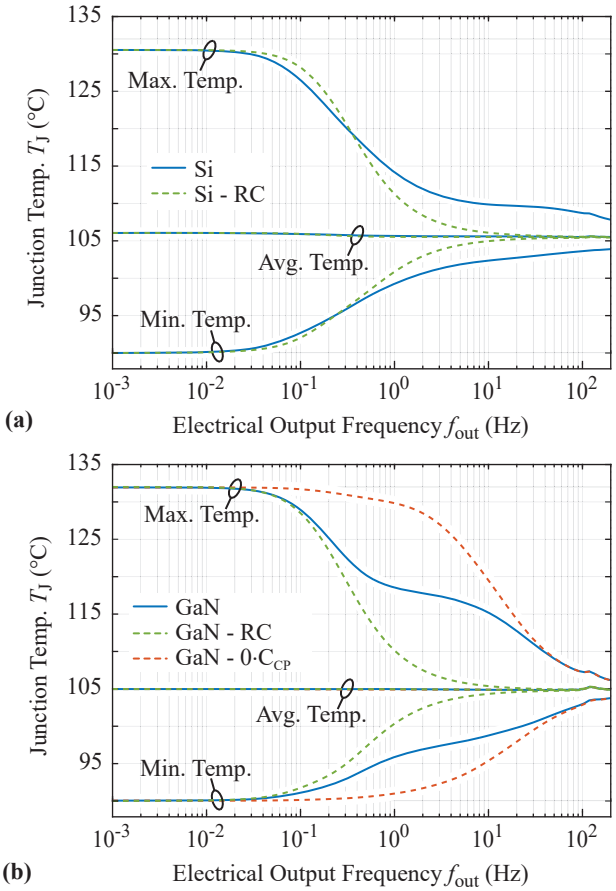


**Fig. 10:** Junction temperature fluctuation around the average junction temperature depending on the electrical output frequency $f_{out}$ for **(a)** one Si and **(b)** two GaN devices per switch (plotted in log-scale) determined with the experimentally deduced models (solid blue lines) and the simplified RC model (green dashed lines) discussed in Section II. For the GaN devices, the influence of the thermal capacitance of the copper piece is shown by removing the thermal capacitance from the model (red dashed lines).

This choice actually results in a fair comparison, since e.g. in Section II the copper piece attached to the GaN chip was selected as half the size of one Si-MOSFET package, thus if the same packaging technology is applied to GaN devices, a similar molded SMD package size would result. Furthermore, as already mentioned, the maximum overload duration of one semiconductor device for a certain overload can directly be deduced for standstill operation based on the thermal time constant $\tau_{semi}$, and also coincides with the maximum system overload duration, since in this case only one bridge-leg is permanently overloaded. However, as soon as the machine starts to rotate, i.e. an electrical output frequency $f_{out} > 0\,\text{Hz}$ is generated, the phases are no more stressed with a DC but with a sinusoidal current, which means that in average within one electrical period the current stress is evenly distributed to all three inverter phases. However, especially for a low output frequency $f_{out}$, the conduction losses still pulsate in each phase with $2 \cdot f_{out}$, whereas the switching losses pulsate with $f_{out}$. Therefore, also the junction temperature shows a pulsation within the electrical period as illustrated in **Fig. 10 (a)** for two parallel GaN devices. Clearly, if the output frequency is increased, this temperature pulsation is more and more smoothed out **Fig. 10 (b)**. It should be mentioned that for both cases, the junction temperature profile is determined from the calculated time-dependent losses in combination with the derived transient thermal models. In addition, for the switching loss calculation again a relatively small current ripple of $10\,\%$ is considered (worst case), and the induced motor voltage is proportionally scaled with the output frequency considering a voltage constant of $k_u = u_{emf}/\omega_{out} = 0.18\,\text{Vs/rad}$ and a winding resistance of $0.1\,\Omega$, since the output voltage defines the required duty cycle and thus the distribution of the

conduction losses between high- and low-side switch.

In **Fig. 10**, the maximum and minimum junction temperatures with respect to the electrical output frequency are shown (in frequency log-scale similar to a Bode diagram) for both selected semiconductor technologies, i.e. one Si and two GaN devices per switch. It can be noted that the junction temperature stays below $135\,^{\circ}\mathrm{C}$ even at standstill for both cases, since the selected switching frequency at overload of $f_{\mathrm{sw,ol}} = 3 \cdot f_{\mathrm{sw,nom}}$ is well below $f_{\mathrm{sw,ol,max}}$. Furthermore, already for low output frequencies the maximum junction temperature as well as the temperature fluctuation start to drop (blue lines). This is also beneficial concering the reliability of the semiconductor devices, since the number of cycles to failures increase with smaller junction temperature variation [33], [34].

Instead of using the determined thermal model, a lumped RC low-pass filter with the equivalent time constants $\tau_{\mathrm{Si}} = 0.4\,\mathrm{s}$ and $\tau_{\mathrm{GaN}} = 0.65\,\mathrm{s}$ deduced in Section II can be used, which results in the junction temperature behavior as indicated with the green dashed line in **Fig. 10**. As can be noted, the corner frequencies of the experimentally determined thermal model and the simplified RC model match quite well, which means that already based on the thermal time constants of the semiconductor devices the effective corner frequency can be roughly estimated and the temperature ripple amplitude depending on $f_{\mathrm{out}}$ is determined as for a first-order low-pass filter. However, while for the simple thermal RC-model and high $f_{\mathrm{out}}$ the temperature variation decays to zero, the empirically determined model still shows a residual temperature ripple. As discussed in Section II, this can be explained by the initial step in the step response shown in Fig. 6, which is due to the small thermal capacitance of the semiconductor device. As can be noted, since the Si chip has a lower thermal contact resistance to the exposed pad, the residual temperature variation is smaller compared to the GaN chip. Finally, for the GaN device also the influence of the thermal capacitance of the copper piece is illustrated (cf. red dashed line in **Fig. 10 (b)**), whereby the influence of the change in the thermal resistance due to a smaller contact area to the TIM is ignored. If the copper piece is removed, the corner frequency increases by roughly a decade and thus strongly degrades the overload capability of the 7L FCi at low speeds, particularly if also the increasing thermal resistance due to the lower contact area between GaN chip and TIM would be considered. Consequently, with GaN devices a similar overload capability as for Si-MOSFETs is only achievable if either a sophisticated cooling concept is used or if GaN devices would also be available in similar SMD packages as used for Si-MOSFETs featuring a dedicated (top-side) cooling pad.

## V. Conclusion

In this paper, the overload capability of a motor-integrated $7.5\,\mathrm{kW}$ 7-Level Flying Capacitor inverter (7L FCi) employing either $200\,\mathrm{V}$ Si-MOSFET or $200\,\mathrm{V}$ GaN-HEMT devices is analyzed. In order to properly design the 7L FCi for a $99\,\%$ nominal efficiency and a 3 times overload operation within $3\,\mathrm{s}$, first the transient thermal models for the two semiconductor technologies are empirically determined. For the surface-mounted Si-MOSFETs the lowest thermal resistance of $0.91\,\mathrm{K/W}$ is achieved by cooling the device through the PCB with a copper inlay. For GaN-HEMT devices, available in a passivated die form, a top-side cooling is proposed, where first a copper piece is attached to the GaN chip top (acting as heat spreader) before it is insulated from the heatsink with a thermal interface material. There, with $1.8\,\mathrm{K/W}$, twice the thermal resistance compared to Si-MOSFETs, however, due to the copper piece similar thermal time constants of $\tau_{\mathrm{Si}} = 0.4\,\mathrm{s}$ and $\tau_{\mathrm{GaN}} = 0.65\,\mathrm{s}$ are obtained. The elaborated thermal models are used to design the 7L FCi, i.e. the number of parallel devices per switch and switching frequencies $f_{\mathrm{sw}}$, for $99\%$ nominal efficiency and 3 times overload capability. It results that one Si device and two GaN devices per switch are reasonable choices. For Si-MOSFETs, a maximum nominal switching frequency of $25\,\mathrm{kHz}$ can be selected, while for GaN devices it can be increased to $60\,\mathrm{kHz}$. As described in the paper, it is also reasonable to increase $f_{\mathrm{sw}}$ during overload operation, since this allows to limit the volume of the passive components. Even if $f_{\mathrm{sw}}$ is linearly increased with the output current amplitude, the maximum junction temperature $T_{\mathrm{J,max}}$ stays well below its absolute maximum ratings, i.e. around $130\,^{\circ}\mathrm{C}$ for the worst case at standstill. It is also shown that $T_{\mathrm{J,max}}$ decreases with increasing output frequency and settles in both cases around $105\,^{\circ}\mathrm{C}$ for nominal speed. It can be stated that $200\,\mathrm{V}$ GaN devices offer similar overload capability as their Si-counterparts and even can improve the VSD system performance with respect to either efficiency or passive component volume. However, it also has to be emphasized that the performances achieved for GaN devices are only possible due to a sophisticated cooling concept, thus in VSD systems, GaN devices are only competitive if similar SMD packages as used for Si-MOSFETs - featuring e.g. a dedicated top-side cooling pad to separate the electrical and thermal cirucits - become available.

## References


[1] T. M. Jahns and H. Dai, "The Past, Present, and Future of Power Electronics Integration Technology in Motor Drives," *CPSS Transactions on Power Electronics and Applications*, vol. 2, no. 3, pp. 197–216, 2017.

[2] M. Kaufhold, H. Aninger, M. Berth, J. Speck, and M. Eberhardt, "Electrical Stress and Failure Mechanism of the Winding Insulation in PWM-Inverter-Fed Low-Voltage Induction Motors," *IEEE Transactions on Industrial Electronics*, vol. 47, no. 2, pp. 396–402, 2000.

[3] A. Tessarolo, D. Giulivo, and M. Mezzarobba, "A System-Level Approach to the Optimal Dimensioning of Induction-Motor Variable-Frequency Drives," in *Proc. of the 13th European Conference on Power Electronics and Applications*, 2009, pp. 1–10.

[4] A. H. Mohamed, H. Vansompel, and P. Sergeant, "Electro-Thermal Design of a Discrete GaN Based Converter for Integrated Modular Motor Drives," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, pp. 1–1, 2021.

[5] J. W. Kolar, J. Biela, S. Waffler, T. Friedli, and U. Badstuebner, "Performance Trends and Limitations of Power Electronic Systems," in *Proc. of the 6th International Conference on Integrated Power Electronics Systems*, 2010, pp. 1–20.

[6] M. Ciappa, W. Fichtner, T. Kojima, Y. Yamada, and Y. Nishibe, "Extraction of Accurate Thermal Compact Models for Fast Electro-Thermal Simulation of IGBT Modules in Hybrid Electric Vehicles,"

*Microelectronics Reliability*, vol. 45, no. 9, pp. 1694–1699, 2005, Proc. of the 16th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0026271405002350

[7] M. Uğur and O. Keysan, "Multi-Physics Design Optimisation of a GaN-Based Integrated Modular Motor Drive System," *The Journal of Engineering*, vol. 2019, no. 17, pp. 3900–3905, 2019.

[8] P. R. Wilson, "Thermal Modeling and Analysis of Power Electronic Components and Systems," in *Power Electronics Handbook (4th Edition)*, M. H. Rashid, Ed. Butterworth-Heinemann, 2018, pp. 1441–1450. [Online]. Available: https://www.sciencedirect.com/science/article/pii/B9780128114070000520

[9] U. Drofenik and J. W. Kolar, "Teaching Thermal Design of Power Electronic Systems with Web-Based Interactive Educational Software," in *Proc. of the 18th Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, vol. 2, 2003, pp. 1029–1036 vol.2.

[10] Y. Shen, H. Wang, F. Blaabjerg, H. Zhao, and T. Long, "Thermal Modeling and Design Optimization of PCB Vias and Pads," *IEEE Transactions on Power Electronics*, vol. 35, no. 1, pp. 882–900, 2020.

[11] *EPC2047*, *EPC*, Jan. 2018.

[12] *IPT111N20NFD*, *Infineon Technologies*, Feb. 2016.

[13] *Alphacool Sarcon XR-m*, *AlphaCool Internaltional GmbH*, Feb. 2016.

[14] M. Ishiko and T. Kondo, "A Simple Approach for Dynamic Junction Temperature Estimation of IGBTs on PWM Operating Conditions," in *Proc. of the IEEE Power Electronics Specialists Conference*, 2007, pp. 916–920.

[15] E. A. Jones and M. de Rooij, in *Proc. of the IEEE 6th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), title=Thermal Characterization and Design for a High Density GaN-Based Power Stage, year=2018, volume=, number=, pages=295-302, doi=10.1109/WiPDA.2018.8569136*.

[16] T. Zhao, J. Wang, A. Q. Huang, and A. Agarwal, "Comparisons of SiC MOSFET and Si IGBT Based Motor Drive Systems," in *Proc. of the IEEE Industry Applications Annual Meeting (IAS)*, 2007, pp. 331–335.

[17] W. Perdikakis, M. J. Scott, K. J. Yost, C. Kitzmiller, B. Hall, and K. A. Sheets, "Comparison of Si and SiC EMI and Efficiency in a Two-Level Aerospace Motor Drive Application," *IEEE Transactions on Transportation Electrification*, vol. 6, no. 4, pp. 1401–1411, 2020.

[18] T. E. Salem and R. A. Wood, "1000-h Evaluation of a 1200-V, 880-A All-SiC Dual Module," *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2192–2198, 2014.

[19] J. M. Erdman, R. J. Kerkman, D. W. Schlegel, and G. L. Skibinski, "Effect of PWM Inverters on AC Motor Bearing Currents and Shaft Voltages," *IEEE Transactions on Industry Applications*, vol. 32, no. 2, pp. 250–259, 1996.

[20] D. Busse, J. Erdman, R. J. Kerkman, D. Schlegel, and G. Skibinski, "Bearing Currents and their Relationship to PWM Drives," *IEEE Transactions on Power Electronics*, vol. 12, no. 2, pp. 243–252, 1997.

[21] G. L. Skibinski, R. J. Kerkman, and D. Schlegel, "EMI Emissions of Modern PWM AC Drives," *IEEE Industry Applications Magazine*, vol. 5, no. 6, pp. 47–80, 1999.

[22] Y. Lei, C. Barth, S. Qin, W.-C. Liu, I. Moon, A. Stillwell, D. Chou, T. Foulkes, Z. Ye, Z. Liao *et al.*, "A 2-kW Single-Phase Seven-Level Flying Capacitor Multilevel Inverter with an Active Energy Buffer," *IEEE Transactions on Power Electronics*, vol. 32, no. 11, pp. 8570–8581, 2017.

[23] M. Guacci, J. Azurza Anderson, K. L. Pally, D. Bortis, J. W. Kolar, M. J. Kasper, J. Sanchez, and G. Deboy, "Experimental characterization of silicon and gallium nitride 200 v power semiconductors for modular/multilevel converters using advanced measurement techniques," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 3, pp. 2238–2254, 2020.

[24] S. Qin, Z. Liao, Z. Ye, D. Chou, N. Brooks, and R. C. Pilawa-Podgurski, "A 99.1% Efficient, 490 W/in$^3$ Power Density Power Factor Correction Front End Based on a 7-Level Flying Capacitor Multilevel Converter," in *Proc. of the IEEE Applied Power Electronics Conference and Exposition (APEC)*. IEEE, 2018, pp. 729–736.

[25] J. Azurza Anderson, G. Zulauf, P. Papamanolis, S. Hobi, S. Mirić, and J. W. Kolar, "Three Levels Are Not Enough: Scaling Laws for Multilevel Converters in AC/DC Applications," *IEEE Transactions on Power Electronics*, vol. 36, no. 4, pp. 3967–3986, 2021.

[26] *Conductonaut*, *Thermal Grizzly*.

[27] "Solder Paste Sn63/Pb37," http://www.chipquik.com/datasheets/SMD291AX10.pdf, accessed: 2$^{th}$ Jan. 2021.

[28] "Thermal Paste t-Global Technology," http://www.tglobaltechnology.com/uploads/files/tds/TG-S606P.pdf, accessed: 15$^{th}$ March 2021.

[29] "Thermal Performance of EPC eGaN FETs - Application Note AN011," https://epc-co.com/epc/Portals/0/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf, accessed: 29$^{th}$ March. 2021.

[30] *A655sc*, *FLIR*.

[31] M. Antivachis, D. Bortis, D. Menzi, and J. W. Kolar, "Comparative Evaluation of Y-Inverter against Three-Phase Two-Stage Buck-Boost DC-AC Converter Systems," in *Proc. of the IEE International Power Electronics Conference (IPEC-Niigata - ECCE Asia)*, 2018, pp. 181–189.

[32] L. Wei, J. McGuire, and R. A. Lukaszewski, "Analysis of PWM Frequency Control to Improve the Lifetime of PWM Inverter," *IEEE Transactions on Industry Applications*, vol. 47, no. 2, pp. 922–929, 2011.

[33] S. Song, S. Munk-Nielsen, C. Uhrenfeldt, and I. Trintis, "Failure Mechanism Analysis of a Discrete 650V Enhancement Mode GaN-on-Si Power Device With Reverse Conduction Accelerated Power Cycling Test," in *Proc. of the IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2017, pp. 756–760.

[34] M. Andresen, K. Ma, G. Buticchi, J. Falck, F. Blaabjerg, and M. Liserre, "Junction Temperature Control for More Reliable Power Electronics," *IEEE Transactions on Power Electronics*, vol. 33, no. 1, pp. 765–776, 2018.