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***Abstract*—Single-phase-supplied variable-speed drive (VSD) systems are widely used in industrial applications, typically following a two-stage design with a boost-type power factor correction (PFC) rectifier at the input and a three-phase voltage source inverter (VSI) at the output. However, the reliance on large electrolytic DC-link capacitors, required to buffer power pulsations at twice the grid frequency, together with the boost inductor, introduces drawbacks in terms of reliability, volume, cost, and complexity. To address these limitations, a dual-inverter topology with a three-phase open-end winding (OEW) machine and the motor power pulsation buffer (MPPB) concept is employed. In this approach, power pulsations are absorbed by the total drive system's inertia, drastically reducing the required DC-link capacitance and thereby eliminating the need for electrolytic capacitors, which enables a more compact, reliable, and long-lifespan drive system.**

This paper presents hardware verification of the dual-inverter MPPB system. A custom-built 1.8 kW demonstrator, supplied from a single-phase 230 V_{rms} AC grid and driving a three-phase OEW motor, is developed and experimentally tested. The measured waveforms confirm that power pulsations are buffered in the mechanical inertia rather than in capacitors, while maintaining PFC operation, regulating the secondary DC-link voltage, and ensuring stable speed control. These results validate the effectiveness of the dual-inverter MPPB concept.

***Index Terms*—Dual-Inverter Topology, Electrolytic Capacitor-Less, Hardware Verification, IGBT Inverter, Open-End Winding PMSM, PFC Operation, Single-Phase, VSD**

I. Introduction

In many industrial applications, variable-speed drive (VSD) systems in the lower kilowatt range, such as those used for compressors, fans, blowers, and pumps, are supplied from a single-phase AC grid [1]. In other cases, single-phase supply must also be employed at higher power levels when no three-phase connection is available, for example, in AC-fed railway systems [2]–[5]. VSD systems commonly utilize three-phase permanent magnet synchronous machines (PMSMs) because of their high torque density, low weight, high efficiency, and compact design [6]. Consequently, a power electronic converter is required to transform the single-phase AC input into a balanced three-phase voltage system with variable amplitude and frequency, enabling speed control of the machine. Moreover, the converter must ensure unity power factor operation, i.e., the input current must remain proportional to the input voltage, to reduce harmonic distortion and reactive power drawn from the grid.

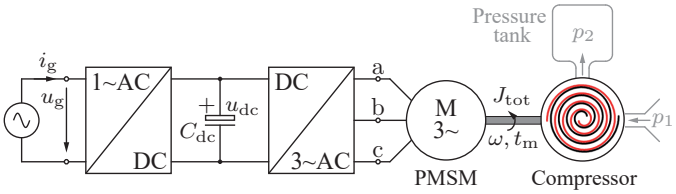


Fig. 1: Overview of the conventional single-phase supplied VSD system, as typically employed in railway applications. The system consists of a front-end PFC rectifier with a large electrolytic DC-link capacitor, followed by an inverter stage that drives the motor, which in turn drives the compressor.

These requirements are typically met by a two-stage architecture consisting of a single-phase power factor correction (PFC) rectifier and a three-phase voltage source inverter (VSI), separated by an intermediate DC-link capacitor [7] (see example of a compressor drive system in **Fig. 1**). Various circuit topologies can be implemented for both the PFC rectifier [8] and the VSI [9]. Nevertheless, the most common configuration employs a unidirectional single-phase boost-type PFC rectifier, realized by a diode bridge followed by a boost converter, in combination with a conventional three-phase two-level VSI [10].

Single-phase supplied drive systems inherently exhibit power pulsations at twice the grid frequency. In conventional single-phase PFC stages, these pulsations are buffered by large electrolytic DC-link capacitors, with capacitance values C_{dc} typically in the millifarad range, to maintain a quasi-constant DC-link voltage for the downstream VSI [11]. In summary, state-of-the art single-phase supplied drive systems rely on a dedicated boost PFC rectifier stage and a bulky electrolytic capacitor, which are both unfavorable with respect

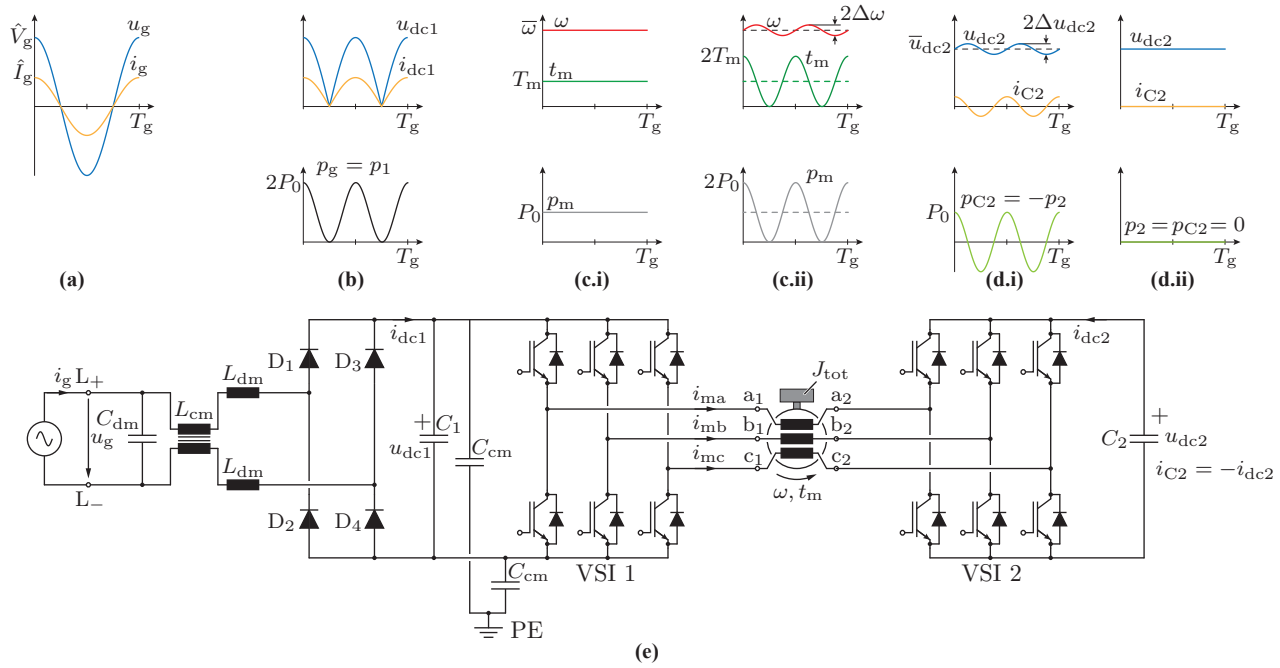


Fig. 2: (a-d) Voltage, current, speed, torque, and power waveforms of the **(i)** conventional dual inverter control scheme with an electrolytic capacitor C_2 required to buffer the pulsating grid power and **(ii)** proposed dual inverter control that buffers the input pulsating power using the mechanical inertia of the drive system. **(e)** Single-phase dual-inverter power circuit comprising two inverters supplying an open-end winding (OEW) PMSM. The EMI filter consists of L_{dm}, C_{dm}, L_{cm}, and C_{cm}, providing differential-mode and common-mode noise attenuation.

to reliability, size, cost, and overall system complexity.

Consequently, several concepts for single-phase supplied drive systems have been proposed in the literature [12], [13], aiming to eliminate the boost converter by connecting the three-phase VSI directly to the diode bridge. This approach reduces the component count and avoids the drawbacks associated with the conventional two-stage architecture. Such solutions are conceptually simple and enable low-cost implementations; however, they suffer from significant limitations. The input current becomes discontinuous, and PFC operation is no longer feasible. In particular, near the zero-crossings of the grid voltage, the maximum output voltage achievable by the VSI, approximately half of the grid voltage amplitude, falls below the induced machine voltage. As a result, both machine control and input current control are lost. This issue becomes even more pronounced at higher rotational speeds, where the induced machine voltage increases, leading to extended zero-current intervals and, consequently, a higher current total harmonic distortion (THD) [14].

To restore PFC operation and ensure full controllability of the machine currents, concepts employing open-end winding (OEW) PMSMs with dual inverters have been introduced [6]. In this approach, a second three-phase inverter (VSI 2) is connected to the opposite machine winding ends and supplied through a floating DC-link capacitor, while the first inverter (VSI 1) is tied to the single-phase diode rectifier, as illustrated in **Fig. 2**. As shown in **Fig. 2(a,b,c.i,d.i)**, the PMSM operates at constant instantaneous speed, such that the single-phase grid power oscillation is buffered by C_2. In this arrangement, VSI 1 processes the pulsating input power p_{g}, consisting of a constant component P_0 and a pulsating term $\tilde{p}_{\mathrm{g}} = p_{\mathrm{g}} - P_0$, to achieve unity power factor operation. Meanwhile, the machine delivers a constant mechanical output power $p_{\mathrm{m}} = P_0$ to the load, and VSI 2 balances the zero-mean pulsating power at twice the grid frequency, $p_{\mathrm{C2}} = \tilde{p}_{\mathrm{g}}$. Since the DC-link capacitor C_2 of VSI 2 must maintain an approximately constant voltage u_{dc2} [15], a large electrolytic capacitor C_2 is required. This, however, imposes major drawbacks with respect to cost, volume, and particularly system lifetime [16].

To eliminate the need for an electrolytic capacitor in the dual-inverter drive of [6], a novel control strategy was introduced by the authors in [17]. In this approach, the power pulsation at twice the grid frequency is buffered by exploiting the inertia of the machine and/or the drive train. This method, referred to as the *Machine Power Pulsation Buffer* (MPPB) [18], effectively operates a three-phase PMSM in a manner similar to a single-phase machine. As shown in **Fig. 2(b,c.ii,d.ii)**, the motor torque t_{M} exhibits a $100\,\%$ ripple, as in single-phase operation, while the resulting single-sided speed ripple

$$\Delta\omega = \frac{P_0}{4\pi f_G \overline{\omega} J_{\mathrm{tot}}} \tag{1}$$

remains small (only a few percent) due to the high total system inertia J_{tot} (see **Fig. 2(c.ii)** for $\Delta\omega$ definition). Consequently, VSI 2 is only required to generate the voltage necessary for current control, without processing any low-frequency pulsating grid power. This drastically reduces the required capacitance of the secondary DC-link capacitor C_2, making

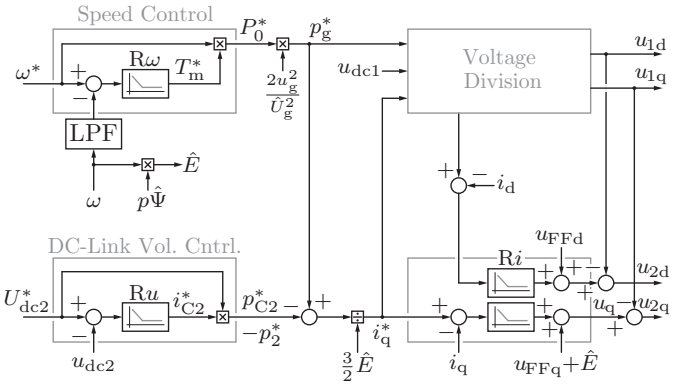


Fig. 3: Implemented control scheme ensuring PFC operation of the dual-inverter single-phase supplied drive system, with the single-phase power pulsation buffered by the motor/drive train's inertia.

it feasible to replace electrolytic capacitors with ceramic or film types. While [17] provides a detailed analysis of this control concept and validates it through simulations, experimental verification has been missing. To address this gap, the present paper reports hardware measurements on a dedicated demonstrator of the dual-inverter topology without electrolytic capacitors.

II. Control Structure

For the experimental evaluation, the control scheme shown in **Fig. 3** is implemented on the hardware demonstrator. The scheme consists of an inner current-control loop (Ri controller), complemented by outer loops for speed regulation (Rω controller) and DC-link voltage control of VSI 2 (Ru controller). The PI speed controller generates the torque reference, which is multiplied by the speed reference to yield the average power reference P_0^*. This reference is then modulated according to the instantaneous grid voltage,

$$\frac{2u_\mathrm{g}^2}{\hat{U}_\mathrm{g}^2} = 2\sin^2(\omega_\mathrm{g} t), \tag{2}$$

where we assume the grid voltage to be equal to

$$u_\mathrm{g} = \hat{U}_\mathrm{g}\sin(\omega_\mathrm{g} t), \tag{3}$$

where the value of the peak grid voltage $\hat{U}_\mathrm{g}$ is specified in **Tab. I**. The resulting grid power reference in the control scheme in **Fig. 3** is given by

$$p_\mathrm{g}^* = 2P_0^*\sin^2(\omega_\mathrm{g} t). \tag{4}$$

From this, the required power for maintaining the voltage of C_2 is subtracted, yielding the mechanical power reference of the motor

$$p_\mathrm{m}^* = p_\mathrm{g}^* - p_\mathrm{C2}^*. \tag{5}$$

The power associated with capacitor C_2 is calculated as the product of the capacitor current reference i_C2^*, generated by the DC-link voltage controller Ru, and the reference voltage of the secondary DC link,

$$p_\mathrm{C2}^* = U_\mathrm{dc2}^*\, i_\mathrm{C2}^*. \tag{6}$$

From the motor power reference p_m^*, the q-axis current reference is obtained as

$$i_\mathrm{q}^* = \frac{2}{3}\,\frac{p_\mathrm{m}^*}{\hat{E}}, \tag{7}$$

where $\hat{E}$ is the induced voltage amplitude. The latter is determined from the measured speed according to

$$\hat{E} = p\,\hat{\Psi}\,\omega, \tag{8}$$

with p denoting the number of pole pairs and $\hat{\Psi}$ the flux linkage of the PMSM.

The voltage division block in **Fig. 3** is implemented as a feed-forward structure, providing the VSI 1 voltage reference directly from the instantaneous values of p_g^*, u_dc1, and i_q^*, which is described in the following. In the first step, the reference amplitude of the machine current in the *dq*-frame is calculated by

$$i_\mathrm{m}^* = \max\left(\frac{p_\mathrm{dq}^*}{u_\mathrm{1max}},\, i_\mathrm{q}^*\right), \tag{9}$$

where

$$p_\mathrm{dq}^* = \frac{2}{3}\,p_\mathrm{g}^*, \tag{10}$$

and

$$u_\mathrm{1max} = \frac{u_\mathrm{dc1}}{2}. \tag{11}$$

The d-axis current reference is then obtained as

$$i_\mathrm{d}^* = \sqrt{(i_\mathrm{m}^*)^2 - (i_\mathrm{q}^*)^2}. \tag{12}$$

To ensure that the motor operates such that the voltage generated by VSI 1,

$$u_1 = \frac{p_\mathrm{dq}^*}{i_\mathrm{m}^*}, \tag{13}$$

is in phase with the machine current i_m^*, the same *dq*-angle φ must be maintained for both voltage and current. This angle is determined from the current components as

$$\cos\varphi = \frac{i_\mathrm{d}^*}{i_\mathrm{m}^*}, \qquad \sin\varphi = \frac{i_\mathrm{q}^*}{i_\mathrm{m}^*}. \tag{14}$$

Accordingly, the outputs of the voltage division block are obtained as

$$u_\mathrm{1d} = u_1\,\frac{i_\mathrm{d}^*}{i_\mathrm{m}^*}, \qquad u_\mathrm{1q} = u_1\,\frac{i_\mathrm{q}^*}{i_\mathrm{m}^*}. \tag{15}$$

With the two motor current references i_d^* and i_q^* known (see (12) and (7)), the current controller R_i is implemented in the same manner as in conventional cascaded machine control, using PI feedback regulators. To improve performance, feed-forward terms are added to account for cross-coupling between the d- and q-axes as well as the induced speed voltages in the dq reference frame, namely

$$v_\mathrm{FFd} = -\omega p L i_\mathrm{q}^*, \tag{16}$$

and

$$v_\mathrm{FFq} = \omega p L i_\mathrm{d}^* + \hat{E}, \tag{17}$$

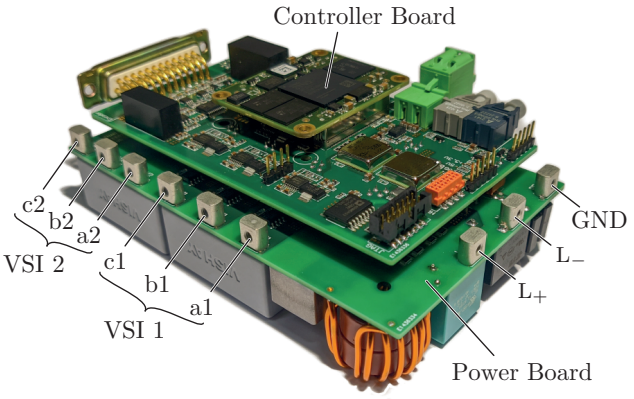


Fig. 4: Dual-inverter hardware demonstrator integrating the input EMI filter, diode bridge rectifier, C_1, VSI 1, VSI 2, and C_2 (see **Fig. 2(e)**). The setup is rated for up to 1.8 kW output power and employs Infineon IM535-U6D six-pack IGBT modules [19].

Parameters	Symbol	Value
Single-Phase Grid		
RMS grid voltage	$U_{\mathrm{g,rms}}$	230 V
Peak grid voltage	$\hat{U}_{\mathrm{g}}$	325 V
Inverter Parameters		
DC-link capacitance	C_1	10 µF
DC-link capacitance	C_2	20 µF
Switching frequency	f_{sw}	16 kHz
DM inductance	L_{dm}	33 µH
DM capacitance	C_{dm}	1 µF
CM inductance	L_{cm}	620 µH
CM capacitance	C_{cm}	5.7 nH
Motor Parameters		
Stator resistance	R	5.6 mΩ
Stator inductance	L	0.45 mH
Number of pole pairs	p	6
Flux linkage	$\hat{\Psi}$	0.043 Wb
Total moment of inertia	J_{tot}	0.01 kgm^2
Controller gains		
Ri closed-loop bandwidth	f_{cc}	3 kHz
Ri proportional gain	K_{pc}	5 V/A
Ri integral gain	K_{ic}	696 V/(As)
Ru closed-loop bandwidth	f_{cu}	500 Hz
Ru proportional gain	K_{pu}	0.01 A/V
Ru integral gain	K_{iu}	500 A/(Vs)
Rω closed-loop bandwidth	f_{cs}	300 Hz
Rω proportional gain	K_{ps}	0.4 sNm
Rω integral gain	K_{is}	50 Nm

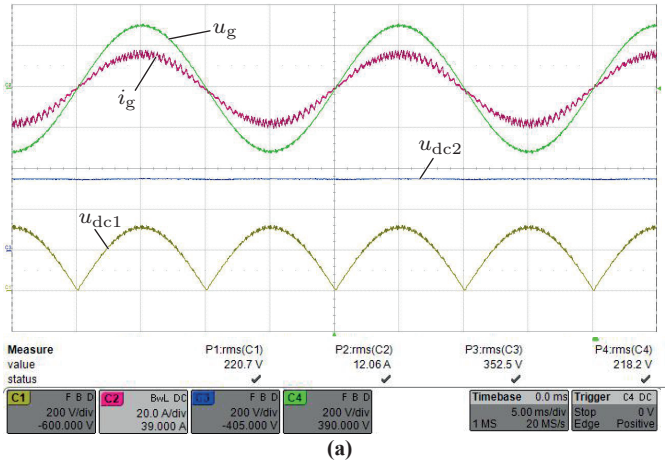
TABLE I: Dual-Inverter Parameters.

where L is the PMSM's stator inductance. The resulting machine voltages v_{d} and v_{q} are thus obtained. Finally, by subtracting the already derived voltage components of VSI 1, $v_{1\mathrm{d}}$ and $v_{1\mathrm{q}}$, the remaining reference voltages for the secondary inverter, $v_{2\mathrm{d}}$ and $v_{2\mathrm{q}}$, are determined.

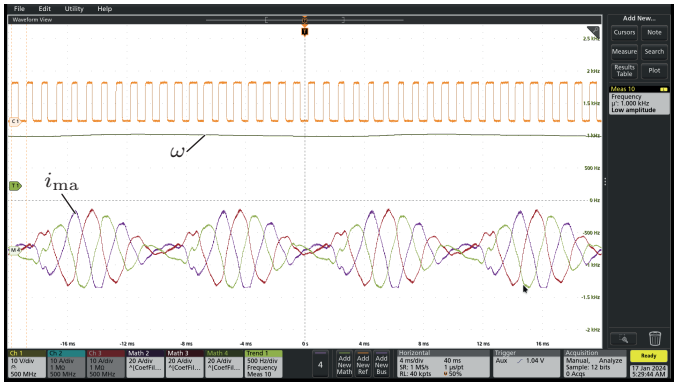
Additional details on the control strategy can be found in [17].

III. Measurement Results

The control scheme shown in **Fig. 3** is implemented on the hardware demonstrator of **Fig. 4**, using the parameters listed in **Tab. I**. The controllers are designed with distinct



(a)



(b)

Fig. 5: Experimental measurements of the dual-inverter VSD system with MPPB control, corresponding to the schematic in **Fig. 2(e)**. **(a)** Grid voltage u_{g}, grid current i_{g}, and DC-link voltages of VSI 1 (u_{dc1}) and VSI 2 (u_{dc2}). Oscilloscope settings: 200 V/div (voltage) and 20 A/div (current). **(b)** Measured speed and motor phase currents. Oscilloscope settings: 500 Hz/div and 10 A/div. The speed is obtained from the frequency of a 20-tooth gear measured by an inductive sensor (top orange square waveform), where a frequency of 1 kHz corresponds to $1\,\mathrm{kHz} \times 60/20 = 3000\,\mathrm{rpm}$.

bandwidths, separated in frequency. The innermost loop, the current controller, operates with the highest bandwidth of 3 kHz. The DC-link voltage controller of VSI 2 runs at about one-sixth of this value, with a bandwidth of 500 Hz, while the outer speed controller is the slowest, with a bandwidth of 300 Hz. The corresponding controller gains, summarized in **Tab. I**, are derived from these bandwidth specifications.

The measurement results obtained from the dual-inverter hardware demonstrator driving the PMSM are presented in **Fig. 5**. As shown in the schematic of **Fig. 2(e)**, the DC-link capacitors C_1 and C_2 (see also **Tab. I**) are implemented with film capacitors and have capacitances only in the microfarad range. Owing to their small values, C_1 and C_2 do not contribute to buffering the single-phase grid power pulsation. Instead, this task is accomplished through the proposed MPPB concept. Therefore, the effectiveness of the proposed concept is clearly demonstrated by the measurement results. This is further proven by the fact that despite the low DC-link

capacitance values, unity power factor operation is maintained, as evidenced by the sinusoidal grid current, which is in phase with the grid voltage and exhibits a measured THD of only $4.46\,\%$. The voltage of the secondary DC link, u_{dc2}, is successfully regulated at the desired value of $300\,\mathrm{V}$.

The measured DC-link voltages u_{dc1} and u_{dc2} further confirm that the single-phase power pulsation is not buffered by the capacitors: u_{dc1} directly follows the rectified grid voltage, while the average of u_{dc2} remains constant. For the sake of comparison, to constrain u_{dc2} between $u_{\mathrm{dc2,min}} = 277\,\mathrm{V}$ and $u_{\mathrm{dc2,max}} = 333\,\mathrm{V}$ by buffering the pulsating power with the capacitance C_2, the required capacitance would be

$$C_2 > \frac{2P_0}{\omega_{\mathrm{g}}\left(u_{\mathrm{dc2,max}}^2 - u_{\mathrm{dc2,min}}^2\right)} = 318\,\mu\mathrm{F}, \qquad (18)$$

which is 16 times larger than the C_2 used in our demonstrator (see **Tab. I**).

The phase current waveforms show that the grid power pulsation is instead absorbed by the motor's inertia. In accordance with the pulsating grid power, $100\,\%$ torque oscillations are present, resulting in motor phase currents with amplitudes modulated at the grid frequency, which is a characteristic signature of the MPPB concept. These torque oscillations induce only minor peak-to-peak speed variations of $\Delta n_{\mathrm{mech}} = 113\,\mathrm{rpm}$, corresponding to about $3.8\,\%$ of the average reference speed of $3000\,\mathrm{rpm}$.

Overall, the measurements confirm the effectiveness of the MPPB concept in the single-phase supplied dual-inverter topology.

IV. Conclusions

This paper presented the hardware verification of a single-phase AC dual-inverter topology employing the Machine Power Pulsation Buffer (MPPB) concept. By utilizing the drive system's inertia to buffer the inherent twice-grid-frequency power pulsation, the MPPB approach drastically reduces the required DC-link capacitance and eliminates the need for bulky electrolytic capacitors. A custom-built dual-inverter demonstrator, based on IGBT modules and film capacitors of only $10\,\mu\mathrm{F}$ (VSI 1) and $20\,\mu\mathrm{F}$ (VSI 2), was developed to validate the concept.

The experimental results confirm that the dual-inverter system reliably drives a three-phase open-end winding PMSM from a single-phase grid, achieving unity power factor operation. The pulsating power results in modulated motor phase current amplitudes and $100\,\%$ torque oscillations with twice grid frequency, which are effectively buffered by the motor's inertia, i.e., the motor speed remains nearly constant, with variations limited to about $3.3\,\%$, demonstrating the robustness of the concept.

Compared to conventional capacitor-based buffering, which would require 16 times higher capacitance and therefore electrolytic capacitors, the MPPB approach enables a far more compact, cost-efficient, and long-lifespan inverter solution. These results highlight the potential of the MPPB-based dual-inverter topology as a promising alternative for applications where system reliability, power density, and lifetime are critical.

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