



Power Electronic Systems
Laboratory

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Proceedings of the 12th Annual IEEE Energy Conversion Congress and Exposition (ECCE 2020),
Detroit, MI, USA, October 11-15, 2020

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Optimized Cascaded Controller Design for a 10 kW / 100 kHz Large Signal Bandwidth AC Power Source

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Abstract—The control system of a phase-modular three-phase 10 kW / 230 V_{rms} Ultra-High bandwidth series/parallel interleaved multi-level AC Power Source (UHPS) for P-HIL applications with 4.8 MHz effective switching frequency is optimized with respect to high bandwidth and low output impedance or output admittance (depending on whether output voltage or output current is controlled), by adding selected and effective enhancements to existing control structures. The theoretical findings are verified by means of a detailed simulation model, which also takes time-discretization effects arising from the FPGA-based digital control unit into account. The comparative evaluation of the investigated control structures reveals that the combination of capacitor current feedback, inductor voltage feedforward, and reference prediction performs best for the control of both, output voltage and output current. In this regard, at 100 kHz and for operation with rated load resistance of 5.3 Ω, the phase-lag of the output voltage of the optimized voltage control system can be reduced from 19°, for the conventional two-loop control structure, to 7°; the small-signal bandwidth increases from 235 kHz to 427 kHz; and the output impedance at 100 kHz decreases from 0.6 Ω to 143 mΩ. In case of output current control, at an output frequency of 60 kHz, and for rated load resistance, the phase-lag of the output current can be reduced from 51° to 33°, for an optimized three-loop control structure, which is accompanied by an increase of the small-signal bandwidth from 63 kHz to 89 kHz and an increase of the output impedance from 11 Ω to 30 Ω at 60 kHz.

I. INTRODUCTION

AC power sources are key components of Power-Hardware-In-the-Loop (P-HIL) testing environments [1]. **Fig. 2** presents a single phase of the investigated phase-modular three-phase power source, which is a triple-interleaved three-level flying capacitor converter (3L3) with a rated power of 10 kW that enables low realization complexity due to the natural balancing of the flying capacitors [2], [3], and a very high effective switching frequency of 4.8 MHz (cf. **Tab. I**). In **Fig. 2**, which presents a block diagram of the phase unit involving the control structure, the 3L3 is replaced with an equivalent voltage source $v_{\text{set}} = \sum_i v_{\text{sw},i}/3$ and the three filter inductors $3 \cdot L_1$ of the first filter stage are simplified to the equivalent filter inductor L_1 . **Fig. 3** demonstrates two example applications of this power source (shown for one phase), i.e., grid emulation for power converter testing and the emulation of electrical machines [4]. Thus, depending on the application, the power source is required to feature voltage or current source characteristic. Furthermore, very high control bandwidth enables extended investigations, e.g., to analyze the behavior of the Device Under Test (DUT) in presence of high-frequency distortions of the supply voltage emulated by the AC power source. The capability of the AC power source is further enhanced by featuring a controlled output impedance,

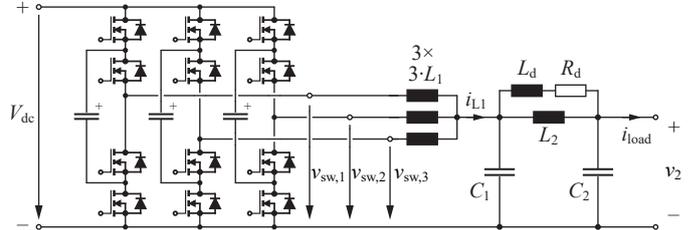


Fig. 1: Structure of the power circuit of a 10 kW/230 V_{rms} phase unit of the Ultra-High bandwidth AC Power Source (UHPS) with three interleaved three-level bridge-legs (3L3).

which is a powerful tool for advanced inspections of the DUT and denotes a further aspect of this research.

The control of output voltage or output current of a power converter with output filter is commonly achieved with a multi-loop control structure [5], [6], e.g., an inner-loop current controller and an outer-loop voltage controller; the emulation of an output impedance, Z_{out} , of the power source is realized by decreasing its output voltage in accordance to the desired impedance and the load current, $-Z_{\text{out}} I_{\text{load}}$ [7], [8]. In order to increase the achievable bandwidth of the output voltage or current control, numerous strategies are proposed in literature, including feedforward of reference voltage and load current [9], [10], state feedback [11], dead-beat control [12], model predictive control [13], nonlinear techniques, e.g., V^2 control [14], and hybrid amplifier concepts [15]. However, most publications only consider systems with low switching frequencies in the kHz range.

The AC power source presented in **Section II** of this paper is designed for exceptionally high large- and small-signal bandwidths of > 100 kHz and > 400 kHz, respectively, which renders more complex control schemes, e.g., model predictive control, unsuitable due to the very limited available computation time of ≈ 100 ns. Instead, in **Section III**, selected and effective enhancements are added to existing control structures, which add only low complexity to the digital control algorithm. The obtained control structures are fully optimized according to [10] in order to enable a fair comparison. According to the obtained findings, the combination of capacitor current feedback, inductor voltage feedforward, and reference prediction facilitates highest performance values for the control of both, output voltage and output current. With this, the control system for output voltage control achieves a small-signal bandwidth of 427 kHz at rated load, $R_{\text{load}} = 5.3 \Omega$, and a phase-lag of 7° at an output frequency of 100 kHz. Furthermore, the output current controller facilitates a small-signal bandwidth of 89 kHz and a phase-lag of 33° at 60 kHz and rated load. The results of a detailed simulation model,

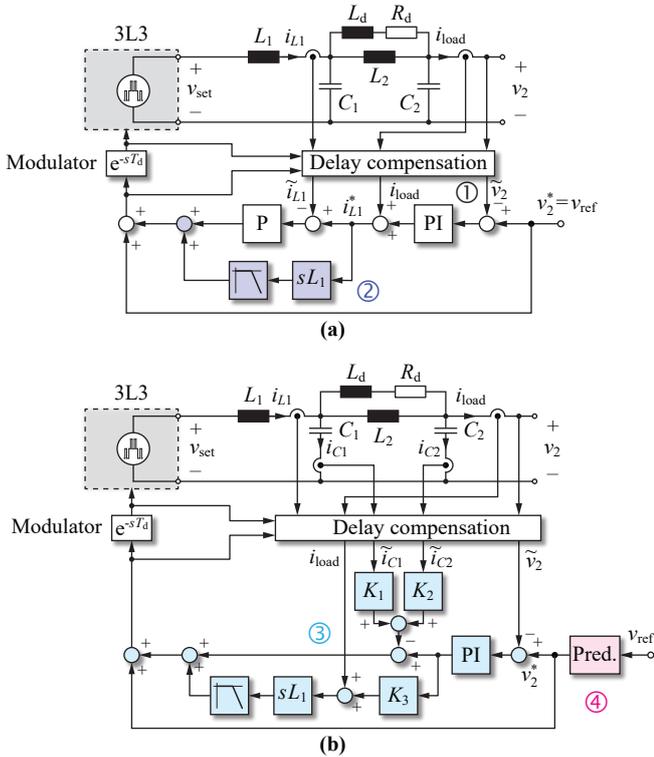


Fig. 2: Control system overview of the investigated UHPS (100 kHz full-scale bandwidth). Different control concepts are evaluated: (a) two-loop cascaded control structure ① and the extension by an inductor voltage feedforward ② to achieve increased bandwidth; (b) capacitor current feedback and inductor voltage feedforward ③ and reference prediction ④ to reduce the phase-lag of the output voltage with respect to the reference voltage. All control structures feature dead time compensation units according to [9], [10]. To simplify the analysis, the system delays of different entities are summarized in the PWM modulator as a single transport delay, T_d .

which incorporates a complete model of the power stage and also takes time-discretization effects arising from the FPGA-based digital control unit into account, are used to verify the theoretical findings.

II. SYSTEM STRUCTURE

The 3L3 converter system depicted in Fig. 1 has been selected due to its excellent dynamic properties and the achievable high signal quality. It consists of three interleaved branches ($N_{par} = 3$) where each is implemented as a three-level ($N_{ser} = 3$) flying capacitor bridge-leg. In total, there are six switching cells that are operated with a switching frequency of $f_s = 800$ kHz, each comprised of a pair of switches and a flying capacitor. The system is operated with a DC-link voltage of 800 V. In a split DC-link configuration four-quadrant operation up to peak voltages of 350 V is achievable. A more detailed overview of the 3L3 is presented in [16].

The output voltage generated by the parallel interleaved multi-level bridge-legs features an effective switching frequency of $f_{eff} = N_{par} \cdot (N_{ser} - 1) \cdot f_s = 4.8$ MHz and is processed with a two-stage LC output filter that has been designed using a filter design-space-based optimization approach [17] such that the filter's reactive power consumption for operation at 100 kHz large signal output and 10 kW remains below a defined limit.

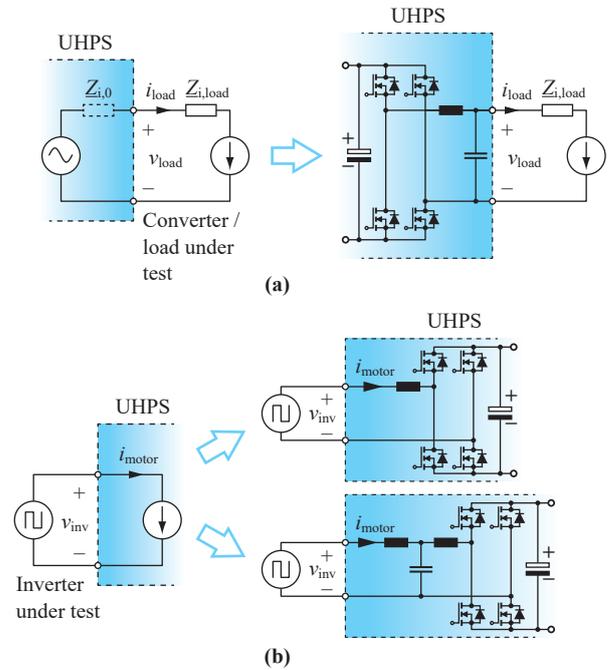


Fig. 3: Selected applications of the investigated bidirectional UHPS shown in simplified form as single H-bridge circuit: (a) testing of a load, e.g., a power converter where the UHPS features voltage source characteristic; (b) motor emulation to test a connected inverter (current source operation of the UHPS). In (b), the filter of the UHPS may be of 1st or 3rd order, depending on whether high bandwidth or high signal current quality is more important.

III. CONTROL SYSTEM OF THE UHPS

Analog-to-digital conversion, computation times, and synchronous PWM generation cause substantial delays in digitally controlled power converters, which limit the achievable control bandwidth. Therefore, time delays in the 3L3 converter are first detailed in Section III-A. Subsequently, the control system is exploited in Section III-B.

A. Time Delays in the 3L3 Converter

A PWM unit with triangular carrier, operated with synchronous double update mode, refreshes the duty cycle after every update period, $T_{up} = T_s/2 = 1/(2f_s)$, and causes a total delay of

$$T_{d,sync} = \frac{3}{2}T_{up} + T_{add}, \quad (1)$$

where $T_{add} = 70$ ns denotes the additional delays that arise from dead time units, signal isolators, gate drivers, and transistors. Due to the high number of switching cells and the

TABLE I: Target specifications of the 3L3 converter.

Number of parallel interleaved branches, N_{par}	3
Number of voltage levels per branch, N_{ser}	3
Large-signal bandwidth	> 100 kHz
Output voltage amplitude (full bandwidth)	325 V
Output power (AC, four-quadrant operation)	10 kW
Nominal load resistance, R_{nom}	5.3 Ω
Effective switching frequency, f_{eff}	4.8 MHz
DC-link voltage	800 V
Semiconductor switching frequency f_s	800 kHz

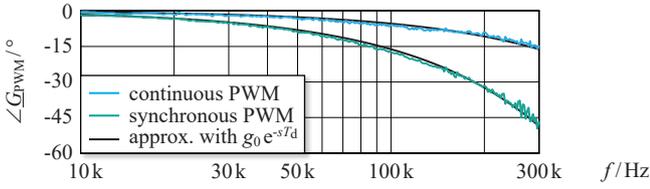


Fig. 4: Simulated (cyan and green) and calculated (black) time delays for the 3L3 converter. Quasi-continuous PWM achieves minimum time delay.

high effective switching frequency, the duration of the update period decreases to

$$T_{\text{up}} = f_{\text{eff}}^{-1} = (N_{\text{par}} \cdot (N_{\text{ser}} - 1) \cdot f_s)^{-1} \quad (2)$$

as compared to a single cell inverter topology and, thus, also $T_{\text{d,sync}}$ decreases accordingly. **Fig. 4** depicts simulated (green curve) and calculated time delays (black curve) of the 3L3 with $f_s = 800$ kHz, and $T_{\text{add}} = 70$ ns. The time delays, calculated with $e^{-j2\pi f T_{\text{d,sync}}}$ match well to the simulated results, with differences in the range of $\pm 2^\circ$. The distortions at high frequencies ($f > 200$ kHz) in the simulated curves arise from a finite PWM quantization resolution.

A further reduction of the time delay can be achieved by quasi-continuous operation of the PWM unit, i.e., with the Analog-to-Digital Converters (ADCs) sampling at high frequency, e.g., 100 MHz, and the FPGA continuously updating the controllers and PWM units (this is comparable to an analog implementation of measurements, controllers, and PWM unit plus a time delay). For given delays of ADCs, digital signal processing, and power stage, a total delay of

$$T_d = T_{\text{meas}} + T_{\text{calc}} + T_{\text{add}} = 50 \text{ ns} + 40 \text{ ns} + 70 \text{ ns} = 160 \text{ ns} \quad (3)$$

results (cyan curve in Fig. 4).

The control system of the UHPS uses quasi-continuous PWM, to achieve minimum delay. For the purpose of simplification of the control design, the total delay, T_d , is attributed to the PWM unit.

Each of the final control structures takes delay compensation into account, in accordance to [9], [10]. This is a model-based approach, which uses the reference voltage and the measured output quantities to predict the filter currents and output voltage used in the feedback loops ahead in time. It reduces the impact of time delays caused by the digital control system, gate drivers, and measurements on the achievable control bandwidth. The implementation uses two first-order differential equations for the inductor current, i_{L1} , and the capacitor voltage, v_2 , cf. Fig. 2(b):

$$\begin{aligned} \frac{di_{L1}(t)}{dt} &= \frac{v_{L1}(t)}{L_1} \approx \frac{v_{\text{set}}(t) - v_2(t)}{L_1}, \\ \frac{dv_2(t)}{dt} &\approx \frac{i_{L1}(t) - i_{\text{load}}(t)}{C_1 + C_2}. \end{aligned} \quad (4)$$

The predicted values are obtained based on the approximations

$$\begin{aligned} \frac{di_{L1}(t)}{dt} &\approx \frac{i_{L1}(t + \Delta t) - i_{L1}(t)}{\Delta t}, \\ \frac{dv_2(t)}{dt} &\approx \frac{v_2(t + \Delta t) - v_2(t)}{\Delta t}, \end{aligned} \quad (5)$$

i.e., by equating (4) and (5),

$$\begin{aligned} i_{L1}(t + \Delta t) &= i_{L1}(t) + \frac{v_{\text{set}}(t) - v_2(t)}{L_1} \Delta t, \\ v_2(t + \Delta t) &= v_2(t) + \frac{i_{L1}(t) - i_{\text{load}}(t)}{C_1 + C_2} \Delta t \end{aligned} \quad (6)$$

result. The expression is iteratively and analytically evaluated on n steps to compensate for the total time delay T_d by using $\Delta t = T_d/n$ in each step.

B. Ultra-High Bandwidth Voltage Control

In a first step, the aim is to control the output voltage with as high as possible bandwidth and as small as possible inner impedance, to cover applications according to Fig. 3(a).

From an initial investigation of different control structures, the three structures listed below are found to be most suitable.

- 1) *Two-loop PI-P control structure:* This structure is referred to with ① in Fig. 2(a) and has been selected since it is well known and commonly used. It is composed of an inner current (P) controller and an outer voltage (PI) controller,

$$\underline{K}_i(s) = K_{\text{pi}}, \quad \underline{K}_v(s) = K_{\text{pv}} [1 + (sT_{\text{iv}})^{-1}], \quad (7)$$

that control the inductor current and the output voltage, respectively. It includes the feedforwards for reference voltage and load current, which are known to allow for increased bandwidth and increased robustness with regard to the connected load [9], [10].

- 2) *Inductor voltage feedforward:* The two-loop control structure is further enhanced by the addition of an inductor voltage feedforward, which is marked with ② in Fig. 2(a). This is an estimate of the inductor voltage calculated using the inductor current reference,

$$v_{L1,\text{est}}(t) = L_1 \frac{di_{L1}^*}{dt}, \quad (8)$$

that is frequency-limited by a 2nd-order Bessel low-pass filter and added to the reference to increase the bandwidth of the current control loop.

- 3) *Capacitor current feedback with inductor voltage feedforward:* This control structure, illustrated in Fig. 2(b) and referred to with ③, uses a single PI controller for the output voltage control, a capacitor current feedback network that realizes active damping of the output filter's resonant pole [9], and different feedforward networks, including an inductor voltage feedforward, to enhance the achievable control bandwidth. Among all investigated control structures, highest bandwidth has been achieved with this structure.

All three multi-loop control structures are individually optimized to maximize the achievable bandwidth while ensuring an acceptable dynamic performance. This enables an unbiased comparison of the configurations. The criteria used to assess the dynamic performance are defined in accordance to [10] and are listed below.

- 1) *Frequency domain response:* The reference transfer function of the system is evaluated to determine the achieved -0.5 dB and -3 dB bandwidths, $f_{0.5\text{dB}}$ and $f_{3\text{dB}}$, and the phases at the corresponding frequencies, $\varphi_{0.5\text{dB}}$ and $\varphi_{3\text{dB}}$.

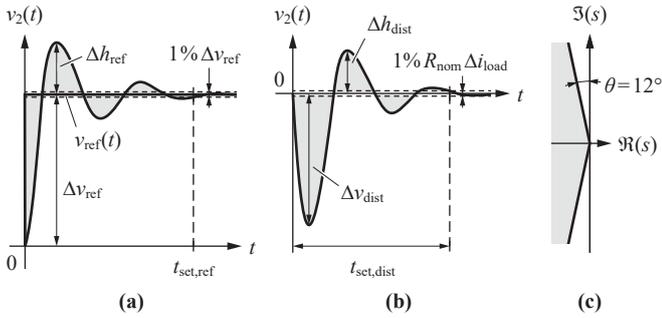


Fig. 5: Illustration of the criteria used to assess the performance of the control system: (a) reference step response, (b) response arising from a step change in the load current, (c) valid pole locations of closed-loop systems.

2) *Reference step response, Fig. 5(a)*: The evaluation considers the relative overshoot, $M_v = \Delta h_{\text{ref}} / \Delta v_{\text{ref}}$, and the settling time until the output is within $\pm 0.5\% \cdot \Delta v_{\text{ref}}$, which is named $t_{\text{set,ref}}$. Additionally, the reference tracking error is assessed by means of the Integral of the Time-weighted Absolute value of the Error of the voltage step response (ITAE),

$$e_{\text{itae,ref}} = \int_0^{t_{\text{set,ref}}} t \cdot |v_{\text{ref}}(t) - v_2(t)| dt. \quad (9)$$

3) *Disturbance step response, Fig. 5(b)*: The performance due to a step change in the load current, Δi_{load} , is assessed with three criteria: the relative overshoot, $M_i = \Delta h_{\text{dist}} / \Delta v_{\text{dist}}$ (Δv_{dist} is the initial dip of the output voltage), the settling time, $t_{\text{set,dist}}$, that denotes the time until the output remains within $v_{\text{ref}} \pm 0.5\% \cdot R_{\text{nom}} \Delta i_{\text{load}}$, and the ITAE criterion,

$$e_{\text{itae,dist}} = \int_0^{t_{\text{set,dist}}} t \cdot |v_{\text{ref}}(t) - v_2(t)| dt. \quad (10)$$

The optimizations of the voltage control structures consider resistive load conditions and take the extreme load conditions into account, i.e., no load ($R_{\text{load}} \rightarrow \infty$) and full load ($R_{\text{load}} = 5.3 \Omega$).

In addition to the performance metrics, the controller designs are subject to defined limitations in order to focus on solutions featuring acceptable performance values and ensure stability. The employed limitations are listed below.

- The poles of all closed-loop transfer functions (e.g., closed inductor current control loop, closed output voltage control loop) must reside to the left of the region depicted in **Fig. 5(c)**. The two linear delimitations that characterize this region start at $0 + j0$ in the complex Laplace-domain and extend towards $-\infty \pm j\infty$ at an angle of 12° to the imaginary axis in order to enable both, fast dynamic response and adequate stability margin.
- Phase margin of open-loop transfer function for output voltage control must be greater than 30° .
- Reference step response: $M_v < 15\%$
- Disturbance step response: $M_i < 20\%$
- Maximum settling times: $100 \mu\text{s}$

A grid search algorithm, realized with multiple nested for-loops, systematically evaluates all possible sets of parameters within given ranges. Inside the innermost for-loop, the algorithm, firstly, disregards the designs that do not satisfy the

given stability and boundary conditions and, secondly, uses the performance metrics of valid designs to establish the design space.

The optimal gains are found in the course of a post-processing step, by minimizing a cost function that is given by the weighted sum of the performance metrics,

$$c = [\gamma_1 \ \gamma_2 \ \dots \ \gamma_8].$$

$$[f_{0.5 \text{ dB}} \ f_{3 \text{ dB}} \ M_v \ M_i \ t_{\text{set,ref}} \ t_{\text{set,dist}} \ e_{\text{itea,ref}} \ e_{\text{itea,dist}}]^T, \quad (11)$$

using $\gamma_{\{1,2\}} < 0$ and $\gamma_{\{3\dots 8\}} > 0$. The values of the weights, γ_i , have been selected manually in order to achieve a low overshoot and a high small-signal control bandwidth.

The presented results consider two simplifications: firstly, the employed two-stage filter is replaced by a single-stage LC filter (using $L = L_1 + L_2$ and $C = C_1 + C_2$) and, secondly, the delay compensator may also employ the undelayed set value, i.e., the value entering the modulator block in Fig. 2, which would not be accessible in a final realization. Respective refinements are subject to future work, although the presented methods remain the same and the achievable performance values will be very close to the presented results.¹ **Fig. 6** depicts the achieved reference transfer functions, $\underline{T}(s)$, in case of nominal load, $R_{\text{load}} = 5.3 \Omega$ and **Tab. II** summarizes the achieved main performance values:

- The phase-lag at the maximum output frequency of 100 kHz and full load, $\varphi_{100 \text{ kHz}}$;
- The achieved small-signal bandwidth at full load, f_{-45° , i.e., the frequency at which the phase-lag of the reference transfer function is -45° under full load condition.

Please note that the delay compensation is not used for control structure ②, since the optimization returns nearly same results with and without delay compensation. It has to be further noted that the cost function c can be adjusted depending on specific performance needs such as, e.g. maximum $f_{-3 \text{ dB}}$, maximum $f_{-45 \text{ deg}}$ or minimum $\varphi_{100 \text{ kHz}}$. According to these results, the addition of the inductor voltage feedforward leads to a significant performance improvement and the control structure ③, i.e., with capacitor current feedback, achieves overall best performance. In this regard, $\varphi_{100 \text{ kHz}}$ drops from -19° , in case of ①, to -11° for ② and -8° for ③. Even though, all three structures achieve similar performances up to a frequency of 100 kHz, structure ③ enables the highest small-signal bandwidth of 393 kHz (compared to 235 kHz for ① and 355 kHz for ②).

¹Due to $L_1 \gg L_2$, the filter transfer functions are nearly the same up to the considered small-signal bandwidths and only differ in the MHz range.

TABLE II: Performance values achieved for output voltage control.

Structure	Phase at 100 kHz (full load), $\varphi_{100 \text{ kHz}}$	Small-signal bandwidth (full load), f_{-45°
①	-19°	235 kHz
②	-11°	355 kHz
③	-8°	393 kHz
④	-7°	427 kHz

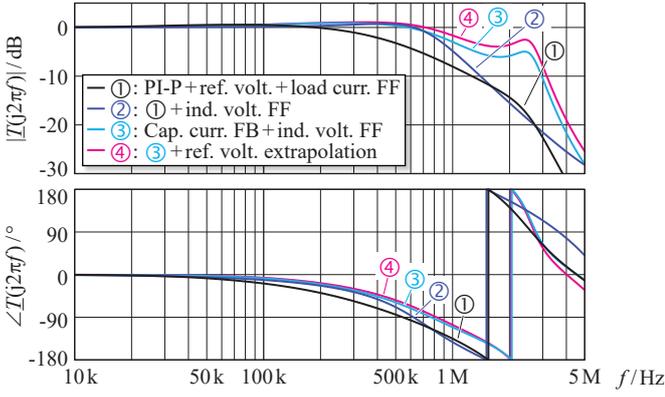


Fig. 6: Calculated reference transfer functions, $\underline{T}(s)$, for the control structures ① to ④, cf. Fig. 2, and $R_{\text{load}} = 5.3 \Omega$.

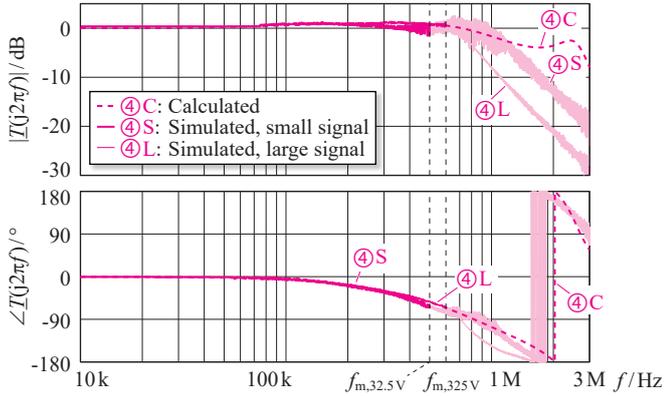


Fig. 7: Calculated and simulated transfer functions for $R_{\text{load}} = 5.3 \Omega$ and control structure ④, which features capacitor current feedback, inductor voltage feedforward, and reference prediction. The simulation is conducted for two different amplitudes, i.e., 325 V (large-signal) and 32.5 V (small-signal); $f_{m,325V}$ and $f_{m,32.5V}$ denote the frequency boundaries above which an output voltage with low distortion is only maintained if multiple switching events during half a switching period are allowed.

Further reduction of the phase-lag is possible by implementing an extrapolation of the reference function ④,

$$\tilde{v}_{\text{ref}}(t) = v_{\text{ref}}(t) + \frac{v_{\text{ref}}(t) - v_{\text{ref}}(t - T_{\text{prv}})}{T_{\text{prv}}/T_{\text{pred}}} \approx v_{\text{ref}}(t + T_{\text{pred}}), \quad (12)$$

which uses current and previous reference values ($T_{\text{prv}} = 30 \text{ ns}$, $T_{\text{pred}} = 150 \text{ ns}$). Since this method only modifies the waveform of the reference, it can be used without changing the controllers; however, with respect to v_{ref} , the overshoot increases. In order to limit the high-frequency gain caused by (12), a 1st-order low-pass filter with cut-off frequency of 1.4 MHz is connected in series to the reference extrapolation. With this, $\underline{T}(s)$ features a maximum gain of 1.6 dB in case of no load and, at full load, a phase-lag of 7° at 100 kHz and a small-signal bandwidth of 427 kHz.

Detailed simulation models, which consider the interleaved multi-level switching stage and incorporate a model of the digital signal processing unit that correctly reproduces the time-discretization due to the finite FPGA clock frequency, are used to verify the calculated results. By way of example, **Fig. 7** presents a simulated frequency response of

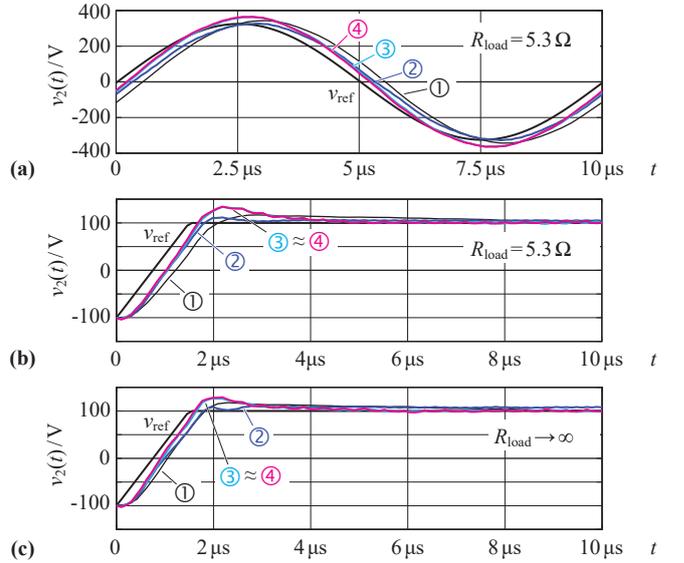


Fig. 8: (a) Simulated response of the converter to a sinusoidal reference (100 kHz, 325 V) and full load; (b) and (c) Simulated responses to a trapezoidal reference ($\pm 100 \text{ V}$, $133 \text{ V}/\mu\text{s}$) at (b) full load and (c) no load.

the reference transfer function for structure ④, by using a chirp signal for $v_{\text{ref}}(t)$ and two different voltage amplitudes of 325 V and 32.5 V, which refer to large-signal and small-signal excitations, respectively. The simulations confirm the calculated results up to a maximum frequency where either the power semiconductors are subject to multiple switching events during one half switching period ($f_{m,325V} = 600 \text{ kHz}$ and $f_{m,32.5V} = 500 \text{ kHz}$ in Fig. 7 for large-signal and small-signal operations, respectively) or where the power stage reaches its physical limits. Multiple switching events during $T_s/2$ can be avoided in the digital implementation by only allowing a single change of the output state during one half switching period, which, however, causes distortions of the output voltage at high frequencies. For this reason, the very high-frequency parts of the simulated frequency responses, shown with light-magenta color in Fig. 7, would be improved with multiple switching events being allowed.

Fig. 8(a) presents the simulated time-domain response to a sinusoidal excitation with a frequency of 100 kHz and an amplitude of 325 V under full-load conditions. In accordance to the analytical result, the phase-lag decreases from 19° to 11°, 8°, and, finally, 7° in ①, ②, ③, and, ④, respectively. **Figs. 8(b)** and **(c)** depict the responses of the output voltage to a trapezoidal reference voltage with $\Delta V_{\text{ref}} = 200 \text{ V}$ and $dv_{\text{ref}}/dt = 133 \text{ V}/\mu\text{s}$, at full load and no load, respectively. In case of full load, the delay time (measured for 0 – 10% of the final value) decreases from 510 ns in ① to 410 ns in ④ and the corresponding rise time (10% – 90%) decreases from 1.3 μs to 1.15 μs . The system remains stable also under no-load conditions, however, the maximum relative overshoot increases and reaches 15% in case of structure ④ under no-load condition.

Fig. 9 depicts the calculated output impedance of the UHPS, assuming a loss-less power converter. At 100 kHz, the resulting impedance is $0.6 \Omega e^{j96.5^\circ}$ for control structure ① and it

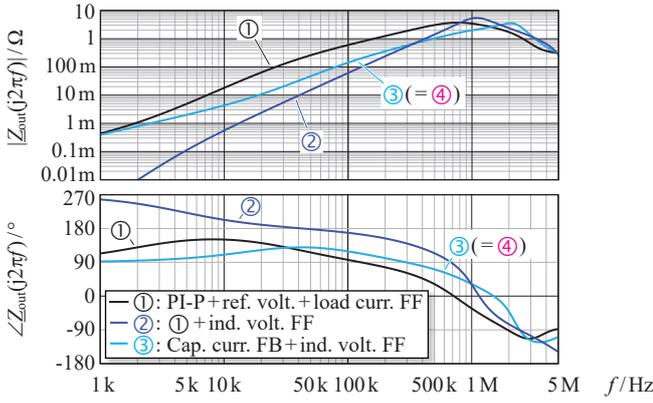


Fig. 9: Output impedance of the converter for output voltage control.

substantially decreases for control structures ② and ③ with values of $61 \text{ m}\Omega e^{j168^\circ}$ and $143 \text{ m}\Omega e^{j119^\circ}$ respectively.²

C. High Bandwidth Optimized Current Control

Contrary to the previous section, the aim is to control the load current with as high as possible bandwidth. In this regard, the output filter is changed to a *LCL* filter according to **Fig. 10**, to define a minimum load-side inductance and enable measurement and control of the output current. The value of the output inductor, L_s , is included in the optimization to further improve the performance.

From an initial investigation of different control structures, the three most suitable structures have been selected, which are listed below.

- 1) *Two-loop control structure ⑤*, *Fig. 10(a)*: This structure stems from [6] and is composed of an inner voltage controller, $\underline{K}_v(s)$, and an outer current (PI) controller, $\underline{K}_i(s)$,

$$\underline{K}_v(s) = \frac{sLK_{pv}}{1 + sT_{iv}}, \quad \underline{K}_i(s) = K_{pi} \left[1 + \frac{1}{sT_{ii}} \right], \quad (13)$$

that control the capacitor voltage and the output load current, respectively. The voltage controller features a differentiator in the forward path [along with a high frequency pole for physical implementation, to compensate for the integral component, $(sL)^{-1}$]. Furthermore, structure ⑤ also includes the feedforward of the reference for the control loop of the capacitor voltage, v_1^* .

- 2) *Three-loop control structures ⑥ to ⑧*, *Figs. 10(b) and (c)*: These structures are obtained by adding load-current (PI) controllers to the corresponding voltage control structures ② to ④. Furthermore, the frequency-limited load voltage (using a 2nd-order Bessel low-pass filter) is added to the output of the load-current controller to calculate the reference of the capacitor voltage, v_1^* . This feedforward enables increased control bandwidth for a wide load range.

Due to the finite FPGA clock frequency, the digitally generated PWM signal leads to quantization effects. In the considered system, these effects are of minor importance if the present operating conditions adequately utilize the converter's output

²Since the reference extrapolation block has no impact on the converter's output impedance, same impedances apply to structures ③ and ④.

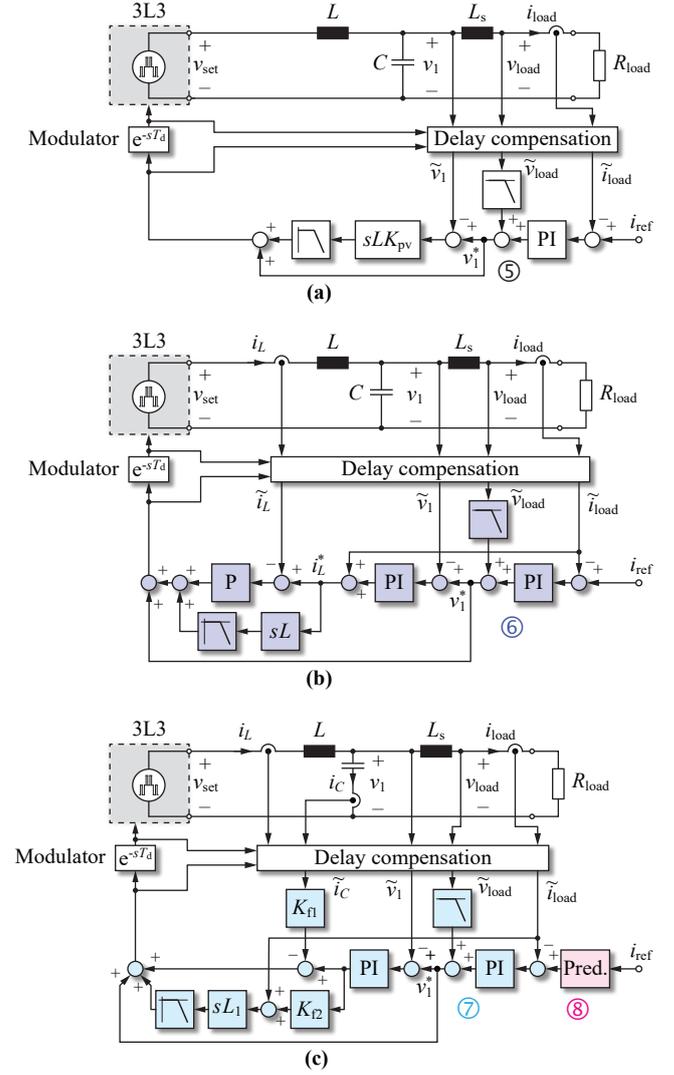


Fig. 10: Control structures selected for the current control: (a) two-loop structure ⑤ according to [6]; (b) three-loop structure ⑥ realized based on the voltage control structure ②, by adding a load-current (PI) controller; (c) three-loop structure ⑦, which is based on the capacitor current feedback structure ③. Structure ⑧ extends ⑦ by a reference current extrapolation.

voltage range. However, in case of output current control and low load resistance, i.e., $R \rightarrow 0$, the converter needs to provide a low voltage, v_{set} , to the output filter and quantization effects become more pronounced. In order to reduce the impact of these effects, the current control structures have been optimized for a reduced cell switching frequency of $f_{s'} = 250 \text{ kHz}$ ($f_{eff'} = 1.5 \text{ MHz}$), which naturally increases the PWM resolution, and the values of the filter components are increased by a factor of $f_s/f_{s'} = 3.2$.

The optimization of the current control structures is conducted in the same way as for the voltage controllers, i.e., same boundary conditions and performance metrics apply. The optimizations for the current controllers consider resistive load conditions ranging from no load ($R_{load} \rightarrow 0$) to full load ($R_{load} = 5.3 \Omega$) by analyzing the performances at the extreme load conditions. Furthermore, stable operation at an increased

load of $R_{\text{load}} = 53 \Omega$ is verified.

Fig. 11(a) presents the closed loop transfer functions corresponding to the structures depicted in Fig. 10 for $R_{\text{load}} = 5.3 \Omega$ and **Tab. III** lists key performance values. The phase is on purpose evaluated at a frequency of 60 kHz to highlight differences in the phase response of the investigated control structures. At nominal load, the structures ⑤ and ⑦ feature similar phase-lags of 40° and 39° at 60 kHz and also the small-signal bandwidths, f_{-45° , are similar, i.e., 65 kHz for ⑤ and 73 kHz for ⑦. With this, they outcompete the three-loop structure with inductor voltage feedforward ⑥ that achieves a phase-lag of 51° and $f_{-45^\circ} = 53$ kHz. Further performance improvements, i.e., a phase-lag of 33° and $f_{-45^\circ} = 89$ kHz, is possible by means of a reference extrapolation based on (12), using $T_{\text{prv}} = 200$ ns, $T_{\text{pred}} = 1$ μ s, and a series-connected 2nd-order Bessel low-pass filter with cut-off frequency of 300 kHz. According to **Fig. 11(b)**, the achieved bandwidth decreases for increasing load resistance. Verification is conducted by means of detailed simulations, e.g., as shown in **Fig. 12** for structure ⑧. Similar to output voltage control, the investigated system is subject to physical limitations, i.e., in case of large-signal excitations (output current amplitude of 60 A) and nominal load. Operation without multiple switching events during one half switching period is feasible up to $f_{m,60\text{A}} = 250$ kHz; for small-signal excitations (amplitude of 2 A), the corresponding limit is at $f_{m,2\text{A}} = 550$ kHz.

Fig. 13(a) presents the simulated output current in case of a sinusoidal reference with $f = 60$ kHz, an amplitude of 20 A, and $R_{\text{load}} = 5.3 \Omega$. The phase-lags correspond to the analytical findings and are 41° , 52° , 38° , and 34° for control structures ⑤, ⑥, ⑦, and ⑧, respectively. The responses of the output current to a trapezoidal reference current with $\Delta I_{\text{ref}} = 10$ A and $di_{\text{ref}}/dt = 2.5$ A/ μ s are shown in **Figs. 13(b) to (d)** for different load resistances, i.e., 53Ω , 5.3Ω , and short-circuit. In case of $R_{\text{load}} = 5.3 \Omega$, depicted in Fig. 13(c), the rise time (10% – 90% of the final value) decreases from 3.6 μ s in ⑥ to 3.3 μ s in ⑧, whereas the delay time (measured for 0 – 10%) remains almost the same (1.4 μ s). For ⑧, an overshoot of 17% results in case of a shorted output.

Fig. 14 depicts the calculated output impedance of the UHPS, assuming a loss-less power converter. At 60 kHz, the resulting impedances are $15 \Omega e^{-j-109.4^\circ}$, $11 \Omega e^{-j-93^\circ}$, and $30 \Omega e^{-j112^\circ}$ for control structures ⑤, ⑥, and ⑦, respectively.

IV. CONCLUSIONS

This paper investigates the dynamic performance of a high bandwidth phase-modular three-phase 10 kW/230 V_{rms} (per phase) AC power source and evaluates different measures to

TABLE III: Performance values achieved for output current control.

Structure	$R_{\text{load}} = 5.3 \Omega$		$R_{\text{load}} = 53 \Omega$	
	$\varphi_{60\text{ kHz}}$	f_{-45°	$\varphi_{60\text{ kHz}}$	f_{-45°
⑤	-40°	65 kHz	-113°	24 kHz
⑥	-51°	53 kHz	-105°	18 kHz
⑦	-39°	73 kHz	-92°	17 kHz
⑧	-33°	89 kHz	-87°	17 kHz

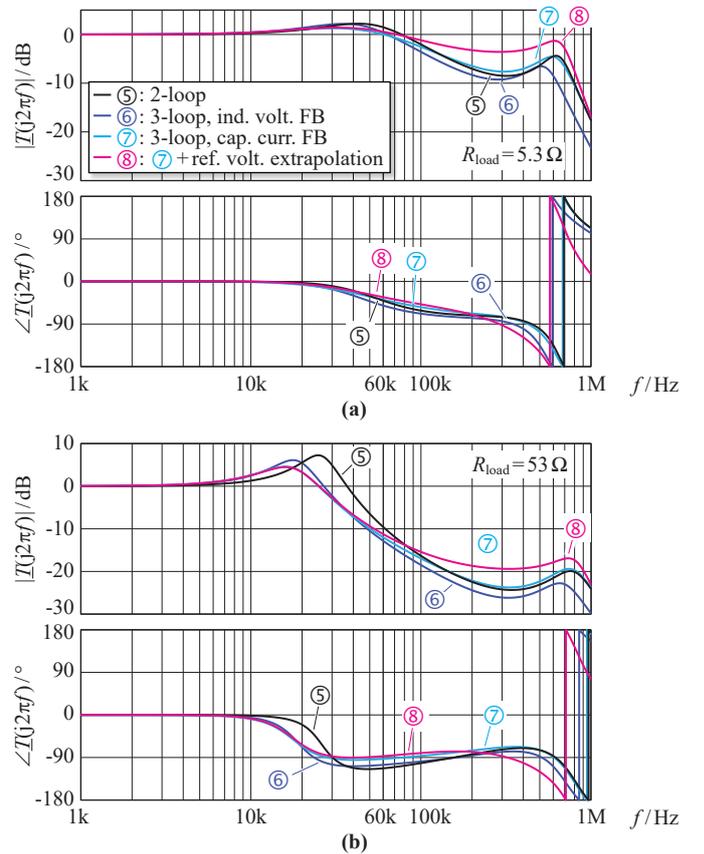


Fig. 11: Calculated reference transfer functions, $\underline{T}(s)$ for control structures ⑤ to ⑧, cf. Fig. 10, and different loads: (a) $R_{\text{load}} = 5.3 \Omega$, (b) $R_{\text{load}} = 53 \Omega$.

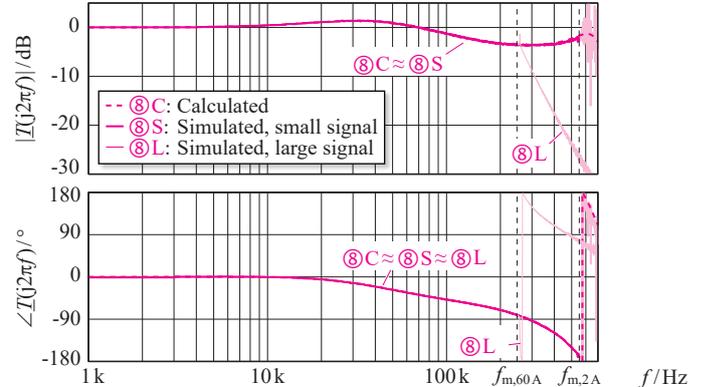


Fig. 12: Calculated and simulated transfer functions for $R_{\text{load}} = 5.3 \Omega$ and control structure ⑧. The simulation is conducted for two different amplitudes, i.e., 60 A (large-signal) and 2 A (small-signal); $f_{m,60\text{A}}$ and $f_{m,2\text{A}}$ denote the frequency boundaries above which a low distortion of the output current is only maintained if multiple switching events during half a switching period are allowed.

increase the achievable control bandwidth by applying specific extensions to a two-loop cascaded control structure. Based on the results of a comprehensive comparative evaluation it is found that the control structures with capacitor current feedback, inductor voltage feedforward, and reference prediction achieve best performance values for the control of both, output voltage and output current.

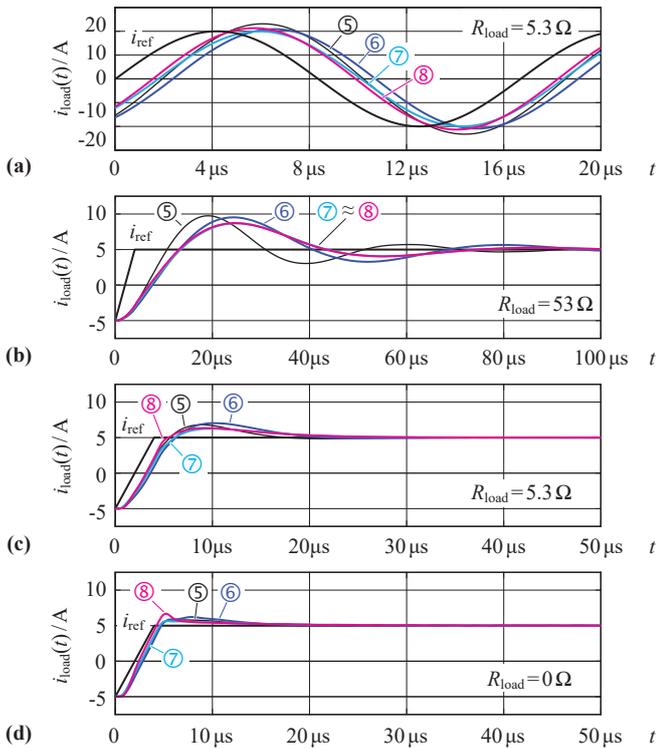


Fig. 13: (a) Simulated time-domain response of the converter for sinusoidal reference (60 kHz, 20 A) and nominal load resistance; (b), (c), and (d) Simulated time-domain responses for trapezoidal reference (± 5 A) at (b) $R_{load} = 53 \Omega$, (c) $R_{load} = 5.3 \Omega$, and (d) $R_{load} = 0$.

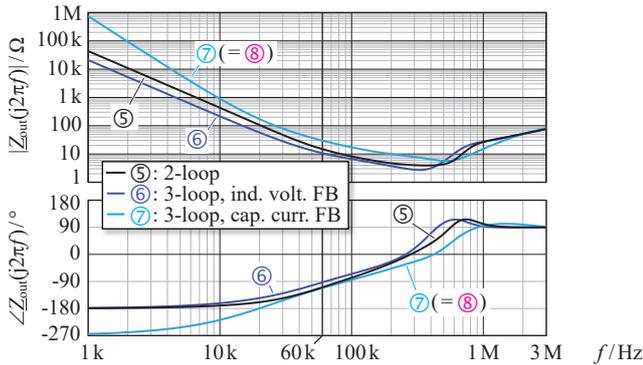


Fig. 14: Output impedance of the converter for output current control.

With regard to output voltage control, large-signal operation (phase voltage amplitude of 325 V) with a small phase-lag of 7° at an output frequency of 100 kHz and a small-signal bandwidth of 427 kHz are achievable under operation with full load. Furthermore, a very low output impedance can be ensured over a large frequency range, e.g., 143 m Ω at 100 kHz. In case of output current control, the phase-lag can be reduced to 33° at large-signal operation with 60 kHz, an output current amplitude of 60 A, and nominal load resistance. The respective small-signal bandwidth for output current control is 89 kHz and the output impedance at 60 kHz is 30 Ω .

The calculated results are verified by means of circuit simulations, using a detailed simulation model that incorporates a complete model of the power stage and also considers the

discrete-time nature of the digital control unit. The experimental verification of the obtained findings will be conducted in an immediate next step, using a hardware prototype of the UHPS that is currently being finalized.

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