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***Abstract*— Power amplifiers providing an output current of high precision, high bandwidth and low distortion are required in different fields like magnetic resonance imaging or motion control systems for semiconductor production processes. This paper analyzes different power stage implementations of switched-mode (Class-D) amplifiers intended for such applications. They are preferred to linear or hybrid solutions as they feature a high output power with a good efficiency at low cost and low complexity. The advent of wide bandgap (WBG) semiconductors based on gallium nitride (GaN) or silicon carbide (SiC) enables Class-D amplifiers with unprecedented performance regarding distortion and bandwidth. Comprehensive circuit simulations incorporating detailed switch- and thermal models of all relevant components are used to compare different implementations of Class-D switching stages based on GaN and SiC semiconductors with respect to output voltage distortion. The systems' sensitivities to various parameters such as power circuit topology or output current amplitude are derived as a performance measure. It is shown that the thermal behavior of the power devices has significant influence on the output distortion and that the dual buck topology, which requires no dead time in between the turn-off and the turn-on of the bridge leg transistors, is less sensitive to parameter variations and has a better distortion performance than the conventional half bridge topology.**

I. Introduction

Amplifiers capable of providing output currents with a high signal to noise ratio (SNR), low harmonic distortion and a high bandwidth are used in different industries. In MRI applications, fast changing currents of high amplitude are required to form the gradient fields. The image quality can be improved by increasing the amplifier's bandwidth as well as its output current quality, leading to faster acquired and less distorted images [1, ch. 11].

In integrated circuit manufacturing, mechanical motion systems, as illustrated in **Fig. 1**, are used for positioning semiconductor wafers in applications like exposure, dicing, inspection or other handling tasks. These systems operate in the nanometer range and incorporate different single- or three-phase electromechanical actuators like voice coils, permanent magnet linear motors or planar magnetic bearings, which have different power ratings (into the kVA range) and different operational profiles (like transient or stationary loading) [2, ch. 5].

As semiconductor structures on the wafers become ever smaller and more complex, it is estimated that the SNR of the amplifiers' outputs needs to increase by $\approx 20\,\mathrm{dB}$ every five years in order to be able to keep track with the industry's requirements [3]. Furthermore, larger $450\,\mathrm{mm}$ diameter wafers will eventually be introduced and the amplifiers must, apart from providing a high output quality, also increase their output power and bandwidth in order to maintain throughput with the larger and heavier handling systems.

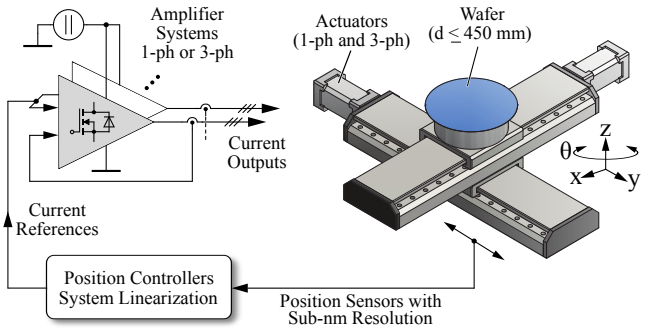

Fig. 1: Wafer positioning system. Different kinds of actuators such as voice coils (1-phase) or permanent magnet motors (3-phase) are driven by precision amplifiers which must provide a high current quality to avoid undesired mechanical movement and to achieve high control dynamics to ensure fast wafer positioning and/or high productivity.

These motion systems use low-friction air- or magnetic bearings and consequently, torques or forces from the actuators easily translate to mechanical movement. This requires amplifiers that provide output currents with a very high SNR ($> 100\,\mathrm{dB}$) in order to avoid unwanted actuator force generation. Furthermore, the electromechanical systems show various nonlinearities such as position sensor gain errors or actuator force ripple. In order to improve the overlaying position control system's performance, feedforward control is extensively used which benefits from linear amplifier transfer characteristics [4]. It is also desired to keep the weight and rigidity of actuator drive cables low as their movement introduces disturbances to the moving system which are difficult to model and compensate for. Consequently, higher voltage actuators are preferred and thus, the amplifier must be capable of providing output voltages in excess of several hundred volts.

Switched-mode (Class-D) or hybrid amplifiers are widely used for driving actuators in wafer processing systems [5], [2]. Class-D solutions can provide high output power, high efficiency, low complexity and low cost. However, due to their switching nature and nonlinear effects of individual system components and functional elements (e.g., transistors or inductors), the distortion content and linearity of the output signal must be carefully considered. A generalized overview of such an amplifier and its most important sources of distortion is illustrated in **Fig. 2**.

Due to the presence of different nonlinear effects causing distortions of the switched-mode amplifier's output, analytical analyses are often constrained to specific operating points or simplified models [6]–[10]. Therefore, a simulation model and its results are presented in this work which allows to

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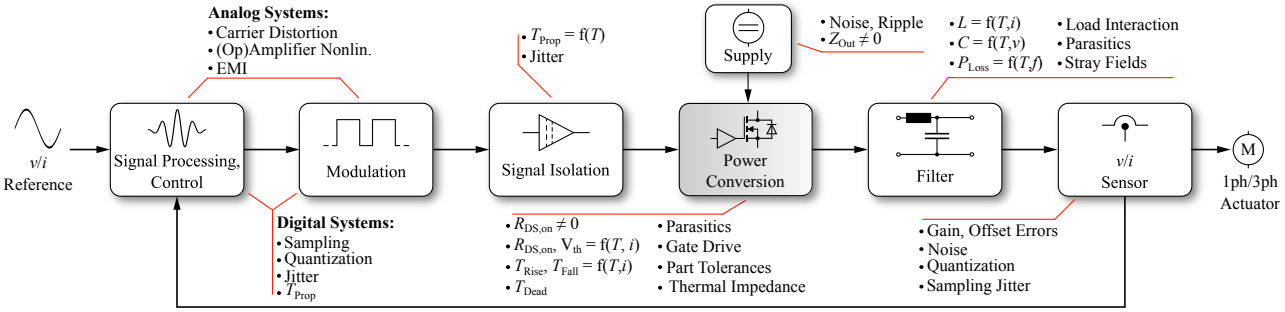

Fig. 2: Sources of output distortion in a generalized switch-mode amplifier system featuring a feedback loop. Many component properties vary with the operating point and signal time behavior (e.g., temperature or output current) of the system, rendering it nonlinear. The control and modulation blocks can be implemented using analog, digital or mixed circuitry.

determine influences of different system components on the amplifier's output voltage quality individually. Only a circuit simulation allows an isolated analysis of the distortion impact of a specific system component as all other components can be modeled as being ideal. Furthermore, it also allows a direct comparison of different design parameters such as switch technology, circuit topology, cooling system or operating point. As the switching stage provides the amplifier's gain and is a main source of distortion, it is the only element considered nonideal in this first analysis step. All other system components like the power supply, the output filter or the modulator are assumed ideal.

Amplifier output distortion components with frequencies in the mechanical system's sensitive frequency range (from DC up to $\approx 10\,\mathrm{kHz}$), especially at frequencies where the position controller provides limited gain, require careful attention as they lead to disturbing mechanical forces and hence, movement in the actuators. Above a certain frequency, the distortion components at the amplifier's output are of insignificance as they are sufficiently attenuated by the mechanical system's inertia and damping.

Amplifiers for mechatronic actuators usually control their output current as it directly produces the force or torque in the actuators. According to the load impedance, any voltage distortion on the amplifier's output will also be reflected in the current. Therefore, this work investigates in a first step the output voltage quality of different switched-mode amplifier concepts where no feedback loop is considered in order to characterize the actual power stage performance.

There are different methods of characterizing the performance of an amplifier that provides an output voltage with amplitude $v(t)$. Apart from the signal to noise ratio,

$$\mathrm{SNR} = 20\log_{10}\frac{v_{1,\mathrm{RMS}}^2}{v_{\mathrm{N,RMS}}^2}, \tag{1}$$

the total harmonic distortion (THD) is also a commonly used performance measure:

$$\mathrm{THD} = 20\log_{10}\frac{\sqrt{v_2^2+v_3^2+\cdots+v_k^2}}{v_1}. \tag{2}$$

Here, v_1 is the amplitude of the signal component with frequency f_1 and $v_{1,\mathrm{RMS}}$ its RMS value. Consequently, v_k is the amplitude of the k-th harmonic component with $f_k = kf_1$. The SNR figure in eq. (1) is similar to the THD, but it relates the signal power to the noise power whereas the signal- and noise RMS voltages are measured across the same impedance and harmonics are excluded from the noise power [11]. In order to capture all distortion components including noise, harmonics or intermodulation products, the total harmonic distortion plus noise (THD+N) or signal to noise and distortion ratio (SINAD) can be used, for which the power of all unwanted signal components is related to the fundamental signal's power [11]. As this work deals with computer simulations, there is no wideband noise of random nature in the signals but only harmonics created by nonlinearities. Consequently, the THD is used as a performance measure. Amplifiers providing a voltage output with low distortion are commonplace in the audio industry and can reach THD levels of $\approx -100\,\mathrm{dB}$ [12].

In this paper, output voltage distortion results of circuit simulations of the amplifier switching stages are presented with the goal of identifying concepts which are most suitable for an amplifier system capable of driving single- or three-phase loads with extremely low distortion. Different topologies and new switch technologies such as GaN and SiC are modeled and simulated in detail together with their cooling concepts. By decoupling the distorting effects from the electrical and thermal systems, the simulations can be significantly accelerated which allows an efficient analysis of many different circuits and operating points. The results finally show that the dual buck topologies deliver a better distortion performance and are less sensitive to parameter changes. Furthermore, GaN transistors are superior to SiC switches for such low-distortion applications in the lower kW range as they exhibit faster switching and less parasitics.

First, in **Section II**, the simulation approach and models of the switching stage are outlined. In **Section III**, the simulation results are presented and interpreted. Finally, a conclusion and outlook are given in **Section IV**.

II. Simulation Setup

The circuit simulation as pursued in this work as well as the different semiconductor topologies, the switch models and the corresponding thermal models are explained in this section.

A. Simulation Approach

The setup of the simulation is illustrated in **Fig. 3**. In a first step, only the switching stage of the amplifier, which consists of the power semiconductor devices as well as their gate drivers, is investigated. All other functional blocks such as

the power supply are assumed ideal. The parameters defining the simulated model can essentially be divided into operating parameters of the amplifier itself and circuit parameters which are used to describe the switching stage.

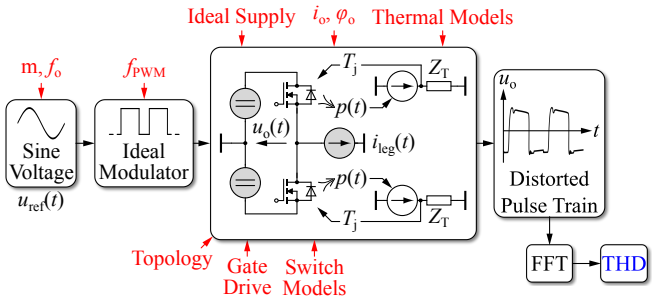

Fig. 3: Simulation setup for the distortion analysis of the switching stage. Different circuit topologies, switch technologies and thermal systems are modeled such that the main nonlinearities are well accounted for. All functional blocks except the switching stage are assumed ideal.

Operating parameters are common in any amplifier implementation; the bridge leg output current has a certain amplitude i_o and its phase φ_o (relative to the fundamental output voltage's phase) can be shifted: $i_{leg}(t) = i_o \sin(2\pi f_o t + \varphi_o)$. The reference input voltage amplitude is represented with the modulation index m: $u_{ref}(t) = m \sin(2\pi f_o t + \varphi_o)$. In the case of this work, the input voltage and output current are both sinusoidal and have the same frequency, f_o. A current ripple is not considered as the output filter is also assumed ideal. In order to reduce the wideband quantization noise which originates from the nonzero simulation time step, a noise shaping modulator is used [13].

The spectrum of the output voltage $u_o(t)$ of the switching stage is calculated numerically using the FFT. In order to accurately represent the low-level amplitudes of the harmonics, an FFT window with a sufficiently high dynamic range[1] is used (high side lobe attenuation) [14]. This requires the simulation of several fundamental output periods due to the window's spectral leakage. From the resulting spectrum, the THD is calculated up to an arbitrarily defined harmonic (k=4 in eq. 2) and not up to a certain frequency while also making sure that no switching frequency components or its sidebands are interfering with the signal harmonics. This is done in order to be able to compare different operating modes, especially with regards to varying output frequencies f_o.

An alternative simulation approach, which does not require the simulation of several fundamental periods, is described in [15]. That method evaluates the amplifier's average output voltage as a function of e.g. the modulation index m and derives the amplifier's respective transfer function, which can then be used to estimate the THD. However, that method offers no option to include thermal models. Consequently, the simulation approach as described above is used in this work as the thermal effects are of great importance which will be revealed by the results in section III.

In the following, the analyzed topologies and switch models of the switching stage are presented.

[1]Kaiser window; $\beta = 38$

B. Considered Converter Topologies

Two main circuit topologies and different derivations are analyzed. First, there is the conventional half-bridge (HB) topology illustrated in **Fig. 4** (a) which requires a dead time T_D to prevent bridge leg shoot-through (simultaneous turn-on of both bridge leg transistors) and is thus expected to provide a limited performance regarding output distortion [8]. In order to avoid the large voltage drops of the WBG devices when operated in reverse conduction mode (which, in the case of GaN transistors, can easily exceed ≈5 V [16]), small SiC free-wheeling diodes are connected in parallel to the power transistors which have a lower voltage drop and only conduct the current during the dead time interval. The half-bridge is operated using pulse width modulation (PWM) as shown in **Fig. 4** (b). Multiple half-bridge legs can be interleaved in order to reduce the current loading of each half-bridge and to increase the effective switching frequency which increases the output dynamics [17]. This topology is illustrated in **Fig. 4** (c) and (d) for two interleaved stages (HB_{2xIL}).

The second topology, denoted as dual buck (DB) topology, requires no dead time and is depicted in **Fig. 4** (e) [7], [3]. One possible operating mode of the switches is illustrated in **Fig. 4** (f). Note that the two switching legs are operated in an interleaving fashion. As with the HB topology, this circuit can also be interleaved [18].

With respect to a fundamental output period, the currents in the DB topology are controlled as shown in **Fig. 4** (g). The offset current I_{Off} is an important circuit parameter as it significantly influences the distortion performance. The leg currents are determined as follows:

$$i_{L1,L2}(t) = \frac{i_o(t)}{2} \pm I_{Bias} \tag{3}$$

$$I_{Bias} = \frac{\hat{i}_o}{2} + I_{Off}. \tag{4}$$

Consequently, it holds that: $i_{L1} + i_{L2} = i_L = i_o$.

In this analysis, which assumes and implements ideal behavior of the functional blocks apart from the switching stage, the control of the leg currents ($i_{L1,L2}$ is not considered and hence the currents are assumed to perfectly track the theoretical sinusoidal reference. This ideal current behavior is also assumed in the HB_{2xIL} topology where the currents must be split between the individual half-bridge legs such that $i_o = i_{L1} + i_{L2}$.

The switching leg of the DB topology (**Fig. 4** (e)) is asymmetric, featuring a transistor and a diode in the main current paths. As mentioned in [3], this leads to distortion as the device's resistances and thermal behavior are not identical and consequently, different current-dependent voltage drops occur. In order to symmetrize the DB topology, two derived circuitries are considered. The first provides synchronous rectification switches in parallel to the diodes D_1 and D_2 (**Fig. 4** (h); (DB_{SR})). Note that this topology is identical to the HB_{2xIL} topology (**Fig. 4** (c)) and dead time is required. However, the currents are controlled in the same manner as in the DB topology (**Fig. 4** (g)). As in the HB topology, small freewheeling diodes are also used to reduce the WBG transistor's reverse conduction voltage drops during the dead time intervals. The other circuitry inserts additional diodes $D_{S1,S2}$ and permanently turned-on transistors ($S_{1,2,ON}$) in the main conduction paths as shown in **Fig. 4** (i) in order to

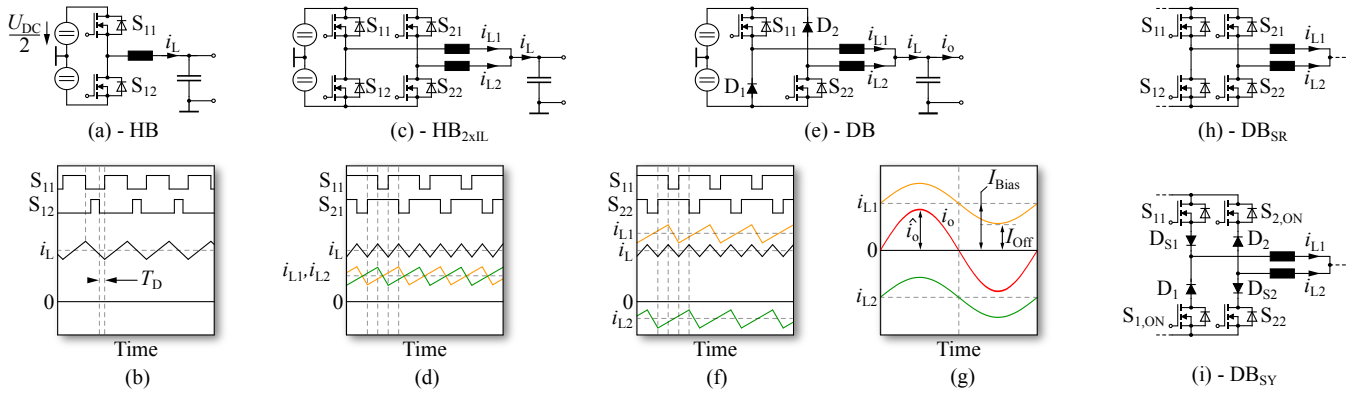

Fig. 4: Topologies considered for the amplifier system. (a),(b): Conventional half-bridge operated with PWM. (c),(d): Interleaved half-bridge topology with phase-shifted PWM carriers. (e): Dual buck (DB) topology which requires no dead time at switching state changes of a bridge leg. (f),(g): Typical operating waveforms for the DB topology for some switching periods and one fundamental period. (h): In order to symmetrize the DB topology, switches for synchronous rectification can be employed in parallel to the diodes of the DB topology in (e). (i): Another symmetrization approach: Diodes $\mathrm{D_{S1}}$, $\mathrm{D_{S2}}$ and permanently turned on transistors $\mathrm{S_{1,ON}}$, $\mathrm{S_{2,ON}}$.

symmetrize the switching legs ($\mathrm{DB_{SY}}$). This leads to higher losses, but the voltage drops are now identical in the upper- and lower side of the switching legs.

C. Switch Model

High switching speeds are desired for this application in order to reduce distortions originating from the finite rise- and fall-times of the switching stage output voltage. Therefore, fast-switching SiC and GaN transistors are evaluated in the course of this analysis. WBG material is also considered for the power diodes (i.e., in the DB topologies) as such devices also show fast switching behavior due to the lack of reverse recovery charges and the presence of only relatively small junction capacitances.

The models for these switching devices are considering the electrical and thermal effects in detail in order to accurately match their real behavior. All model parameters are either derived from manufacturer's datasheets or based on simple FEM simulations, as explained below.

1) Electrical Models: The circuits used to implement the transistor and diode models are illustrated in **Fig. 5** [19]. An evaluation of different WBG transistor datasheet shows that it is sufficient to model the dependencies of the device's parameters as follows:

$$
\begin{aligned}
v_{\mathrm{Th}},\, g_{\mathrm{m}} &= \mathrm{f}(T_{\mathrm{j}}) \Rightarrow i_{\mathrm{g_m,ON}}(t) = (v_{\mathrm{GS}}(t) - v_{\mathrm{Th}}) g_{\mathrm{m}} \\
V_{\mathrm{D_{gm}}},\, R_{\mathrm{D_{gm}}} &= \mathrm{f}(v_{\mathrm{GS}}, v_{\mathrm{Th}}) \\
R_{\mathrm{DS,on}} &= \mathrm{f}(T_{\mathrm{j}}, i_{\mathrm{DS}}) \\
C_{\mathrm{DS}},\, C_{\mathrm{GD}} &= \mathrm{f}(v_{\mathrm{DS}}) \\
R_{\mathrm{D}}, v_{\mathrm{D}} &= \mathrm{f}(T_{\mathrm{j}}) \\
C_{\mathrm{D}} &= \mathrm{f}(v_{\mathrm{CA}}).
\end{aligned}
$$

These parameters and dependencies can be extracted from manufacturer's datasheet specifications and implemented in the simulation software [20].

In order to take differences between switch technologies into account, the transistor model is adjusted accordingly. The diode $\mathrm{D_{gm}}$ is the freewheeling diode of the controlled current source $\mathrm{g_m}$. If the transistor is turned on ($v_{\mathrm{GS}} > v_{\mathrm{Th}}$), its forward voltage $V_{\mathrm{D_{gm}}}$ and drift resistance $R_{\mathrm{D_{gm}}}$ are set to zero such that it can conduct the excess current from $\mathrm{g_m}$ without

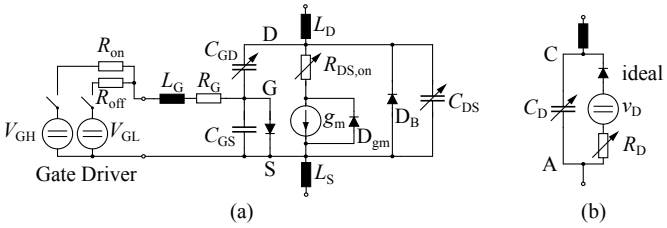

Fig. 5: (a): Electrical transistor and (b): diode model used for the simulations. All parameters are derivable from datasheet specifications.

influencing the rest of the circuit. The behavior of this diode in the transistor cutoff case ($v_{\mathrm{GS}} < v_{\mathrm{Th}}$) is different in SiC and GaN devices. As SiC devices have a body diode $\mathrm{D_B}$ which conducts during reverse operation, $V_{\mathrm{D_{gm}}}$ and $R_{\mathrm{D_{gm}}}$ are set to high values in order to prevent this diode from conducting. However, in GaN devices, the body diode $\mathrm{D_B}$ is absent and the parameters of $\mathrm{D_{gm}}$ are adapted during cutoff in order to account for their reverse conduction behavior. GaN transistors turn their channel on in the reverse conduction case [16] and consequently, the reverse current flows through $R_{\mathrm{DS,on}}$. This can be achieved by setting $R_{\mathrm{D_{gm}}}$ to zero in order to enable a current path from source to drain through $R_{\mathrm{DS,on}}$. Additionally, the reverse voltage drop of GaN transistors is a strong function of the gate voltage v_{GS} and can be accounted for by adjusting $V_{\mathrm{D_{gm}}}$ accordingly. Finally, the diode between gate and source is only present in some GaN devices [21].

As the simulation results will show, the gate driver's properties can significantly influence the resulting output distortion. This is expected as the driver directly determines the transistor's switching behavior. In order to consider this effect, the gate driver is modeled using different gate voltages ($V_{\mathrm{GH,L}}$) and resistors ($R_{\mathrm{On,Off}}$) for turn-on and turn off respectively as illustrated in **Fig. 5** (a).

As the junction temperature T_{j} influences many parameters, a thermal model is included in the simulations which allows an accurate determination of T_{j} for both transistors and diodes. It is presented in the following section.

2) Thermal Model: The thermal system is comprehensively modeled and takes the cooling approaches of different switch

packages into account.

Fig. 6 (a)-(c) illustrates three different cooling solutions. Some PCB-mounted devices require a cooling path through the PCB itself using thermal vias (**Fig. 6** (a)) [22]. However, some SMD devices offer a path of lower thermal resistance when directly cooled at the case (**Fig. 6** (b) [16]). And finally, through-hole devices are usually mounted directly on a heat sink with an electrically isolating heat pad (**Fig. 6** (c)).

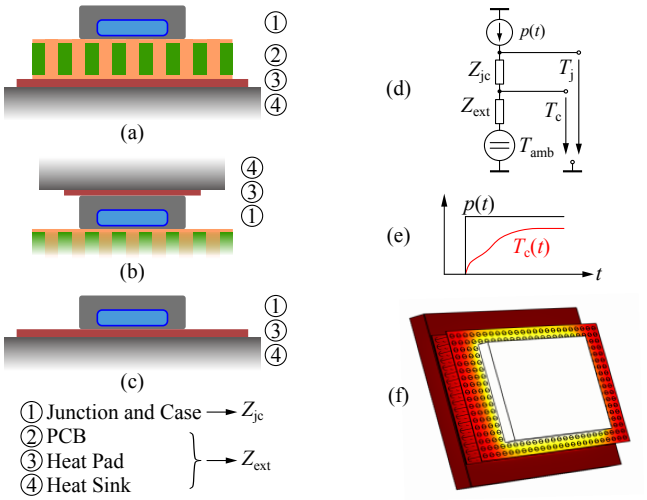

Fig. 6: Different switch cooling approaches and thermal modeling process. (a) and (f): Surface-mounted device cooled through the PCB or (b): directly at its case. (c): Through-hole device mounted on a heat sink. (d): Equivalent circuit for the thermal models. Z_{jc} is available from datasheets whereas Z_{ext} is extracted from the system's thermal step response (e) which is obtained using transient FEM simulations (f).

The thermal model which is implemented for each switching device is illustrated in **Fig. 6** (d). It consists of the thermal impedance Z_{jc} from junction to case and an impedance Z_{ext} from the case to ambient. From manufacturer's datasheets, a thermal step response plot of Z_{jc} is usually available. Using system identification techniques, the transfer function model of Z_{jc} can be identified and directly implemented in the simulation software [23], [20]. However, for the impedance Z_{ext} from case to ambient, such transient data is not available. Consequently, models of the thermal systems are identified from thermal step responses which are obtained from FEM simulations (**Fig. 6** (e) and (f)). This is done for the three different cooling solutions as illustrated in **Fig. 6** (a)-(c).

In order to avoid harmonic distortion due to circuit asymmetry (unevenly heated switching devices) and temperature dependent voltage drops, it is important that the temperature differences between the devices vary as little as possible over a fundamental output period. Consequently, the thermal impedances between the devices and the heat sink must be kept as low as possible. This can be achieved by using the appropriate cooling solution for each device as illustrated in **Fig. 6** (a)-(c). As for the heat sink, it is modeled as an ideally conductive plate being at a constant temperature T_{amb}. This models a water cooled heat sink which keeps T_{j} low and thus helps achieving low distortion since many WBG transistors show a near quadratic dependency of the $R_{\mathrm{DS,on}}$ on the junction temperature and are thus best operated at low temperatures.

Conduction- and switching losses of the power semiconductors are, in the case of conduction losses, directly evaluated in the simulation model. The current-, voltage- and frequency-dependent switching losses are either extracted from manufacturer's datasheets (where available), from publications or they have been estimated using detailed manufacturer's SPICE models [24], [25], [26]. The momentary losses of each device are fed into their thermal models in each simulation time step and the resulting junction temperature is used to vary the switching device's parameters accordingly (cf. **Fig. 3**).

As the fundamental output frequency f_{o} is less than 50 Hz, a simulation encompassing several periods of f_{o} is unfeasible as it would take a long time to evaluate and would also create a large amount of data as the simulation time step must be kept comparably small ($\approx$300 ps) in order to correctly represent fast switching transitions and to reduce the time-quantization noise. However, this problem can be circumvented due to the fact that the distortion effects of the electrical- and thermal model can be decoupled; simulation results show that, if thermal effects are neglected (T_{j} = const.), the resulting distortions are independent of f_{o}, as long as $f_{\mathrm{PWM}} >> f_{\mathrm{o}}$ such that the harmonics introduced by the PWM modulator are of no concern. This allows to shift all thermal transfer functions G_{T} (5) in frequency and one obtains $G_{\mathrm{T,shift}}$ as shown in (6). The method is also shown graphically in **Fig. 7** on an exemplarily thermal transfer function's magnitude.

$$G_{\mathrm{T}}(s) = \frac{a_0 + a_1 s + \cdots + a_n s^n}{b_0 + b_1 s + \cdots + b_n s^n} \tag{5}$$

$$G_{\mathrm{T,shift}}(s) = \frac{a_0 + (\frac{f_{\mathrm{T}}}{f_{\mathrm{o}}}) a_1 s + \cdots + (\frac{f_{\mathrm{T}}}{f_{\mathrm{o}}})^n a_n s^n}{b_0 + (\frac{f_{\mathrm{T}}}{f_{\mathrm{o}}}) b_1 s + \cdots + (\frac{f_{\mathrm{T}}}{f_{\mathrm{o}}})^n b_n s^n}. \tag{6}$$

Now, $G_{\mathrm{T,shift}}$ can be used in a simulation with $f_{\mathrm{o}} > f_{\mathrm{T}}$ and the behavior of the thermal system is identical to a simulation where G_{T} is used with $f_{\mathrm{o}} = f_{\mathrm{T}}$. Advantageously, f_{o} can now be chosen to be in the kilohertz-range, which significantly accelerates the simulation process, while f_{T} determines the desired fundamental frequency for the thermal behavior, which is e.g., 50 Hz. This method also allows to account some fundamental periods for the thermal system to reach its steady-state.

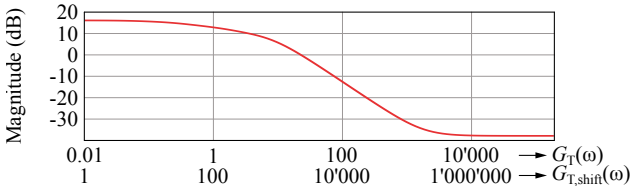

Fig. 7: Magnitude plot of an exemplary thermal transfer function and the effect of the frequency shift. $f_{\mathrm{o}} = 100 f_{\mathrm{T}}$

Tab. I lists data of different transistors and diodes together with their cooling solution as they are used in the simulations. Switches with different characteristics (i.e. capacitances or thermal properties) have been selected in order to cover a broad field of properties.

III. Simulation Results

This section presents the simulation results of the topologies and semiconductors introduced previously. Sensitivity analyses have been performed which reveal how strongly

Trans.	Ref.	V_{BD}	$R_{DS,on}$ 25°C	$I_{DS,Max}$ 25°C	Cooling (**Fig. 6**)
GaN	GaN_{T1}	650 V	55 mΩ	30 A	PCB (a)
GaN	GaN_{T2}	600 V	56 mΩ	≈20 A	PCB (a)
GaN	GaN_{T3}	200 V	25 mΩ	22 A	Top (b)
SiC	SiC_{T1}	1200 V	80 mΩ	36 A	Heat sink (c)
SiC	SiC_{T2}	1200 V	25 mΩ	90 A	Heat sink (c)
Diode	Ref.	V_{BD}	Q_j 3-300V	I_{Max} 125°C	Cooling (**Fig. 6**)
SiC	SiC_{D1}	650 V	17 nC	10 A	PCB (a)
SiC	SiC_{D2}	650 V	35 nC	20 A	Heat sink (c)
SiC	SiC_{D3}	1200 V	37 nC	15 A	Heat sink (c)

TABLE I: Different WBG transistors and diodes used in the simulations. The „Ref." fields are used to label the figures in section III

the system's output THD reacts to variations of different parameters. The sensitivity is defined as the partial derivative of the converter's THD with respect to a single parameter x (e.g., modulation index or dead time) at a given nominal operating point X_0:

$$S(x)\big|_{X_0} = \frac{\partial\,\mathrm{THD}}{\partial x}\bigg|_{X_0}. \tag{7}$$

In order to determine S, all model parameters are kept at their nominal value whereas the parameter being analyzed (x) is swept over a certain range and the resulting THD is plotted against it.

The THD is evaluated using (2) with $k = 4$ and the thermal models are considered as explained in section II-C2. T_{Step} was always chosen such that the (time-) quantization did not affect the outcome of the simulation ($T_{Step} < 300\,\mathrm{ps}$). The ambient temperature T_{amb} is set to 40 °C in all simulations. Furthermore, the data as illustrated in the following plots is slightly interpolated using splines. Refer to table I for the abbreviation of the devices and to **Fig. 4** for the topology designations.

In the following, selected sensitivity plots are presented which allows a comparison of different systems and a performance evaluation.

A. Gate Driver Parameter Selection

As the gate driver directly influences the transistor's switching behavior, sensitivity analyses of its parameters ($V_{GH}, V_{GL}, R_{on}, R_{off}$, cf. **Fig. 5**) are performed. **Fig. 8** shows the results for the GaN_{T1} transistor in both the HB and DB topology.

The HB topology shows higher sensitivities to the gate driver's parameters, especially R_{on} is of significance.

In all simulations that have been performed, the gate driver's parameters were chosen with the help of such a sensitivity analysis in order to find a configuration which is both stable in all operating points (e.g., no parasitic switch turn-on/off at bridge output voltage transitions with a high $\mathrm{d}u/\mathrm{d}t$) and results in low distortion.

B. Topology Comparison

In **Fig. 9**, the different topologies are analyzed with sweeps over the modulation index m and the output current i_o using the GaN_{T1} transistor. Additionally, the results from an ideal HB topology (i.e., ideal switches, no parasitics) are plotted.

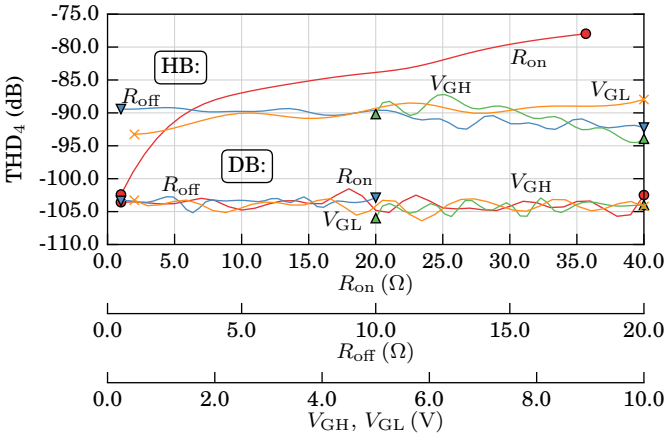

Fig. 8: Sensitivities to the gate driver's parameters for the DB and HB topology with GaN_{T1} and SiC_{D1} as switch and diode. $f_{PWM} = 100\,\mathrm{kHz}$, $f_T = 50\,\mathrm{Hz}$, $f_o = 2\,\mathrm{kHz}$, $m = 0.75$, $i_o = 3\,\mathrm{A}$, $\varphi_o = 0°$, $T_D = 15\,\mathrm{ns}$, $I_{Off} = 5\,\mathrm{A}$, $U_{DC} = 400\,\mathrm{V}$. The nominal parameters are: $R_{on,nom} = 5\,\Omega$, $R_{off,nom} = 2\,\Omega$, $U_{GH,nom} = U_{GL,nom} = 7\,\mathrm{V}$.

This ideal HB topology performs worse if it has some dead time than the topology with the realistic transistor model and circuitry. This is due to the output capacitance of the transistors which improve the distortion in topologies that require some dead time [27]. The ideal HB with no dead time ($T_D = 0$) reveals the lower THD boundary due to the nonzero simulation time step of $T_{Step} = 233\,\mathrm{ps}$ that was chosen in this simulation.

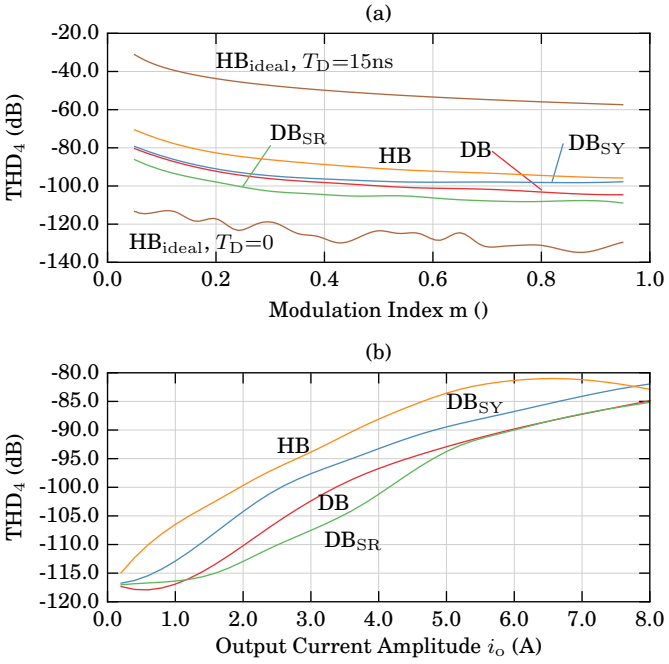

Fig. 9: Comparison of different circuit topologies with the GaN_{T1} switch and the SiC_{D1} diode. THD as a function of (a): the modulation index m and (b): the output current amplitude i_o. $f_{PWM} = 100\,\mathrm{kHz}$, $f_T = 50\,\mathrm{Hz}$, $f_o = 2\,\mathrm{kHz}$, $m_{nom} = 0.75$, $i_{o,nom} = 3\,\mathrm{A}$, $\varphi_o = 0°$, $T_{D,HB} = 15\,\mathrm{ns}$, $T_{D,DB_{SR}} = 15\,\mathrm{ns}$, $I_{Off} = 5\,\mathrm{A}$, $U_{DC} = 400\,\mathrm{V}$.

This analysis reveals that the dual buck topologies show less output distortion than the HB topology with $T_D = 15\,\mathrm{ns}$. A further reduction of dead time, which would reduce the

THD, is considered difficult in a real system in order to safely prevent cross-conduction, even with fast-switching transistors. On the other hand, in the dual buck topologies, the offset current can be increased up to a certain degree, which can be used to reduce distortion components as will be shown in section III-E.

For the DB topologies which employ a diode in the power path (i.e., the DB and $\mathrm{DB_{SY}}$ topologies), the THD is better when the diode $\mathrm{SiC_{D1}}$ is used instead of $\mathrm{SiC_{D2}}$ or $\mathrm{SiC_{D3}}$ as this diode has a smaller junction capacitance but higher conduction losses compared to the other two. This enables fast switching transitions at the cost of higher temperature swings, which nonetheless results in a lower THD in the considered operating ranges.

The synchronously rectified DB topology ($\mathrm{DB_{SR}}$) requires some dead time, too. Simulations show that there is little sensitivity of the output THD to this dead time. This is due to the use of SiC freewheeling diodes and the fact that the leg current always flows in the same direction in the DB topologies which defines the commutation behavior, rendering it less sensitive to the output current's amplitude and phase.

C. Transistor Comparison

The THD performance of the different switches is illustrated with the $\mathrm{DB_{SR}}$ topology in **Fig. 10**.

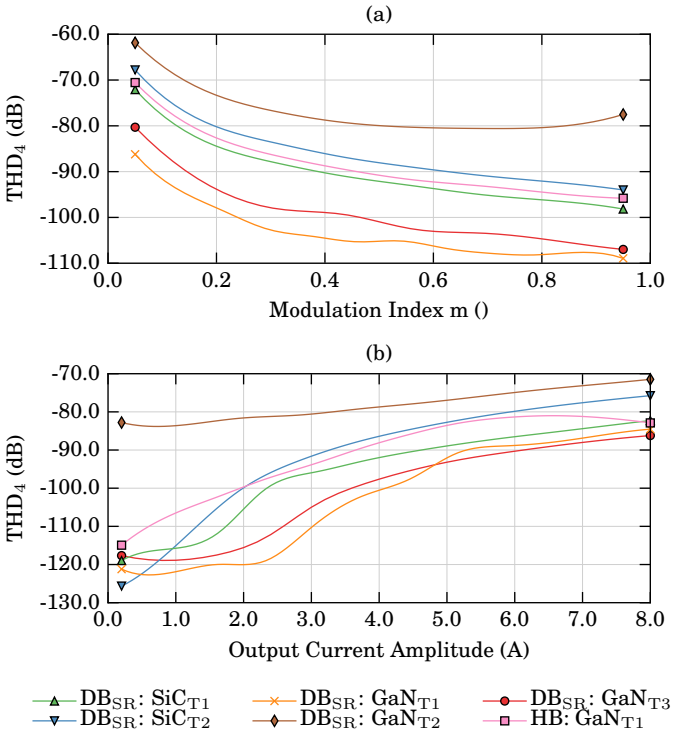

Fig. 10: Comparison of different switch technologies. THD as a function of (a): the modulation index m and (b): the output current amplitude i_o. $f_\mathrm{PWM} = 100\,\mathrm{kHz}$, $f_\mathrm{T} = 50\,\mathrm{Hz}$, $f_\mathrm{o} = 2\,\mathrm{kHz}$, $m_\mathrm{nom} = 0.75$, $i_\mathrm{o,nom} = 3\,\mathrm{A}$, $\varphi_\mathrm{o} = 0°$, $T_\mathrm{D,HB} = 15\,\mathrm{ns}$, $T_\mathrm{D,DB_{SR}} = 20\,\mathrm{ns}$, $I_\mathrm{Off} = 5\,\mathrm{A}$, $U_\mathrm{DC} = 400\,\mathrm{V}$ ($150\,\mathrm{V}$ with $\mathrm{GaN_{T2}}$).

Switches which have a low thermal impedance to the ambient temperature show less distortion as their junction temperature swing during an output period is lower in amplitude and hence, their parameters (e.g., $R_\mathrm{DS,on}$) are changing less. As a comparison, the HB topology with the $\mathrm{GaN_{T1}}$ switch is also illustrated.

D. Sensitivity to the Dead Time

The dead time T_D in the HB topology has a significant influence on the THD as illustrated in **Fig. 11**. It is noteworthy that the THD shows a local minimum regardless of switch technology. This is due to the fact that in topologies with dead time, the transistor's output capacitance helps to reduce distortion as it symmetrizes the voltage switching transitions, which only works well in certain operating ranges [27]. This local minimum's position and extent depends on the output capacitance of the switch as well as R_on of the gate driver.

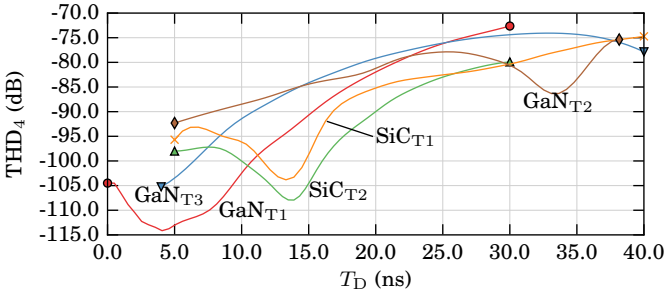

Fig. 11: Influence of the dead time T_D with different switches in the HB topology. $f_\mathrm{PWM} = 100\,\mathrm{kHz}$, $f_\mathrm{T} = 50\,\mathrm{Hz}$, $f_\mathrm{o} = 2\,\mathrm{kHz}$, $m = 0.75$, $i_\mathrm{o} = 3\,\mathrm{A}$, $\varphi_\mathrm{o} = 0°$, $U_\mathrm{DC} = 400\,\mathrm{V}$ ($150\,\mathrm{V}$ with $\mathrm{GaN_{T2}}$).

E. Sensitivity to the Offset Current

Similar than the dead time in the HB topology, the offset current I_Off influences the THD in the DB topologies as shown in **Fig. 12**. In the DB and $\mathrm{DB_{SY}}$ topologies, the THD increases with increasing I_Off since a higher offset current leads to faster switching transitions. However, at a certain magnitude of I_Off, the thermal variations of the devices lead to a deterioration of the THD.

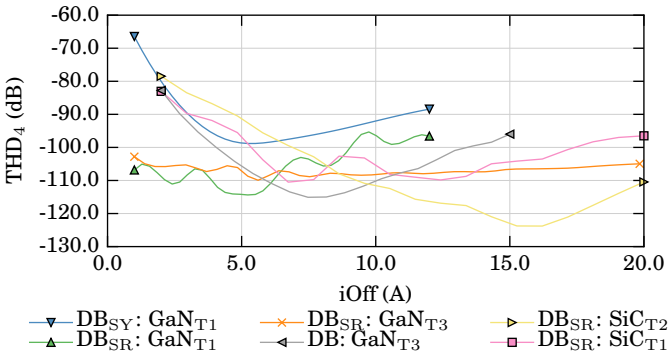

Fig. 12: Influence of the offset current I_Off with different switches in different DB topologies. $f_\mathrm{PWM} = 100\,\mathrm{kHz}$, $f_\mathrm{T} = 50\,\mathrm{Hz}$, $f_\mathrm{o} = 2\,\mathrm{kHz}$, $m = 0.75$, $i_\mathrm{o} = 3\,\mathrm{A}$, $\varphi_\mathrm{o} = 0°$.

The synchronously rectified (SR) dual buck topologies are more sensitive to the offset current. This is due to the influence of the gate turn-on resistor $R_\mathrm{on}$on the output voltage transition during the dead time interval which is required for this topology.

F. Sensitivity to the Switching Frequency

The influence of the switching frequency f_{PWM} is illustrated in **Fig. 13** for both the HB and DB topologies. For higher switching frequencies, the relative duration of the nonzero output voltage transition time to the switching period increases which leads to higher distortion at higher switching frequencies.

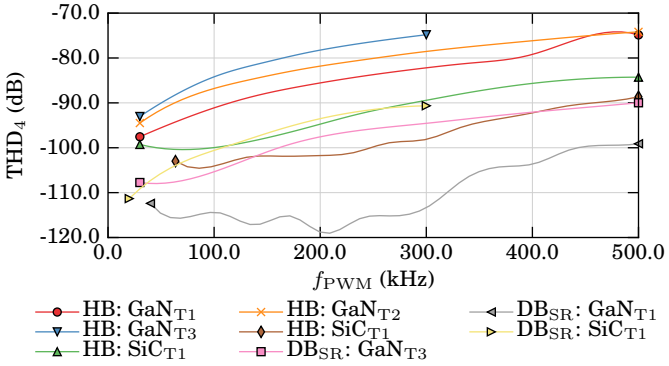

Fig. 13: Influence of the switching frequency f_{PWM} with different switches in different HB and DB topologies. $f_{\mathrm{T}} = 50\,\mathrm{Hz}$, $f_{\mathrm{o}} = 2\,\mathrm{kHz}$, $m = 0.75$, $i_{\mathrm{o}} = 3\,\mathrm{A}$, $\varphi_{\mathrm{o}} = 0°$, $T_{\mathrm{D,HB}} = 15\,\mathrm{ns}$.

However, a low switching frequency might not be desired as the amplifier's output bandwidth strongly depends on f_{PWM}. A possible solution to this tradeoff between distortion and bandwidth is by operating several power stages with interleaved PWM signals whereas each leg has a relatively low switching frequency. In an interleaved system, the achievable output bandwidth increases linearly with the number of interleaved stages. Another possibility are multi-cell systems which are also based on an interleaved operation [17].

In the interleaved topologies (e.g., $\mathrm{HB}_{\mathrm{2xIL}}$), which consist of several identical switching units, the voltage presented to the output filter is the arithmetic mean of the individual units' output voltages. Assuming perfect symmetry of an interleaved topology and considering the fact that the interleaving of the PWM carriers does not affect low-frequency (baseband) harmonics, it is sufficient to investigate only a single switching unit as all output voltage spectra of the individual interleaved units are identical. The interleaving only affects spectral components and harmonics of the switching frequency which are not of interest in this analysis as it is assumed that these components are sufficiently filtered and therefore not of concern to the mechanical actuators.

G. Sensitivity Analysis Summary

This section evaluates the sensitivities of different topologies and switches to their parameters. Therefore, the sweeps of the sensitivity parameters x (cf. eq (7)) are evaluated in a fixed range as listed in **Tab. II**.

In **Fig. 14**, the absolute values of the maximum sensitivities over the ranges defined in **Tab. II** are illustrated for different DB topologies. The synchronously rectified DB topologies ($\mathrm{DB_{SR}}$) react more sensitive to most parameters as their dead time renders the leg's voltage transition dependent of the operating point to some degree. As a further measure of comparison, the average THD of each performed parameter sweep in the ranges listed in **Tab. II** is shown in **Tab. III** for the best performing configurations.

Parameter		Considered range
Modulation index	m	$0.05 \cdots 0.95$
Output current amplitude	i_{o}	$1\,\mathrm{A} \cdots 3\,\mathrm{A}$
Switching frequency	f_{PWM}	$50\,\mathrm{kHz} \cdots 500\,\mathrm{kHz}$
Dead time	T_{D}	$5\,\mathrm{ns} \cdots 40\,\mathrm{ns}$
Offset current	I_{Off}	$1\,\mathrm{A} \cdots 15\,\mathrm{A}$
Output phase angle	φ_{o}	$-90° \cdots 90°$
DC link voltage	U_{DC}	$0.3 \cdots 1.5 \cdot U_{\mathrm{DC,nom}}$

TABLE II: Parameters used in the sensitivity analysis and their corresponding range in which the data is evaluated.

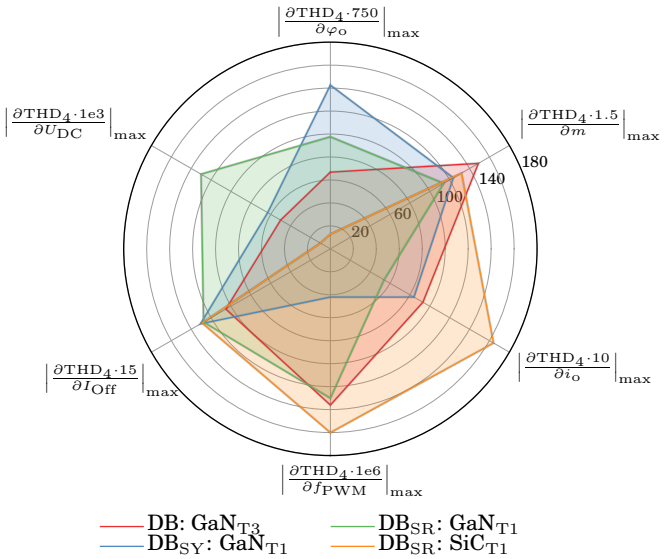

Fig. 14: Maximum of the absolute values of the sensitivities in their respective parameter ranges (cf. Tab. II) for different dual buck topologies.

IV. Conclusion

A comprehensive analysis of different circuit topologies and switch technologies for an amplifier system providing an extremely low output distortion over a frequency range from DC to several kilohertz with output voltages of several hundred volts is presented. Computer simulations that incorporate detailed semiconductor switch models and corresponding thermal models are used to analyze the effects of important circuit parameters.

The results reveal that the dual buck (DB) topology shows less distortion and parameter sensitivity than a single half bridge which requires some dead time at the switching state transitions. The offset current in the DB topology provides a degree of freedom which is used to reduce harmonic distortion. Furthermore, the improved synchronously rectified DB topology is symmetrical and shows less distortion than the traditional DB topology. Additionally, wide bandgap GaN transistors show higher switching dynamics and incorporate less parasitics in their packages which renders them superior to SiC transistors for the considered application. Using these devices in a DB topology, high-power and low-THD amplifiers are enabled which can reach THD values below $-110\,\mathrm{dB}$.

Topology	Switch	Swept Parameter m	i_o	f_PWM	T_D	I_Off	φ_o	U_DC	Total
$\mathrm{DB_{SR}}$	$\mathrm{GaN_{T1}}$	−103	−111	−110	n/a	−104	−113	−105	−107.6
	$\mathrm{GaN_{T2}}$	−76	−82	−79	n/a	−98	−94	−91	−85.3
	$\mathrm{GaN_{T3}}$	−99	−113	−103	n/a	−107	−109	−110	−106.8
	$\mathrm{SiC_{T1}}$	−90	−106	−90	n/a	−102	−96	−96	−96.7
	$\mathrm{SiC_{T2}}$	−87	−99	−87	n/a	−103	−92	−92	−93.3
$\mathrm{DB_{SY}}$	$\mathrm{GaN_{T1}}$	−94	−102	−93	n/a	−89	−102	−97	−96.2
DB	$\mathrm{GaN_{T1}}$, $\mathrm{SiC_{D1}}$	−96	−110	−96	n/a	−99	−103	−103	−101.2
	$\mathrm{GaN_{T3}}$, $\mathrm{SiC_{D1}}$	−100	−112	−99	n/a	−104	−107	−106	−104.7
HB	$\mathrm{GaN_{T1}}$	−88	−100	−84	−89	n/a	−94	−93	−91.3
	$\mathrm{GaN_{T3}}$	−78	−92	−82	−92	n/a	−90	−84	−86.3
	$\mathrm{SiC_{T1}}$	−95	−100	−92	−86	n/a	−101	−102	−96
	$\mathrm{SiC_{T2}}$	−77	−85	−97	−91	n/a	−91	−91	−88.7

TABLE III: Averages of the $\mathrm{THD_4}$ over the sweep ranges as given in Tab. II of selected topologies. Units: (dB). The nominal values of the parameters are: $m = 0.75$, $i_\mathrm{o} = 3\,\mathrm{A}$, $f_\mathrm{PWM} = 100\,\mathrm{kHz}$, $T_\mathrm{D} = 15\,\mathrm{ns}$, $I_\mathrm{Off} = 5\,\mathrm{A}$, $\varphi_\mathrm{o} = 0^\circ$, $U_\mathrm{DC} = 400\,\mathrm{V}$ or $150\,\mathrm{V}$ (for $\mathrm{GaN_{T3}}$).

The analysis performed for this paper only considered the power stage and the other system components (cf. **Fig. 2**) were modeled as ideal. Accordingly, besides experimentally verifying the presented theoretical analysis, several functional units need to be further considered, e.g., the distortion introduced by the finite precision of a digital modulator can be mitigated by using oversampled noise-shaping techniques [28]. Clock jitter, which occurs in any digital system, is also of concern and methods of reducing this effect will benefit the whole system [29]. Power supply variation can be minimized by incorporating a low-impedance supply and by feedback as well as feedforward control structures [30]. Furthermore, an appropriate converter control structure will improve the system's precision and reduce distortion even further [31].

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