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M. Antivachis,
M. Kasper,
D. Bortis,
J. W. Kolar

Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

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Michael Antivachis, Matthias Kasper, Dominik Bortis and Johann W. Kolar
Power Electronic Systems Laboratory
ETH Zurich, Physikstrasse 3
Zurich, 8092, Switzerland
antivachis@lem.ee.ethz.ch

***Abstract*—The Input Series Output Parallel (ISOP) multi-cell converter approach allows breaking the performance barriers of conventional single-cell telecom rectifier systems by leveraging the advantages of using multiple interleaved low-voltage and/or low-current converter cells. The ISOP interconnection in the DC/DC converter part of the cells, however, requires the employment of some kind of isolation in each cell, which is typically provided by transformers. An analysis of the losses and of the volume of the entire multi-cell system reveals that these transformers contribute a major part to the system losses and are responsible for a significant share of the total volume. However, as the transformers are mainly required for providing galvanic isolation in the ISOP structure and not for voltage conversion, series capacitors represent an alternative to decouple the series connected input terminals of the cells from the parallel connected output terminals. Compared to conventional solutions with transformers, the resulting capacitive power transfer ISOP multi-cell DC/DC converter (CPT-ISOP-MCC) system features lower losses and a smaller volume. In this paper, the benefits as well as the limitations in the design and operation of CPT-ISOP-MCC systems are analyzed in detail. In order to comprehensively evaluate the CPT against the magnetically isolated concept, i.e. inductive power transfer (IPT) converter topology, a multi-objective optimization is performed with respect to the achievable efficiency and power density for both types of converters. Based on the optimization result, a prototype of a CPT GaN DC/DC converter is realized and compared to its IPT GaN DC/DC converter counterpart, along with measurement results. Furthermore, a complete single-phase $3.3\,\mathrm{kW}$ AC/DC converter system with a high power density of $\rho = 3.92\,\mathrm{kW/dm^3}$ and an efficiency of $\eta = 97\%$ is presented, incorporating the CPT-DC/DC converter stages in ISOP topology.**

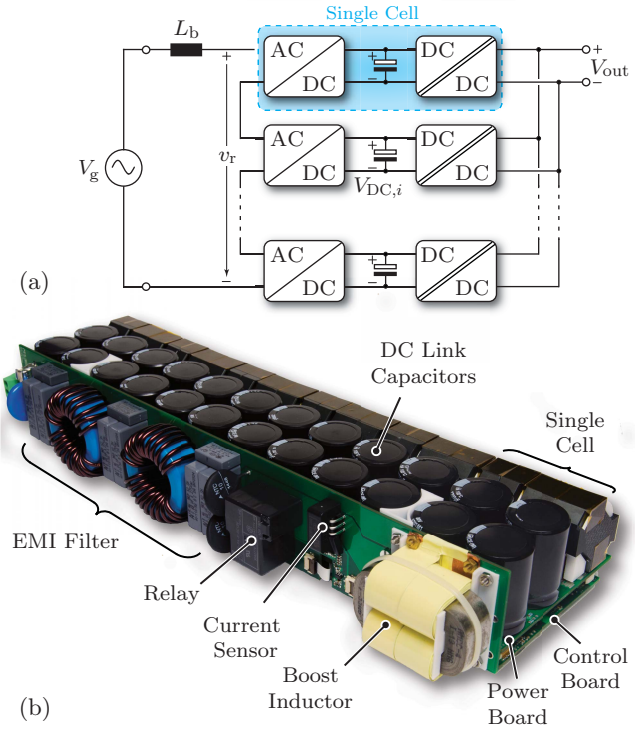

Fig. 1: ISOP multi-cell AC/DC telecom rectifier system: (a) Each converter cell contains an AC/DC rectifier input stage and a transformer isolated, i.e. inductive power transfer (IPT) DC/DC converter stage; (b) Hardware prototype ($V_{\mathrm{in,RMS}} = 230\,\mathrm{V}, V_{\mathrm{out}} = 48\,\mathrm{V}, P_{\mathrm{sys}} = 3.3\,\mathrm{kW}$) with $N_{\mathrm{cells}} = 6$ cells with a maximum efficiency of $\eta = 97.7\,\%$ and a power density of $\rho = 2.2\,\mathrm{kW/dm^3}$.

I. Introduction

Driven by the rising demand for highly efficient telecom and server power supplies resulting from the global trend of cloud computing, the industry research efforts for new converter topologies with improved performance concerning efficiency and power density have been considerably increased.

The most efficient and compact single-phase telecom power supply units that have been published so far are based on a modular approach. On the one hand, converter cells with the full voltage rating can be parallel interleaved, as for example in [1], where a triple-parallel TCM PFC rectifier system is combined with a double-parallel interleaved phase-shifted full-bridge (PSFB) DC/DC converter employing Si semiconductors. The concept of parallel interleaving allows to share the current between converter stages, which drastically reduces the ohmic losses, while a high partial load efficiency is attainable by always utilizing an optimal subset of the total number of parallel cells [2], [3].

On the other hand, the concept of connecting multiple converter cells in series allows to share the voltage stress among the cells and thus enables the use of low-voltage semiconductors with superior Figure-of-Merits compared to high-voltage semiconductors. This concept of series interleaving and splitting the voltage level among several low-voltage cells can either be only applied to the DC/DC converter stage of a telecom

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power supply (comprising a front-end PFC rectifier and an isolated DC/DC converter output stage [4]), or to the full converter system [5] as shown in **Fig. 1(a)** with a series connection of the cell's input terminals and a parallel connection of the output terminals (denominated as ISOP, i.e. input series output parallel arrangement, in the following). The latter fully modular and/or cellular structure facilitates a highly efficient and very compact system design ($\eta = 97.7\,\%$, $\rho = 2.2\,\mathrm{kW/dm^3}$, $V_{\mathrm{in,RMS}} = 230\,\mathrm{V}, V_{\mathrm{out}} = 48\,\mathrm{V}, P_{\mathrm{sys}} = 3.3\,\mathrm{kW}$) also for employing only low-voltage Si semiconductors (cf. **Fig. 1(b)**). In this system, each converter cell comprises an AC/DC rectifier input stage, which is a full-bridge operated with totem-pole modulation (i.e. one bridge leg operates with PWM and the other bridge leg switches with fundamental frequency), and an isolated DC/DC converter output stage realized as transformer isolated, i.e. inductive power transfer (IPT), phase-shifted full-bridge (PSFB) converter (cf. **Fig. 2(a)**) which is denominated as IPT-PSFB in the following. In [6] it is shown, that the ISOP converter approach provides significant benefits in terms of reduced conduction and switching losses and smaller volumes of inductive components and heat sinks. However, the analysis of the volume and loss distribution of the system shown in **Fig. 1(b)** reveals, that the majority of the losses is contributed by the DC/DC converter stages, where almost half of the losses in the DC/DC converters are resulting from the transformers. Furthermore, the transformers represent a significant part (60%) of the total volume of the DC/DC converter stages. The transformers have turns ratios of $N_1/N_2 = 1:1$ and thus are not required for stepping the cell DC-link voltage up or down but solely for providing the galvanic isolation between the parallel connected outputs and the series connected inputs. Therefore, the isolation can alternatively also be provided by coupling capacitors in series with the bridge leg outputs as shown in **Fig. 2(b)** resulting in a capacitive power transfer (CPT) phase-shifted full-bridge (CPT-PSFB) converter. These coupling capacitors allow to block the DC-voltage differences between the cell potentials on the primary side and the common secondary side output voltage. On the other hand, the capacitors are representing direct connections for the high-frequency differential mode AC signals of each DC/DC converter due to their low impedance, $Z_{\mathrm{c}} = 1/(\omega C)$, at high frequencies and thus do not disturb the operation of the DC/DC converters. As a result, the coupling capacitors can eliminate the two mentioned drawbacks of the transformers concerning volume and losses and are therefore allowing to further improve the system performance regarding efficiency and power density.

The concept of capacitive coupling (CC) for isolation purposes and/or CPT was introduced in [7] for SEPIC DC/DC converters due to the difficulty of using transformers in this kind of topology. In [8] and [9] the idea of CPT was extended to three-phase three-level AC/DC SEPIC PFC rectifiers. The design and realization of a CPT-DC/DC converter based on a series resonant converter (SRC) topology for a low-power wireless charging application was demonstrated in [10]. In order to achieve a high voltage conversion ratio with CPT-DC/DC converters, multiple capacitively coupled dual active bridge converters were interconnected in an ISOP arrangement

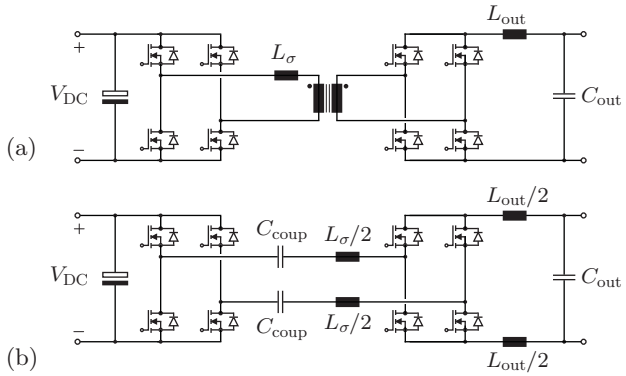

Fig. 2: Different isolation concepts for the phase-shifted full-bridge converter (PSFB): (a) Conventional magnetically coupled converter topology (IPT-PSFB) and (b) proposed capacitively coupled converter topology (CPT-PSFB) where the transformer is replaced by two coupling capacitors C_{coup} and series inductors L_σ.

in [11]. Furthermore, the applicability of CPT as a transformerless safety isolation feature in different converters topologies was demonstrated in [12] and [13]. Even though the above cited references have demonstrated the viability of CC as an alternative means to provide isolation in power converters, there has neither been an in-depth analysis of the degrees of freedom in the design of CPT-DC/DC converters in ISOP arrangement nor a comprehensive comparative evaluation between the IPT-based converter and the CPT-based converter in terms of achievable efficiency and power density.

Consequently, this paper thoroughly investigates the concept of CPT for ISOP multi-cell DC/DC converter (CPT-ISOP-MCC) systems and evaluates the achievable performance benefits of CPT compared to IPT converter systems. In a first step, the degrees of freedom in the design and operation of CPT-DC/DC converter cells in an ISOP configuration are analyzed in **Sec. II**. Subsequently, in **Sec. III** a multi-objective optimization of a CPT-PSFB DC/DC converter cell with low voltage GaN switches is performed with respect to efficiency and power density. The optimization results are compared to the achievable performance of an optimized conventional IPT-PSFB DC/DC converter cell. Furthermore, in **Sec. IV** two prototypes of GaN PSFB converter cells, one with CPT and the other with IPT isolation, are presented and measurement results are shown. Based on the findings of the previous sections, a full single-phase AC/DC telecom power supply employing a CPT-ISOP-MCC system as DC/DC conversion stage is presented in **Sec. V**. Finally, conclusions are drawn in **Sec. VI**.

II. Capacitively Coupled DC/DC Converters

In this section, several important aspects and design constraints of CPT-DC/DC converters are described.

A. ZVS Operation of a CPT-PSFB DC/DC Converter

The operation of a IPT-PSFB DC/DC converter typically relies on the leakage inductance of the transformer (besides the magnetizing inductance) to achieve soft-switching of the leading leg of the primary full-bridge. This bridge-leg is

always switched after the freewheeling phase where only the leakage inductance drives the switching transition. The condition for a complete soft-switching process depends on the stored energy in the leakage inductance, the stored charge in the parasitic output capacitance of the switches of the bridge-leg and the DC-link voltage [14]. Since the transformer is omitted in the CPT-PSFB concept, a dedicated inductor has to be added in series with the coupling capacitors for ensuring soft-switching. This inductor basically resembles the former leakage inductance of the transformer.

B. High-Frequency Common-Mode Analysis

Any common-mode (CM) disturbance on the primary or secondary side of CPT-DC/DC converters leads to unwanted CM currents flowing through the coupling capacitors. The disturbances can be, e.g., a result of certain modulation schemes of the primary side full-bridges of the ISOP connected DC/DC converters (cf. **Fig. 3(a)**) which result in high-frequency CM voltages. In a high-frequency equivalent circuit, each primary side full-bridge can be split into a CM and two differential mode (DM) voltage sources (cf. **Fig. 3(c)**) with

$$v_{\mathrm{CM},i} = \frac{v_{\mathrm{a},i} + v_{\mathrm{b},i}}{2} \tag{1}$$

and

$$v_{\mathrm{DM},i} = \frac{v_{\mathrm{a},i} - v_{\mathrm{b},i}}{2} \ , \tag{2}$$

where the output voltages of the bridge-legs ($v_{\mathrm{a},i}$ and $v_{\mathrm{b},i}$) are referenced to the imaginary mid-point of each input and/or DC-link capacitor. In the equivalent circuit, the series connected primary side full-bridges can be referenced to the same ground potential since the series connection of the DC-link capacitors is just a CM offset voltage seen by the coupling capacitors which is irrelevant to the following analysis (in a first step the input voltages $V_{\mathrm{DC},1}$ and $V_{\mathrm{DC},2}$ can be assumed constant, i.e. free of high-frequency components and of equal value).

In the case of phase-shifted modulation of the bridge-legs on the primary side, the voltage waveforms v_{a} and v_{b} exhibit DM as well as CM components, as shown in **Fig. 3(b)**. If the CPT-DC/DC converter cells are operated interleaved in order to reduce the total output current ripple (e.g. with a optimal phase-shift of $\delta = 360°/(2 \cdot N_{\mathrm{cells}})$, N_{cells} denominates the number of cells and the factor 2 is a result of the frequency duplication seen by the output inductors $L_{\mathrm{out},i}$, [15]), CM currents will circulate between the different cells. This is shown in **Fig. 3(b)** where the CM voltage of the second cell ($v_{\mathrm{CM},2}$) appears phase shifted against the first cell. In this case, the difference between these two CM voltages is $v_{\mathrm{CM,tot}} = V_{\mathrm{DC}}$ which can drive a CM current circulating between the two cells. Without proper attenuation, these currents can impair the system performance. In order to achieve the best attenuation of the CM currents, the series inductor and the output inductor should be split equally and placed in the positive and the negative rail, as shown in **Fig. 3(a)**. Based on the voltage-time area of the CM voltage and the impedance offered by L_σ and L_{out} the peak-to-peak CM current ripple can be derived

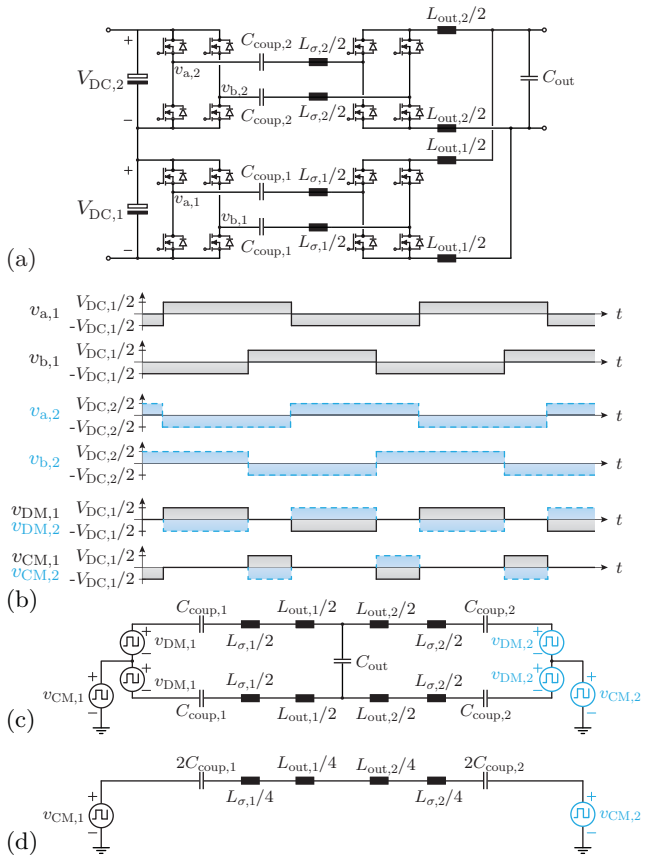

Fig. 3: High-frequency CM analysis of CPT-ISOP-MCC systems: (a) Example of two CPT-PSFB DC/DC converter cells in ISOP configuration with equal splitting of L_σ and L_{out} to the positive and negative rails in each cell. (b) Derivation of the CM and DM voltage waveforms of the primary side full-bridge of the first CPT-PSFB converter cell. The voltage waveforms of the second converter cell are also shown for the case that the two converter cells are operated interleaved. (c) Combined CM and DM equivalent circuit of the CPT-ISOP-MCC. (d) CM equivalent circuit only. (e) Possible locations for additional CM chokes.

according to the CM equivalent circuit of **Fig. 3(d)**, which is omitted here for the sake of brevity.

In addition, dedicated CM chokes can be added to the converter cells to achieve a greater attenuation of the high-frequency CM disturbance. The CM chokes can be inserted at different locations in the CPT-ISOP-MCC system as visualized in **Fig. 3(e)**.

Another concept for avoiding the problem of high-frequency CM disturbances uses bipolar operation of the full-bridges. In this operation mode the primary side bridge-legs are operated with a duty-cycle of 50% and a phase-shift of $180°$ and therefore the bridge-leg voltages v_{a} and v_{b} exhibit no CM voltage component if ideal switching transitions are assumed. This modulation scheme can be used e.g. in CPT series resonant converter cells or CPT dual active bridge converter cells.

In summary, the problem with CM disturbances in the CPT-ISOP-MCC system can be solved by

- preventing the creation of CM disturbances with no interleaving between the converter cells, i.e. synchronizing

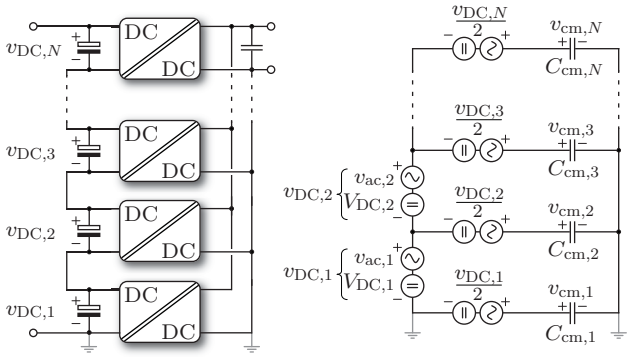

Fig. 4: Low-frequency CM equivalent circuit (right) of the CPT-ISOP-MCC system (left). (The output voltage is assumed constant, i.e. free of low-frequency as result of the output voltage control. Furthermore, the negative output terminal is considered to be connected to ground.) This equivalent circuit allows to model the influence of voltage fluctuations on the DC-link voltages $v_{DC,i}$. Due to the low frequency of the disturbance, the impedance of the CM path in each cell is dominated by the coupling capacitors whereas the series inductance and the output inductance can be neglected.

the switching patterns, or by

- employing CM chokes, if the impedance offered by the inductors L_σ and L_{out} is not sufficient, or by
- using bipolar modulation, such as applicable to CPT series resonant or CPT dual active bridge converters.

C. Selection of Coupling Capacitance Value

In order to select a suitable capacitance value for the coupling capacitors, the lower and upper boundaries of the capacitance values have to be derived.

For the upper boundary, the inherent power fluctuation present in a single phase AC/DC telecom power supply with twice the mains frequency, e.g. 100 Hz for the European mains, has to be considered. This power fluctuation results in a voltage ripple on the DC-link capacitors which is also present on the coupling capacitors. The voltage ripple creates unwanted CM currents charging/discharging the coupling capacitors and thus additional reactive power circulation. Mathematically, the peak voltage fluctuation ΔV_{tot} of the total DC-link with twice the grid frequency ω_g can be derived as

$$\Delta V_{tot} = \frac{P_{sys}}{2\omega_g \cdot C_{DC,tot} \cdot V_{DC,tot}} \tag{3}$$

(neglecting the energy stored in the coupling capacitors) where P_{sys} is the rated system output power, $V_{DC,tot} = \sum_{i=1}^{N_{cells}} V_{VD,i}$ is the average value of the total DC-link voltage and $C_{DC,tot}$ is the total DC-link capacitance (i.e. series connection of the DC-link capacitors of all cells and any additional full voltage capacitors of the DC-link). Under the assumption that ΔV_{tot} is small compared to the average DC-link voltage, the fluctuation of the DC-link voltage can be assumed to be sinusoidal. Hence, the input voltage of each cell can be written as sum of a DC-component and an AC-component, i.e.

$$v_{DC,i}(t) = V_{DC,i} + v_{ac,i}(t) = V_{DC,i} + \Delta V_i \cdot \sin(2\omega_g t)\ , \tag{4}$$

where $i \in [1, N_{cells}]$. Due to the self-balancing nature of the ISOP interconnection of the cells [15], it can be assumed that the input voltages of all cells are equal, which means that $V_{DC,i} = V_{DC} = V_{DC,tot}/N_{cells}$ and $\Delta V_i = \Delta V = \Delta V_{tot}/N_{cells}$. According to the low-frequency CM equivalent circuit of the CPT-ISOP-MCC system (cf. **Fig. 4**), the CM voltage across the coupling capacitors in a converter cell (i.e. $C_{cm,i} = 2 \cdot C_{coup}$) can be written as

$$v_{cm,i} = \left(i - \frac{1}{2}\right) \cdot V_{DC} + \left(i - \frac{1}{2}\right) \cdot \Delta V \cdot \sin(2\omega_g t)\ . \tag{5}$$

The AC-component of $v_{cm,i}$ drives a current through $C_{cm,i}$ which has an RMS-value of

$$I_{cm,RMS,i} = \frac{1}{\sqrt{2}} \cdot \left(i - \frac{1}{2}\right) \cdot V_{DC} \cdot 2\omega_g \cdot C_{cm,i}. \tag{6}$$

The total CM current through all coupling capacitors can thus be obtained by summing up all individual CM currents, i.e.

$$I_{cm,RMS,tot} = \sum_{i=1}^{N_{cells}} I_{cm,RMS,i} = N_{cells}^2 \cdot \frac{\Delta V}{\sqrt{2}} \omega_g \cdot C_{cm}. \tag{7}$$

This value can be related to the RMS-current value of the DC-link capacitors, given as

$$I_{DC\text{-}link,rms} = \frac{\Delta V_{tot}}{\sqrt{2}} \cdot 2\omega_g \cdot C_{DC,tot}, \tag{8}$$

which yields

$$k_{i,cm} = \frac{I_{cm,RMS,tot}}{I_{DC\text{-}link,rms}} = \frac{N_{cells} \cdot C_{cm}}{2 \cdot C_{DC,tot}}. \tag{9}$$

This equation can be solved to find the maximum allowable CM capacitance value and thus the maximum coupling capacitance value ($C_{cm,max} = 2 \cdot C_{coup,max}$) for a chosen value of $k_{i,cm}$. The result of the above calculations for a system with $N_{cells} = 6$, $P_{sys} = 3.3\,\text{kW}$, $\omega_g = 2\pi 50\,\text{Hz}$, $V_{DC,tot} = 400\,\text{V}$ and a peak voltage fluctuation of $\Delta V = 0.05 \cdot V_{DC,tot}$ of the DC-link and a chosen value $k_{i,cm} = 0.2$ yields a maximum allowable capacitance value of the coupling capacitors of $C_{coup,max} = 21.9\,\mu\text{F}$.

On the other hand, the lower boundary for the capacitance value of the coupling capacitors is defined by the maximum permissible voltage ripple caused by the high-frequency DM AC-current at full load operation. By approximating that the DM current through the capacitors is a square wave with a magnitude equal to the load current $I_{load,i}$ impressed by the cell output inductors (i.e. neglecting the ripple of the output current), the charge flowing into/out of the coupling capacitors during half a switching period is

$$Q_{DM} = \frac{I_{load,i}}{2 \cdot f_{sw}} \tag{10}$$

with f_{sw} being the switching frequency. If the total maximum differential mode voltage ripple at the coupling capacitors should be limited to a fraction of the cell DC-link voltage (i.e. $\Delta V_{DM} = k_v \cdot V_{DC}$) the total DM capacitance has to be at least

$$C_{DM,min} = \frac{Q_{DM}}{\Delta V_{DM}} = \frac{Q_{DM}}{k_v \cdot V_{DC}}\ . \tag{11}$$

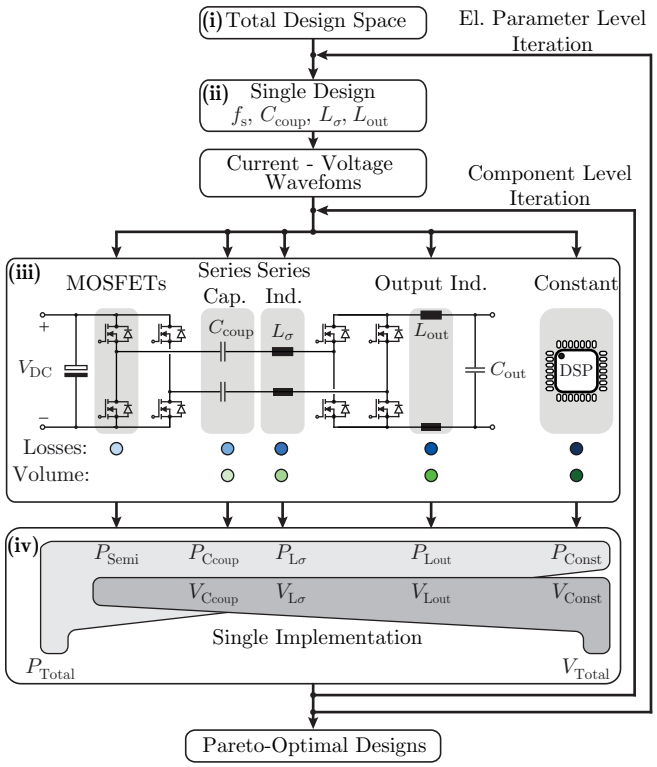

Fig. 5: Flowchart visualization of the multi-objective optimization of the CPT-PSFB DC/DC converter. The IPT-PSFB DC/DC converter has been optimized in a similar manner in [5].

Since the coupling capacitors are effectively connected in series for the DM equivalent circuit, each coupling capacitor is required to have a value of

$$C_{\text{coup,min}} = 2 \cdot C_{\text{DM,min}} = \frac{I_{\text{load},i}}{f_{\text{sw}} \cdot k_{\text{v}} \cdot V_{\text{DC}}} \ . \tag{12}$$

This value is inversely proportional to the switching frequency and thus a converter operating at a high switching frequency enables the use of coupling capacitors with a low capacitance and hence small volume. This favors the application of GaN semiconductors for the concept of capacitive coupling.

III. Converter Optimization

In order to obtain a comprehensive and meaningful comparison between the performance of the PSFB DC/DC converters with IPT and CPT, a multi-objective optimization with respect to efficiency and power density is performed for both concepts fulfilling the specifications of **Tab. I**. With this optimization the design space, which contains all degrees of freedom in the implementation of a converter system, is mapped into the performance space where the efficiency and power density of each converter design is shown. The mapping function is obtained by calculating the total losses and the total volume of each converter implementation which requires detailed models for the losses and volumes of the components employed in a design, as visualized in the flowchart in **Fig. 5**. Based on the obtained performance space, the Pareto-optimal designs can be identified for both converter concepts [16].

Tab. I: Specifications used for the optimization of the IPT-PSFB and CPT-PSFB converters.

Parameter	Variable	Value
Nominal Input Voltage	V_{in}	66 V
Nominal Output Voltage	V_{out}	48 V
Rated Power	$P_{\text{out,rat}}$	550 W

The design space contains different levels of degrees of freedom. The first level is the abstract level of electrical parameters, which defines a single converter design:

- *Switching frequency*: The switching frequency of both converter concepts (CPT and IPT) is varied in the range of $f_{\text{sw}} = 100\,\text{kHz}...400\,\text{kHz}$.
- *Output current ripple*: The peak-to-peak output current ripple is varied in the range of $\Delta I_{\text{out},i} = 5\%...20\% \cdot I_{\text{out,avg},i}$
- *Coupling Capacitance*: In the CPT-PSFB converter the value of the coupling capacitors is varied between the minimum and maximum values as derived in Sec. II.
- *Series Inductance*: The value of the series inductance in the CPT-PSFB and the leakage inductance of the transformer in the IPT-PSFB depends on the minimum output power level at which ZVS should be achieved. This level is set to $P_{\text{out,min}} = 30\% P_{\text{out,rat}}$.

For a single converter design (cf. **Fig. 5(ii)**) there are still many available degrees of freedom on the component level. Thus, the investigation of a single design constitutes a subordinate optimization problem, which yields a Pareto frontier for each component which are then combined into the total Pareto front of this single design implementation by sweeping through all possible combinations of the component implementations (cf. **Fig. 5(iii)**). The analysis includes:

- *Magnetic components*: The implementation of magnetic components offers a great variety of degrees of freedom including the core shape, core size, core material, winding type, winding number and air-gap. For all magnetic components in both concepts (i.e. transformer, output inductor and series inductor) ferrite material N87 (TDK-EPCOS) and litz wires are selected.
- *Coupling Capacitors*: For the CPT-PSFB prototype the coupling capacitors are chosen to have ceramic X7R material and a voltage rating of $V_{\text{DC,max}} = 250\,\text{V}$.
- *MOSFET*: For the MOSFETs the technology (i.e. Si or GaN) as well as the chip-size can vary. In this optimization, GaN is selected for highest performance. Due to the limited availability of GaN semiconductors with a blocking voltage of $V_{\text{DS,max}} = 100\,\text{V}$, only EPC2001c switches are considered without chip size optimization.

In order to map the obtained design implementations into the performance space, accurate component loss and volume models have to be applied for the aforementioned components:

- *Magnetic Components*: The modeling of magnetic components in terms of losses and volumes is a multi-physics problem since the electrical, the magnetic and the thermal domain are coupled as described in [17].
- *Coupling Capacitors*: The coupling capacitors contribute to additional volume and due to their ESR also to

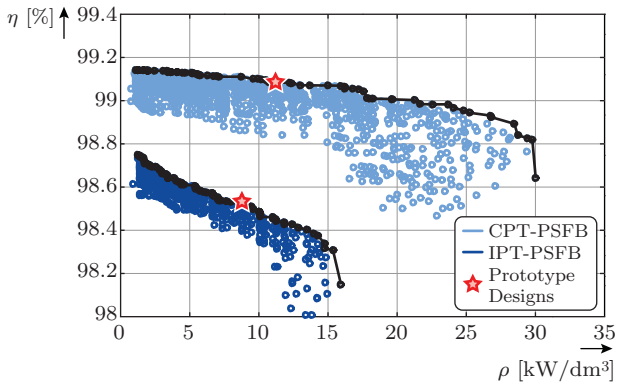

Fig. 6: η-ρ efficiency vs. power density Pareto optimization results of the GaN IPT-PSFB and the GaN CPT-PSFB DC/DC converter. The efficiencies are calculated for the operation at nominal voltages and an output power level of $P_{\text{out,opt}} = 80\%P_{\text{out,rat}}$. The power density is obtained by summing up all boxed component values of a design. Additionally, the designs are indicated which are selected for realization as prototypes.

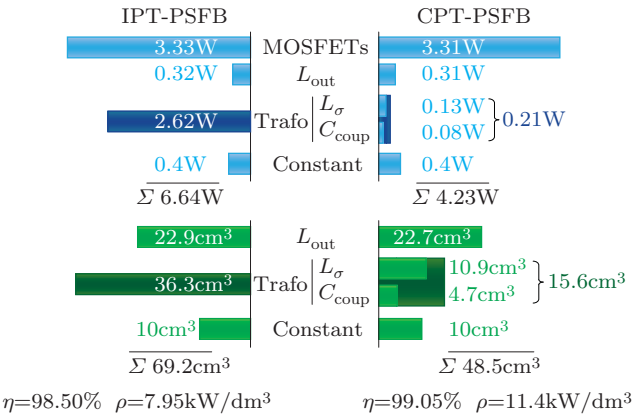

Fig. 7: Detailed break-down of the calculated losses and volumes of the components employed in the two prototype designs (i.e. IPT-PSFB and CPT-PSFB) for operation at nominal input and output voltages and an output power of $P_{\text{out}} = 80\%P_{\text{rat}} = 440\,\text{W}$.

conduction losses.

- *MOSFETs*: Due to ZVS operation of the MOSFETs only conduction losses and gate driver losses are taken into account.
- *Constant Losses and Volumes*: The losses caused by auxiliary electronics like the DSP are approximated by a constant loss term of $P_{\text{const}} = 0.4\,\text{W}$. The volume of the auxiliary electronics and the PCBs are estimated to be around $V_{\text{const}} = 0.01\,\text{dm}^3$.

By summing up the losses (calculated for an output power level of $P_{\text{out,opt}} = 80\%P_{\text{out,rat}}$) and volumes of all components in each design implementation (cf. **Fig. 5(iv)**), and by consequently iterating the process for all the designs constituting the complete design space, the total performance space is created. The results of this optimization process for both converter topologies are shown in **Fig. 6** with respect to efficiency (η) and power density (ρ) of the designs.

The power density is calculated by relating the rated power to the sum of the boxed component volumes. In a real setup, the space between the components and mechanical constraints will reduce the power density by a factor of 0.6...0.8. This is especially true for the highly compact designs of the CPT-PSFB converter (i.e. $\rho \geq 30\,\text{kW/dm}^3$).

The electrolytic DC-link capacitors are not part of the optimization since they can be regarded as part of the AC/DC conversion stage to filter the power fluctation with twice the mains frequency.

Nevertheless, the optimization results clearly indicate the performance benefits offered by the concept of capacitive coupling. For the same power density the CPT-PSFB converter achieves an efficiency improvement of $\Delta\eta = +0.4\%...+0.7\%$ compared to the conventional IPT-PSFB converter. Additionally, the CPT-PSFB converter allows to achieve power densities which are a factor of two higher than the maximum achievable power density of the IPT-PSFB converter.

IV. Measurement Results

Based on the optimization results of the previous section, two designs are selected (i.e. one design of the IPT-PSFB converter and one design of the CPT-PSFB converter, cf. **Fig. 6**) for experimental verification. A detailed break-down of the losses and volumes of the two converter designs is shown in **Fig. 7**. The designs for the realization as prototypes have been selected such that they have the same output inductor volume. Thus, the improvement in power density by removing the transformer and replacing it with coupling capacitors and a series inductor can directly be seen in **Fig. 8(a)** and **(b)**, where the prototypes are depicted in a side-by-side comparison. The coupling capacitors of the CPT-PSFB converter are placed partially also in between the control and power board. A detailed list of the components employed in the IPT-PSFB and CPT-PSFB GaN converter prototypes is given in **Tab. II**. The efficiencies of both systems have been measured for nominal operating voltages and different levels of output power. The measurement results are shown for comparison in **Fig. 8(c)**. The PCBs in both converter prototypes have four coppers layers with a copper thickness of $t_{\text{Cu}} = 35\,\mu\text{m}$ each, which leads to total resistances of the PCB conduction paths of $R_{\text{PCB}} = 7\,\text{m}\Omega$ in both converters. The resistive losses caused by the PCBs are subtracted in the corrected efficiency curves of **Fig. 8(c)** which can be considered as upper limits for the prototypes if thicker copper layers are chosen. But even then the efficiency measurement results of the converter systems are lower than the calculated efficiency values (cf. **Fig. 7**). One reason for this was found to reside in the losses associated with the charging/discharging process of the synchronous rectification full-bridge and the attached overvoltage snubber, as used in [6]. Furthermore, the difference between the calculations and the measurements can also be partially explained by higher than expected conduction losses in the GaN switches due to suboptimal gate driver layouts which resulted from the compromise to achieve a higher power density. This effect also prevented measurements at elevated power levels due to the limitations of the passive cooling concept. Nevertheless, the

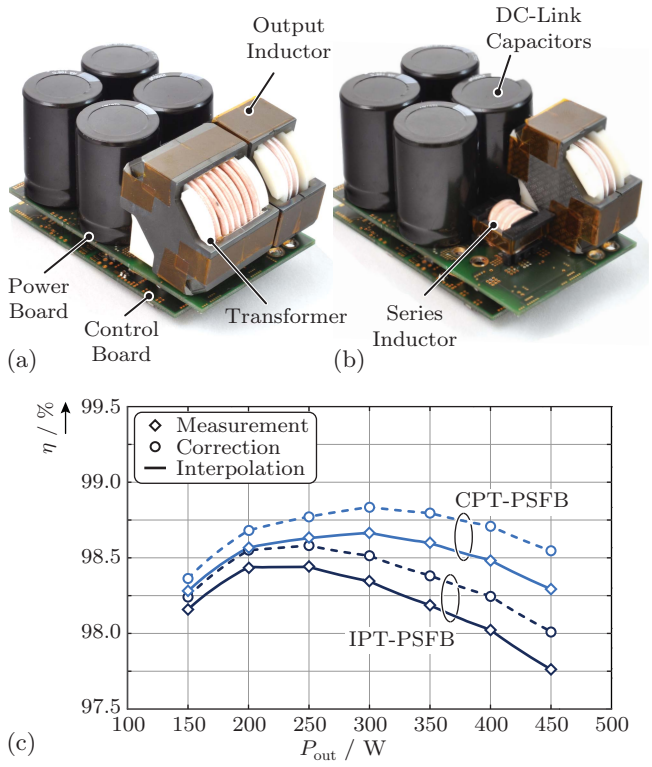

Fig. 8: Experimental results: (a) Hardware demonstrator of the GaN IPT-PSFB DC/DC converter and (b) hardware demonstrator of the GaN CPT-PSFB converter. By replacing the transformer with a series inductor and coupling capacitors (placed in between the control and power board), the total volume of required components can be decreased. (c) Comparison of the measured efficiency of the two converter prototypes. The corrected efficiency curves (shown dashed) are obtained by subtracting the resistive PCB losses and can be regarded as upper efficiency limits for the case where thicker PCB copper layers are used.

gain in efficiency which can be achieved by the transformerless CPT-PSFB system in contrast to the IPT-PSFB converter is clearly recognizable.

V. Full AC/DC Telecom Power Supply Module

The superior performance of the CPT-DC/DC converters, compared to their conventional IPT counterparts is evident from the previous sections. However, in the context of a telecom rectifier application, the AC/DC stage, which is an indispensable part of the system, must also be incorporated in the multi-objective optimization. Only then, tangible results on a holistic system level can be acquired.

Tab. II: List of employed components in the IPT-PSFB and the CPT-PSFB GaN converter prototypes.

Parameter	IPT-PSFB	CPT-PSFB
Switching Frequency	155 kHz	185 kHz
MOSFETs (prim. & sec.)	EPC2001c, $R_{DS,on} = 7\,m\Omega$	EPC2001c, $R_{DS,on} = 7\,m\Omega$
Output Inductor	$Lo = 12.6\,\mu H$ $N_{turns} = 4$ RM14LP ferrite N87	$Lo = 28\,\mu H$ $N_{turns} = 4$ RM14LP ferrite N87
Transformer	$N_{prim} : N_{sec} = 7 : 7$ RM14 ferrite N87	N/A
Series Inductor	N/A	$Lo = 1\,\mu H$ $N_{turns} = 4$ E20 ferrite N87
Coupling Capacitors	N/A	$C_s = 12\,\mu F$, X7R SMD 2220, V_{max}=250 V

If the DC/DC converter stage in the telecom power supply is realized as a CPT-ISOP-MCC, the AC/DC rectifier stage has to provide a single DC-link voltage in order to avoid steeply changing cell potentials as given for the fully modular/cellular concept of **Fig. 1(a)**. For achieving highest efficiencies of the AC/DC rectification stage, the switching as well as the conduction losses have to be minimized. On the one hand, the switching losses of the high-voltage (i.e. $V_{DS} = 600\,V$) switches can be reduced, if not completely eliminated, by means of ZVS operation like with a triangular current mode (TCM) control. On the other hand, the conduction losses can be lowered by paralleling and/or interleaving multiple TCM rectifier stages, such as proposed with 3 stages in [1] for a system with $\eta = 98.5\%$ and $\rho = 4.8\,kW/dm^3$. The semiconductors used in the implementation of [1] are Si MOSFETs which can be replaced by GaN HEMTs with the same voltage rating but lower $R_{DS,on}$ for the same chip area. Furthermore, since the double-line frequency power pulsation with the accompanying voltage ripple on the DC-link capacitors creates CM disturbances in the CPT-DC/DC converters, the power pulsation can be compensated by a dedicated Power Pulsation Buffer (PPB) [18]. This concept allows to obtain a stable DC-link voltage without any voltage fluctuation as well as to reduce the total size of employed DC-link capacitors. The improvement in power-density and voltage stability, however, is a trade-off with the efficiency of the PPB. The employed semiconductors can also be GaN HEMTs with a voltage rating of $V_{DS} = 600\,V$ if a buck-type PPB is used.

The analysis of high-frequency CM disturbances in the CPT-ISOP-MCC has revealed, that topologies with bipolar modulation are preferable since they create no CM voltage component. This indicates that the CPT-DAB topology is the most promising and suitable choice for this kind of application as it also provides voltage controllability. By connecting at least six CPT-DAB converter cells in ISOP connection, the DC-link voltage of each cell is low enough to employ $V_{DS} = 100\,V$ GaN HEMTs.

The schematic of the power circuit of the full single-phase telecom power supply incorporating all of the above mentioned parts is depicted in **Fig. 9**. Based on the cited publications and the results of this paper, a performance estimation of this system results in a power density of $\rho = 3.92\,kW/dm^3$ and an efficiency of $\eta = 97\%$. Hence, the approach of capacitive coupling enables a new path to achieve very high power-densities.

As a comparison, in case the IPT-DC/DC converters are employed, the utilization of a modular AC/DC stage is enabled (**Fig. 1(c)**) which results in a more efficient but less compact converter system ($\eta = 98\%$, $\rho = 2.2kW/dm^3$, $V_{in,RMS} = 230\,V$, $V_{out} = 48\,V$, $P_{sys} = 3.3\,kW$, [5]).

Thus, it can be deduced that the choice between capacitive and magnetic coupling of the DC/DC converters and the related consequences for the design of the AC/DC stage represents a trade-off between efficiency and power density, with the

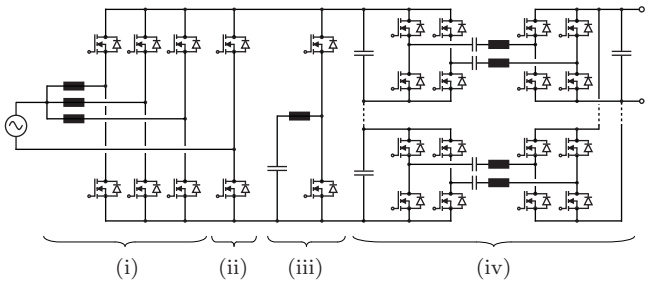

Fig. 9: Proposed single-phase AC/DC telecom power supply module with a CPT-ISOP-DC/DC stage employing only GaN switches: (i) Triple interleaved high-frequency bridge-legs of the TCM PFC rectifier stage, (ii) low-frequency totem-pole bridge-leg, (iii) power pulsation buffer for compensation of the pulsation of the input power, and (iv) CPT-ISOP-DC/DC converter stage comprising six ISOP connected CPT-DC/DC converter cells. (Please note, that the CM and DM EMI input filters are not shown due to space constraints.)

approach of capacitive coupling potentially enabling high power densities and the concept of magnetic coupling allowing for high efficiencies.

VI. Conclusions

The design steps towards a highly efficient and extremely compact ISOP-DC/DC converter system beyond the limits of state-of-the-art systems are presented based on the concept of CPT. This concept allows replacing the transformers of the DC/DC converters of a conventional approach with a significantly more compact and efficient combination of coupling capacitors and series inductors. The limitations and design constraints associated with the approach of CPT are analyzed in detail in this paper, including the phenomenon of circulating CM currents in the CC-ISOP-MCC system as a result of CM disturbances and their remedies.

In order to quantify the performance benefits of transformerless CPT converters against conventional IPT converters, a comprehensive multi-objective optimization is performed for both converter types with GaN semiconductors. From the optimization results it can be concluded that the capacitive coupling approach can simultaneously increase the power density as well as the efficiency of the DC/DC converters. This performance improvement is also verified with two DC/DC converter cell prototypes ,i.e. an IPT-PSFB converter and a CPT-PSFB converter with both employing low-voltage GaN semiconductors.

Finally, the investigated CPT-ISOP-MCC system is analyzed within the context of a complete AC/DC single-phase telecom power supply module in combination with a triple-interleaved TCM PFC rectifier and a PPB for compensating the double-line frequency power pulsation. The performance achievable with this system ($\rho = 3.92\,\mathrm{kW/dm^3}$, $\eta = 97\%$) shows that the concept of CPT enables a new path for system designs with exceptional power density.

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