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Performance Comparison of a GaN GIT and a Si IGBT for High-Speed Drive Applications

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***Abstract*— GaN power switches enable better switching characteristics compared to state-of-the-art power transistors that are widely used today. Due to their lower switching losses, GaN switches may lead to new horizons in key application areas of power electronics such as photovoltaic converters, high-speed electrical drives and contactless power transfer. However, this technology has not yet diffused fully into the industry. Therefore, today only limited experimental data is available on those switches.**

In this paper, a synchronous buck converter is designed using two 600 V, 15 A GaN GIT switches developed by Panasonic. Guidelines for an optimum PCB layout are given. Both electrical and calorimetric power loss measurements are shown. Finally, a comparison is made between the GIT and a similarly rated Si IGBT for high-speed electrical drive applications where the higher switching frequencies enabled by the use of GaN is shown to reduce the rotor losses in two typical types (slotted and slotless stator) of high-speed permanent-magnet electric machines.

Keywords*— *GaN, switching loss, loss measurements, motor drives

I. INTRODUCTION

Increasing the switching frequency of power electronic converters has been a long-term trend, driven mainly by smaller volume and/or higher power density requirements. Particularly converters employing a transformer or inductors benefit from higher switching frequencies. Typical examples are photovoltaic inverters, DC-DC converters used in distributed photovoltaic maximum power point trackers [1], telecommunication power supplies [2], automotive industry [3] and inductive power transfer applications [4].

Additionally, in electrical drives increasing the switching frequency of the inverter decreases the ripple of the machine current, leading to lower losses in the electrical machine. In [5] it is shown that by increasing the pulse-width-modulation (PWM) frequency of the inverter, the rotor losses of a permanent-magnet (PM) motor can be decreased. However, the increasing switching losses of the inverter may lead to a lower overall efficiency. This method may be used in applications such as high-speed spindles or drills below a few kW, where the machine compactness is of highest priority and additional losses in the converter can be tolerated.

However, the switching frequency of a converter cannot be increased beyond a certain limit, above which the switching losses decrease the converter efficiency to unacceptable values and the increased heatsink sizes decrease the power density. Moreover, the safe operation of the converter is endangered due to increased junction temperatures of the switches.

So far Gallium Nitride (GaN) devices have been employed mainly for radio-frequency or microwave applications [6]. However, their low on-state resistances and recently higher breakdown voltages make them an interesting option for power electronic switches [7]. In [8], a commercially available 200 V GaN transistor is used to build a switched capacitor voltage doubler that achieved 94.4% efficiency at 480 W output power while switching at 893 kHz. The same GaN transistor is tested in [9] and its switching characteristics are reported under hard and soft switching conditions. The performance of GaN and Si switches are compared in a 1 MHz 150 W dual active bridge DC-DC converter [10] where Si switches are only considered for the secondary side bridge.

Until recently, there have been no commercially available GaN power switches in the market with blocking voltages higher than 200 V [6]. However, today the performance of high voltage GaN switch prototypes is reported in an increasing number of publications. In [11], advances in GaN power switches are reviewed, and a novel cost-effective, normally-off Gate-Injection-Transistor (GIT) is presented. The specific on-state resistance and the off-state breakdown voltage of this device are reported as 2 $m\Omega cm^2$ and 700 V. Furthermore, six GITs forming a three-phase inverter are integrated in one IC which is used for driving a motor with up to 20 W of output power. Discrete GaN GITs with a blocking voltage of 650V are used to build a three-phase motor drive in [12]. The efficiency of this inverter is reported to be over 98% between 100 W and 900 W output power at 200 V DC link voltage and 6 kHz switching frequency. A similar inverter built using discrete GaN GIT switches is reported to have an efficiency of 99.3% at 1500 W output power when the switching frequency is 4 kHz in [13]. A boost converter for photovoltaic maximum power point tracking is built in [6]. A 600 V 15 A GaN GIT and a Si IGBT with similar ratings are compared for the realization of the transistor and a 600 V 15 A GaN and 600 V 16 A SiC Schottky diode are comparatively evaluated for implementing the freewheeling diode of the

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boost converter. The GaN GIT is shown to lead to higher efficiencies compared to the Si IGBT whereas the GaN and SiC Schottky diodes show similar performance. However, the lower production costs of the GaN diode is argued to result in the future in very competitive prices compared to the SiC devices. A 1 kW, 1 MHz resonant DC-DC converter built using GaN GITs is shown in [14] where the factors limiting the performance (overheating components) are reported to be the inductive components and not the transistors. A motor drive inverter using different 600 V GaN switches is shown in [15], and the reduction of the output filter size with increasing PWM frequency is highlighted. The possibility of using GaN power switches in automotive applications is reviewed in [3].

In this work, the performance of 600 V 15 A GaN GITs that are developed by Panasonic is evaluated experimentally in a DC-DC converter. The same GITs are also used in [6]. Due to the high switching speed of the GaN devices, switching losses are very difficult to determine accurately by measuring the device voltages and currents simultaneously, due to highly demanding bandwidth and synchronization requirements. Therefore, in this work a calorimeter is used for measuring the total heat generated by the converter system, resulting in a direct power loss measurement. Furthermore, using a DC-DC converter topology enables highly accurate electrical DC input and output power measurements for evaluating the switch performance, which are also carried out in addition to the calorimetric measurements.

Moreover, in this work the effect of the PCB layout on the converter performance is stressed and guidelines for an optimum PCB layout are given. Finally, the measured GaN GIT performance is compared to the performance of a Si IGBT in a motor drive application to show the benefits of the GaN switches.

II. The Prototype Converter

A. Topology selection

The main goal of this work is to evaluate the performance of the GaN switches experimentally and to assess the possible performance increase GaN switches may offer in a practical application. For doing so, a DC-DC buck converter is built using two GaN switches in a half bridge configuration.

There are several reasons for choosing this topology. Firstly, measuring the switch current and the voltage across the switch to determine the switching losses requires high measurement bandwidth and a very good synchronization between the current and voltage measurements. However, in a DC-DC converter, input and output power of the converter can be easily measured with high accuracy and the switching losses can be deduced using a model for the other lossy elements (in this case an inductor), eliminating the need for challenging measurement bandwidth and synchronization.

Secondly, the half bridge configuration is a building block that is used in converters for applications such as

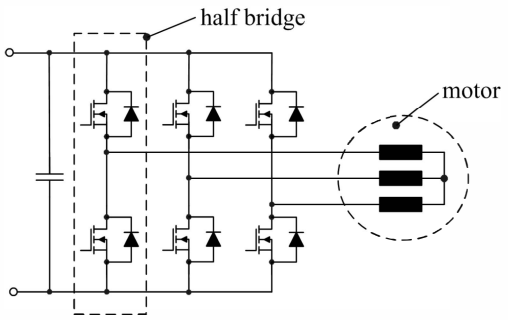

Fig. 1. A three-phase drive inver er, comprising three half bridge circuits (bridge legs), each of which can be seen as a bidirectional DC-DC conver er.

bi-directional DC-DC converters and motor drives. As an example, Fig. 1 shows a half bridge topology in a 3-phase 2-level inverter, which is widely used for AC motor drives. The abovementioned applications may benefit from the better switching performance GaN power switches are offering. However, the switching losses are also affected to a large extent by the actual circuit board layout and the layout parasitics. As no current and voltage measurements are needed directly on the switches, the circuit board layout can be optimized as in a final converter design. Therefore, the results taken on a half bridge configuration with an optimized circuit board layout are directly applicable to converters for a wide range of applications. The space requirement for two gate driver circuits instead of one makes the board layout more challenging, but also more realistic with respect to these applications.

Finally, in a half bridge topology, the parasitic couplings limit the switching speeds due to the false-firing (or spurious triggering) problem [16], [17]. For example when the upper switch turns on very fast, the parasitic capacitive coupling between the drain and the gate of the lower switch may cause the lower switch to turn on inadvertently, leading to a temporary cross conduction (short circuit of the DC link) which decreases the efficiency and may even lead to the destruction of the converter. In this work, this problem is taken into account as a half bridge topology is used.

Due to the reasons listed above, a half bridge topology was chosen to evaluate the switch performance while reflecting the situation in converters used for a wide range of applications.

Fig. 2 shows the half bridge converter built using 600 V, 15 A GaN GIT switches.

B. Gate drive circuit

Two identical gate drive circuits fed with isolated DC-DC converters are used for driving the power switches. A LM5114 gate driver IC from Texas Instruments is selected because its high current source/sink capability allows fast switching of the GaN switches. Another useful feature of this IC is the independent source and sink outputs, enabling different impedances for the turn on and turn off paths and making it possible to control rise and fall times independently. The gate drive circuit is shown in Fig. 3. For turning the switch on, 3.5 V is applied between its gate and source

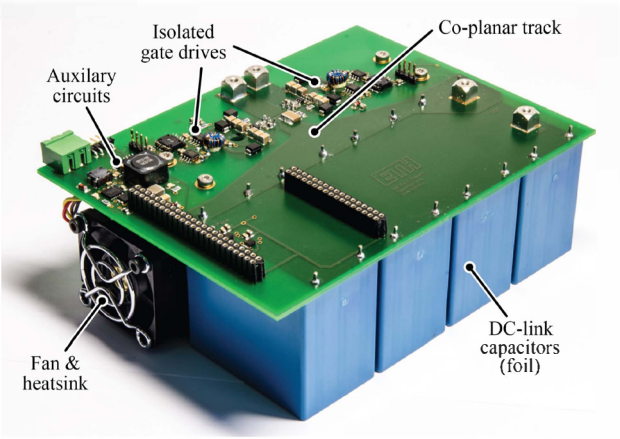

Fig. 2. Photograph of the half bridge circuit using GaN GIT switches.

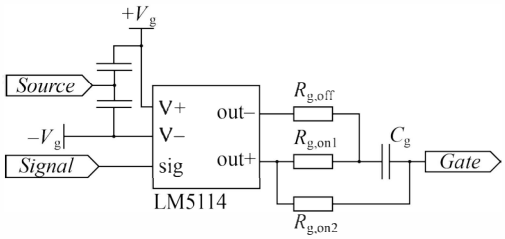

Fig. 3. Schematic of the gate drive circuit. $+V_g$ and $-V_g$ voltages are generated by an isolated DC-DC converter, and may have different amplitudes (e.g., +3 V, -5 V) with respect to the source potential of the power switch.

via an R-C network. $R_{g,on1}$ along with C_g determines the maximum gate current and its duration whereas $R_{g,on2}$ is used to adjust the continuous gate current to keep the device in conduction. Increasing the maximum gate current leads to higher switching speeds and hence to lower switching losses. However, due to the parasitic inductance of the commutation loop, very high switching speeds may lead to voltage spikes on the switches. As the GITs used in this work are not avalanche rated, the voltage across the device should never exceed the rated voltage, not even during the switching transients. Furthermore, the low threshold voltage (around 1.2 V) of the GITs and a very fast switching may lead to unintentional turn on as described in [16] and [17]. A very low or zero $R_{g,off}$ ideally reduces the impedance between the gate and source when the device is off. However, it has been found experimentally that a resistance lower than 15 Ω leads to unwanted oscillations in the gate circuit due to the parasitic inductances and capacitances.

In the off-state a negative voltage is applied between the gate and source of the switch to avoid unintentional turn on. However, a negative gate voltage increases the voltage drop on the switch during its reverse current conduction (during the dead time, where both switches of the half bridge configuration are turned off), leading to higher losses [18]. Therefore the dead time has to be as short as possible. On the other hand, the minimum necessary dead time in a half bridge configuration depends on the output current. As the investigation of a load dependent dead time is beyond the scope of this work, here the dead time is set to 150 ns, which is found to be adequate for output currents above 1 A.

The values of $R_{g,off}$, $R_{g,on1}$, $R_{g,on2}$, and C_g leading to the shortest switching times without causing oscillations exceeding the safe operating range according to the datasheet were experimentally determined to be 15 Ω, 5 Ω, 40 Ω, and 47 nF respectively.

C. Board layout considerations

For a fast switching converter, special attention must be paid to the printed circuit board (PCB) layout. Along with the package of the power semiconductors, the board design defines the parasitics that affect the performance of the converter, mainly due to the strong dependency of the switching losses on the parasitic elements. The GITs used in this work have a standard TO-220 package, which defines an important portion of the actual parasitics on the board that cannot be further reduced (the lead inductance of a TO-220 package can be up to 12 nH according to [19]). On the other hand, the board layout is optimized for minimum additional parasitics while using discrete elements for power switches, gate drivers and gate resistors.

Two important aspects to consider when designing the board are the gate loop layout, and the commutation loop layout [20], and they are discussed in the following sections.

1) Gate loop

The gate drive loop, i.e., the path of the gate current while turning the power switch on or off is shown in Fig. 4(a). Any parasitic inductance of this loop limits the switching speed of the power switch and leads to higher switching losses. A photo of the gate drive circuit is shown and the turn on path is highlighted in Fig. 4(b). When the switch is turned on, the current flows from the capacitor bank through the gate driver IC and the R-C network to the gate pin on the top layer of the PCB; and from the source pin back to the capacitor bank through the middle layer (the one that is closest to the top layer) of the PCB. The return path on the middle layer is designed as a plane instead of a thin track and connected to the top layer using several parallel connected vias to reduce the inductance as much as possible. Similarly, the gate current path while turning the switch off is shown in Fig. 4(c).

It can be seen in Fig. 4 that the gate loop design provides a return path for the current immediately beneath its flow path, minimizing the parasitic inductance. The arrangement of components given in Fig. 4 shows that a much smaller loop is not possible using discrete elements for the gate driver, the gate resistors and the gate capacitor. In such a configuration, the pins of the power switch's package are contributing significantly to the overall parasitic inductances.

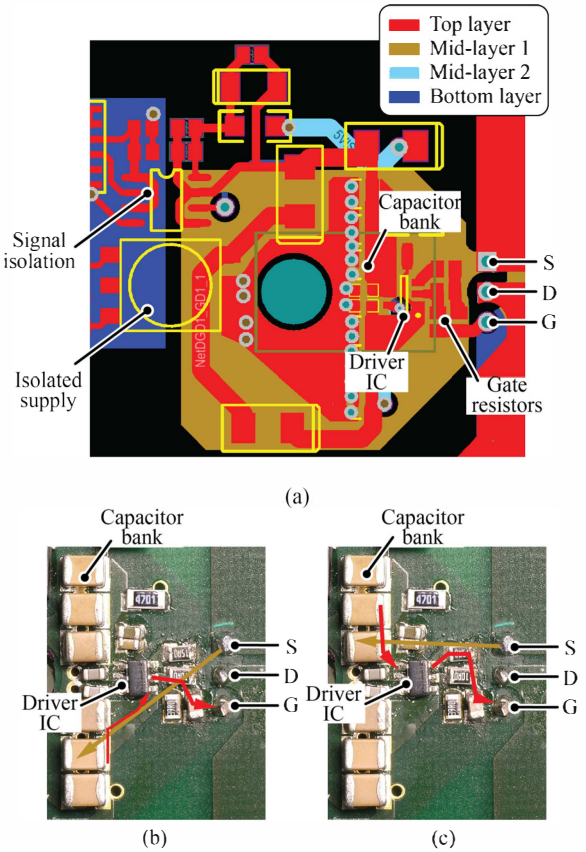

Fig. 4. (a) The gate drive circuit PCB layout. (b) Gate current path during turn on. (c) Gate current path during turn off. The colors of the arrows in (b) and (c) denote the board layer where the current flows.

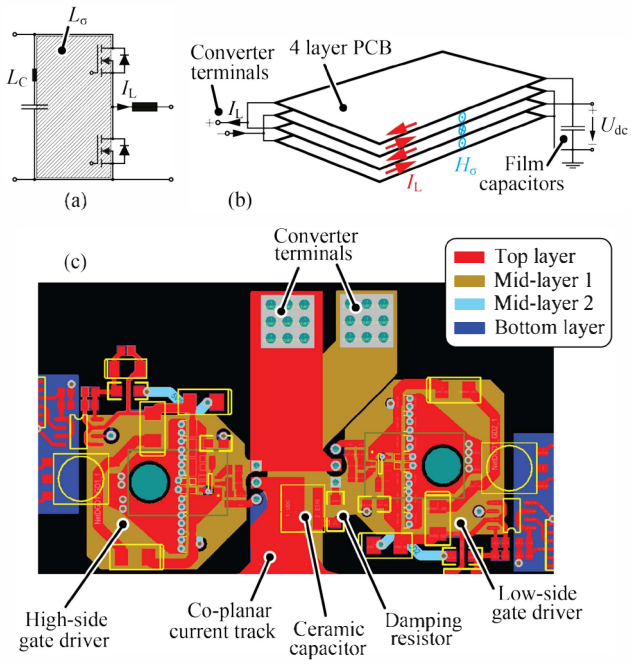

Fig. 5. (a) Commutation loop where L_C denotes the stray inductance of the capacitors and L_σ is the parasitic inductance introduced by the circuit board and the packages of the switches. (b) A co-planar track topology used to minimize the track inductance. (c) Circuit board layout showing the positioning of the two switches and their gate drive circuits.

2) *Commutation loop*

The commutation loop is the area covered by the path from the DC link capacitor bank through the upper and lower switch back to the capacitor bank, as shown in Fig. 5(a). A large commutation loop leads to higher voltage overshoot, decreased input voltage capability, and higher EMI [20].

The capacitor bank is made of foil capacitors that can be seen in Fig. 2, due to their low parasitic inductances. Four capacitors are connected in parallel for decreasing the parasitic inductance L_C of the capacitor bank further. The large package size and the pin positions of the foil capacitors lead to a large commutation loop area. Therefore, a small ceramic capacitor with a damping resistor is placed on the board close to the pins of the switches, as shown in Fig. 5(c). The commutation loop current path is arranged in co-planar tracks as shown in Fig. 5(b), in order to minimize the parasitic inductance.

III. The Measurement Setup

The total losses of a converter can be measured directly using thermal measurements with a calorimeter. As this is a direct loss measurement, the accuracy is independent of the actual power being processed by the converter. This enables more accurate measurements when compared to electrical input and output power measurements. On the other hand, calorimetric measurements are time consuming, as the thermal time constant of a large calorimeter like the one used in this work can be in the order of hours, meaning that each measurement may take considerable time. Electrical measurements, on the other hand, can be taken as soon as the converter reaches a given operating point.

The measurement setup is shown in Fig. 6. An 11 mH air cored inductor and a 220 µF electrolytic capacitor is used to build a synchronous buck converter with the half bridge board. Yokogawa WT3000 power analyzer is used to measure the DC input and output powers as well as the separate power inputs for the gate drive circuits and the auxiliary power that supplies the signal processor board and the fan on the heat sink.

The difference of the electrical input – output power measurements gives the total losses of the converter, including the switching and conduction losses of the power switches as well as the losses of the inductor. As an air core inductor is used with a sufficiently large inductance, the output current can be assumed to be DC. Hence, the inductor losses can be calculated using its DC resistance, which is measured to be 507 mΩ (including the cabling of the test setup) using a voltage source with a current limit, two Agilent 34410A multimeters and a Burster 1282 10 mΩ shunt resistor. The accuracy of the multimeters are ± 0.6% for the current measurement and ± 0.04% for the voltage measurement. The shunt resistor has 20 ppm accuracy.

IV. Measurement Results

Table I shows the measurement results taken by both the power analyzer and the calorimeter where f_{sw} is the switching frequency, P_{out} is the output power, I_{out} is the inductor current, P_{aux} is the supply of the signal processor and the cooling fan, T_j is the estimated junction temperature based on a thermal model of the switches and the heat sink, P_{cal} is the power measurement read by the calorimeter and P_{el} is the difference of the total electrical input and output power measurements after subtracting the estimated power losses of the inductor and the cables of the set setup. The calorimeter and the electrical power analyzer are connected together, i.e., electrical and thermal measurements are taken simultaneously. The input voltage is 400 V and the duty cycle is 0.5 for all the measurements described in this work.

Results of the calorimetric loss measurements are also plotted in Fig. 7 and Fig. 8. In Fig. 7, the estimated junction temperature difference between the maximum and the minimum switching frequencies is minimum (15 °C) for 3.5 A and maximum (25 °C) for 6.5 A.

A junction temperature rise from 75 °C to 100 °C increases the on-state resistance of the GaN GIT by only 10%; therefore this effect is neglected when estimating the switching energies. Assuming that the only frequency dependent loss component in the half bridge converter is the switching loss of the GITs, the total switching energies can be extracted as 140, 128, 118 and 93 µJ based on the calorimeter and 162, 141, 115 and 100 µJ based on the electrical power measurements at 6.5, 5.5, 4.5 and 3.5 A, respectively (all at 400 V). The estimated junction temperatures are not constant for these operating points, however, the results of double pulse measurements given in [6] shown that the switching losses of the GaN GITs do not change significantly with temperature, especially at drain current levels considered in this work.

V. Application Example: High-Speed Motor Drives

High-speed drives is an emerging topic gaining increasing popularity both in academia and industry due to the higher power densities enables by high rotational speeds. In [21], two typical high-speed machines are analyzed and the asynchronous harmonics in the air gap flux are shown to induce eddy current losses in the rotor. This decreases the machine efficiency. Furthermore, the rotors of these machines contain permanent magnets which demagnetize at elevated temperatures. In standard low-speed surface-mount permanent-magnet machines, there is no retaining sleeve on the rotor and the magnets can be segmented to limit the eddy current losses. However, for the high-speed machines such as the ones shown in [21], segmenting the magnets would only lead to shifting the losses from the magnets to the sleeve and segmenting the sleeve is not possible as a one piece metallic sleeve is needed to provide sufficient mechanical strength.

The rotor losses can be decreased by increasing the inverter switching frequency and having a more sinusoidal machine current [21]. However, the inverter switching frequency cannot be increased above a certain level due to the increasing switching losses. In certain applications where the machine compactness is of highest importance, lower inverter efficiency can be tolerated to save on the machine losses. However, the cooling capability and the maximum allowed junction temperature of the semiconductor switches of the inverter set an upper limit on the maximum inverter losses. For this reason, in this section the possibility of exploiting the performance of GaN GITs in high-speed drives is analyzed and the performance of the GIT is compared to a state-of-the-art Si IGBT.

The conceptual drawings of the two types of typical high-speed motors analyzed in [21] are shown in Fig. 9. The actual off-the-shelf machines analyzed in that work are rated at 600 W and 3.5 A, therefore not suitable to be

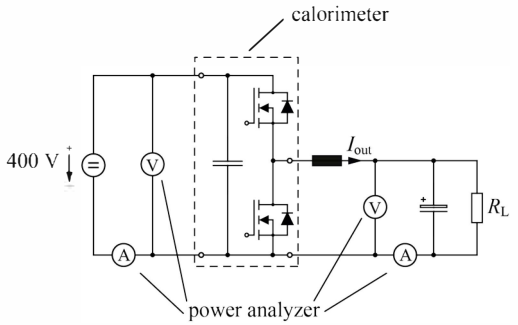

Fig. 6. The measurement setup. The power analyzer measures the input and output powers as shown. Two additional channels of the power analyzer are used to measure the gate and auxiliary (signal processor and fan) powers separately (not shown). The half bridge losses are also measured in a calorimeter. The output inductor is not placed in the calorimeter, therefore its losses need to be estimated and subtracted from the electric power measurements for a comparison with the calorimeter.

Table I. Measurement results.

f_{sw} (kHz)	I_{out} (A)	P_{out} (W)	P_{aux} (W)	T_j (°C)	P_{el} (W)	P_{cal} (W)
25	3.50	689.3	7.17	48	12.36	11.02
25	4.50	882.9	7.26	57	13.48	12.14
25	5.50	1076.2	7.26	64	13.16	13.58
25	6.50	1268.2	7.25	76	14.11	15.81
50	3.50	684.0	7.26	44	14.89	13.47
50	4.51	876.9	7.27	60	15.47	15.36
50	5.51	1068.9	7.25	70	16.58	16.42
50	6.52	1259.0	7.26	83	18.22	19.15
80	3.50	678.6	7.27	58	18.50	17.09
80	4.51	872.0	7.27	67	20.12	18.48
80	5.51	1057.8	7.26	78	21.26	21.26
80	6.50	1246.9	7.24	94	24.85	23.88
100	3.50	678.1	7.24	60	19.52	17.92
100	4.50	867.6	7.29	69	21.37	21.04
100	5.51	1055.8	7.27	81	23.46	23.32
100	6.51	1241.6	7.27	95	25.85	26.16
120	3.50	674.1	7.27	64	22.01	19.87
120	4.52	865.0	7.25	74	24.32	23.49
120	5.50	1048.8	7.20	87	26.67	25.49
120	6.50	1233.0	7.22	101	29.63	29.11

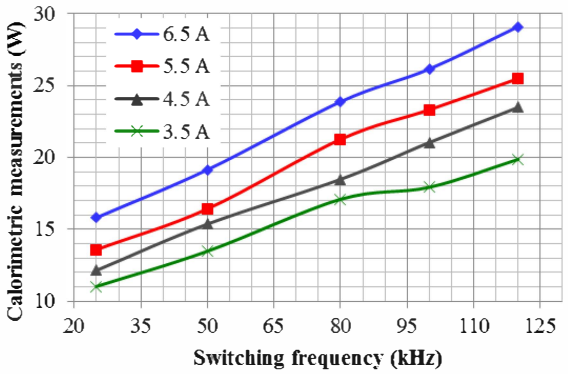

Fig. 7. Results of calorimetric loss measurements vs. switching frequencies. The measured values include the half bridge converter losses (switching and conduction losses, gate supply and auxiliary power) but exclude the inductor losses. If the temperature variations within measurements with the same output currents are neglected, the slope of the curve gives the switching energy of the GIT. The estimated junction temperatures for each operating point can be found in Table I.

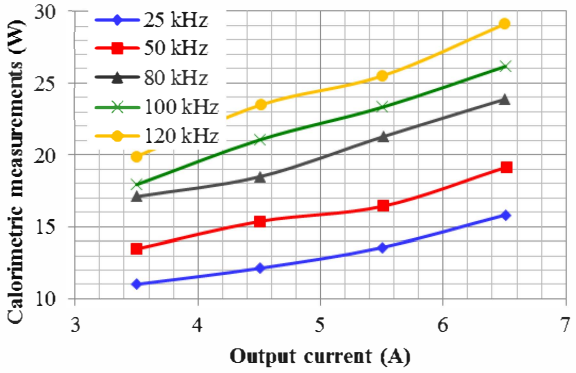

Fig. 8. Results of calorimetric loss measurements vs. different output currents. The measured values include the half bridge converter losses (switching and conduction losses, gate supply and auxiliary power) but exclude the inductor losses. The estimated junction temperatures for each operating point can be found in Table I.

considered as a direct application to the GITs analyzed in this work. Consequently, based on the actual machines of [21], two fictitious machines are designed by scaling the diameter of the machines to increase the rated power while keeping the nominal current density in the windings constant. The number of winding turns is adjusted to match the machine voltage with the 400 V DC link voltage at which the GITs have been tested. As the focus is on the relative machine loss change with respect to inverter switching frequency, a detailed thermal analysis is omitted in a first step. Mechanical constraints such as the stresses in the rotor or rotordynamic constraints are also neglected for the same reason. The parameters of the resulting slotted and slotless machines are given in Table II.

After the machines are designed, the phase current waveform is calculated analytically assuming a 2-level, 3-phase inverter operating with space-vector-modulation, taking the DC link voltage, the machine back EMF,

Table II. Parameters of the fictitious machines.

	Slotted	Slotless
Rated speed (rpm)	100,000	
Rated power (W)	3140	
Rated current (A)	7	
Flux linkage (mWb)	20.6	20.3
Phase inductance (μH)	320	155
Phase resistance (Ω)	0.54	0.21

machine inductance and the inverter switching frequency into account. The phase current waveforms for the slotless machine for 25 kHz and 200 kHz inverter switching frequency can be seen in Fig. 10.

Once the current waveform is generated, the core (stator iron) and rotor (eddy current) losses in the machine are calculated using a 2-D time-transient finite element (FE) model in which the calculated phase currents are impressed in the machine windings. The copper losses are calculated by the machine phase resistance and the RMS value of the calculated phase current, neglecting any skin and proximity effects. This is a reasonable assumption as generally litz wires are used in high-speed electric machines to limit skin and proximity effect losses.

A 600 V, 15 A Si IGBT with antiparallel diode in a TO-220 package (IKP15N60T) is selected to be compared to the GaN GITs analyzed in this work. This IGBT is selected because the current and voltage ratings as well as the package and the internal antiparallel diode make it a direct replacement for the analyzed GaN GITs.

Two inverters, one built with Si IGBT/antiparallel diodes and the other with GaN GITs are assumed. From the machine current calculated above and the switching signals, the currents through the IGBT/diodes (for Si inverter) and through the GaN GITs (for GaN inverter) are calculated separately. Currents at switching instants are calculated similarly. Finally, voltage drops over the Si IGBTs and the diodes as well as the switching energies for the IGBTs are read from the IGBT datasheet to estimate the total losses of the Si inverter for a given machine and operating point. For the GaN inverter, the on-state resistance is read from the datasheet (which is verified in [6]) and the switching energies are extracted from the measurements presented in this work.

The datasheet for the IGBT contains information on the switching and conduction losses at different junction temperatures. In [6], on-state resistance of the GIT is measured also at different temperatures. However, as the measurements in this work are carried out in a fixed ambient temperature the junction temperature of the GITs could not be controlled and varied between 45 ˚C and 100 ˚C. The average of estimated junction temperatures for all the measurement points is around 70 ˚C. Therefore, in order to make a fair comparison, also a junction temperature of 70 ˚C is assumed when reading the on-state resistance of the GIT and voltage drops over the Si IGBT and the antiparallel diode as well as the switching energies for the IGBT from datasheets.

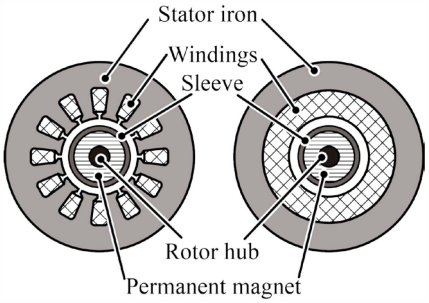

Fig. 9. Conceptual drawing of the slotted (left) and the slotless (right) types of high-speed permanent-magnet synchronous motors as shown in [21].

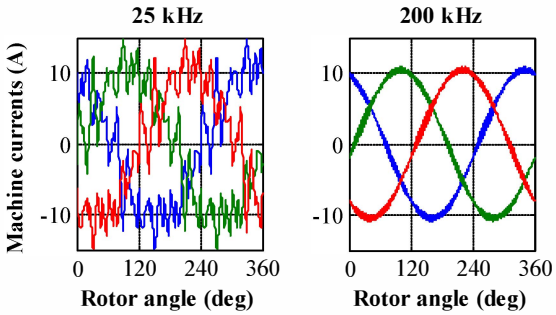

Fig. 10. Phase currents of the slotless machine at 25 kHz (left) and 200 kHz (right) inverter switching frequency.

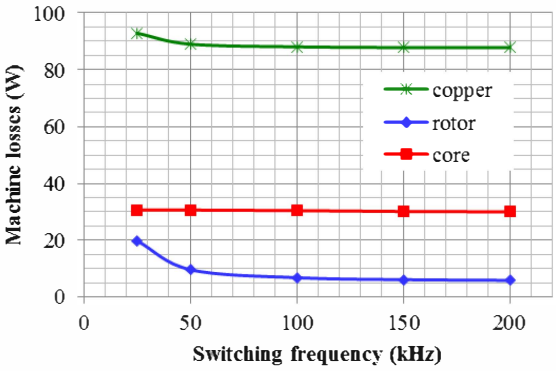

Fig. 11. Losses of the slotted machine vs. inverter switching frequency. If ideal (pure sinusoidal) phase currents are assumed, the copper losses are 80 W and the rotor losses are 5.5 W.

Different components of the machine losses are shown with respect to the inverter switching frequency in Fig. 11 for the slotted machine and in Fig. 12 for the slotless machine. It is clearly visible that for both machines, the rotor losses can be decreased significantly by increasing the inverter switching frequency. The slotted machine has more core losses due to higher flux density in the stator core and also due to its lossier stator core material compared to that of the slotless machine. Nevertheless, in both of the machines the iron losses do not change strongly with the inverter switching frequency because of the weak armature reaction. As the RMS value of the phase current also does not change much, the copper losses also stay almost constant beyond 50 kHz. The rotor losses approach zero in the slotless machine whereas they cannot be decreased below 5.5 W in the

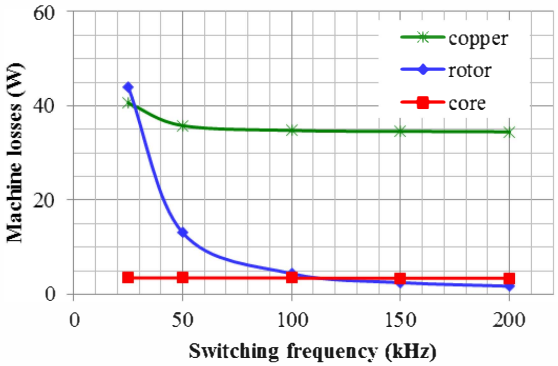

Fig. 12. Losses of the slotless machine vs. inverter switching frequency. If ideal (pure sinusoidal) phase currents are assumed, the copper losses are 31 W and the rotor losses are 0.3 W.

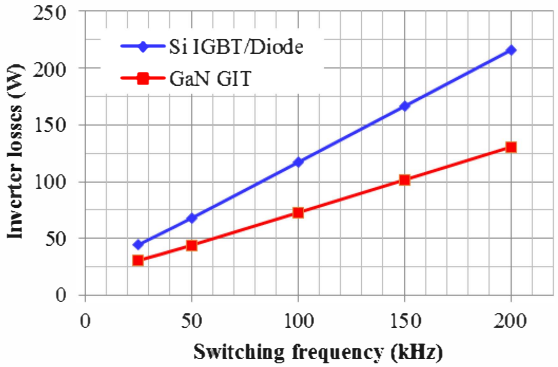

Fig. 13. Losses of the GaN and Si inverters vs. switching frequency. The machine is running at100 krpm and 300 mNm.

slotted machine. This amount of rotor losses is caused by the slot harmonics of the slotted machine, and would be present even if no harmonics are present in the phase currents of the machine.

Fig. 13 shows the estimated inverter losses when the slotless machine is driven by the Si inverter or the GaN inverter. The GaN inverter clearly outperforms its Si counterpart for this application. In other words, the GaN GITs analyzed in this work can be used advantageously in high-speed motor drives to push the switching frequency above limits that are today given by the state-of-the-art Si devices and lead to decreased rotor losses in the machines.

VI. Conclusions and Outlook

In this work, the performance of 600 V, 15 A GaN GIT power switches is investigated experimentally. Guidelines are summarized for an optimum design of the PCB layout. The test converter is a synchronous buck converter which comprises a half bridge configuration with an external inductor and a capacitor. The losses are determined under different operating conditions by electrical input and output power measurements as well as calorimetric measurements. The switching energies of the GITs are calculated from these experiments. When compared to measuring the switch voltage and currents

simultaneously to determine the switching energies, the method presented in this paper avoids the high bandwidth and synchronization requirements. Furthermore, as there is no current and voltage measurement directly on the transistors, the PCB layout of the half bridge circuit is optimized for minimum parasitics. As the actual switching losses depend on the PCB parasitics, the results of the measurements can be directly applied to converter systems that employ half bridge structures, e.g., bi-directional DC-DC converters or AC motor drives. On the other hand, as the measurements are done in a fixed ambient temperature, the junction temperature is not the same for the measurements presented in this work. In this work, this effect is neglected as the dependency of the switching energies and the on-state resistances of the GaN GITs are reported to be relatively insensitive to temperature variations.

High-speed electric drives are shown as a possible application for the GaN power transistors. Higher switching frequencies enabled by the use of GaN are shown to reduce the rotor losses in high-speed permanent-magnet electric machines and lead to higher efficiencies and/or higher power densities in machines.

In this work, the gate resistor and capacitor values are determined experimentally to keep the oscillations in the gate loop within safe operating limits and to avoid spurious triggering. Using packages that are better suited for high switching speeds (i.e., packages with smaller parasitic inductances) will enable better utilization of the GaN GITs.

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