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Comparative Evaluation of Minimum Conduction Losses of Battery-Integrated Multilevel Inverters

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Abstract*—Conventionally, high-voltage batteries are interfaced to ac systems (e.g., motors or the mains) via three-phase dc-ac inverters. Recently, battery-integrated multilevel inverters (BIMIs) have attracted interest by distributing the power electronics within the battery: each battery cell (or group of battery cells) is equipped with a low-voltage switching stage, and the resulting modules are cascaded into one string per phase. A first variant uses full-bridge (FB) switching modules with four switches each, whereas a second option termed "BM3" requires only three instead of four switches per module, which restricts the string output voltage to positive values and hence doubles the number of modules compared to the FB-BIMI (for equal ac output voltage capability), but facilitates paralleling of battery cells for lower instantaneous string output voltages. This paper first derives the optimal BM3-BIMI configurations for a given number of modules, minimizing conduction losses. Then, for equal total silicon (Si) chip area, an FB-BIMI still exhibits 10–30% lower conduction losses (depending on the modulation index) than a BM3-BIMI. To compare systems with different semiconductor materials, i.e., a two-level (2L) silicon carbide (SiC) inverter and BIMIs with Si switches, a possible characteristic is the embodied energy per semiconductor die area, which is closely related to the embodied carbon footprint and also related to cost. Targeting equal total embodied carbon footprint of the power semiconductors, a BIMI can thus use 3.25 times more Si chip area than a 2L SiC inverter (225 kW, 800 V dc) with a dc-side battery, which then achieves almost a factor of five lower total losses—even when including switching losses—than an FB-BIMI at nominal current. Furthermore, due to their phase-modular nature, BIMIs introduce strong low-frequency pulsations in the battery power flow, leading to approximately twice the battery losses compared to a 2L-based system using the same number of battery cells.

***Index Terms*—Battery-integrated multilevel inverter, ac battery, conduction losses, carbon footprint, two-level SiC inverter.**

I. Introduction

In typical battery applications, e.g., in electric vehicles, a three-phase two-level (2L) dc-ac converter, often realized with SiC power transistors (e.g., rated at 1200 V for an 800 V battery), interfaces a high-voltage (HV) battery to a three-phase mains or a three-phase motor, see **Fig. 1a.i**. The assembly of a HV battery from numerous individual battery cells further requires the use of a battery management system (BMS) for monitoring and balancing the state of charge (SoC) of the cells, etc. While a BMS may include switches to allow for charge transfer between neighboring cells (balancing), these switches are dimensioned for low currents only.

This has motivated concepts integrating the battery, the BMS, and the dc-ac inverter, by equipping each battery cell, or group of battery cells, with certain power conversion functionality, forming a battery-integrated multilevel inverter (BIMI), see **Fig. 1a.ii**. There, each phase of the converter is formed by a string of many modules containing a battery and a switching stage; the string can then synthesize a multilevel output voltage. This, however, results in an ac component in the string power and current, whereas a standard 2L inverter draws constant power and current from the dc-side battery (under symmetric phase loading and stationary operation), see **Fig. 1b**.

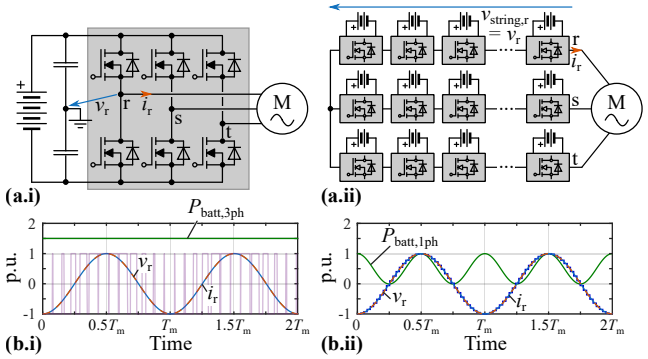

Fig. 1. (a) Circuit topology and **(b)** key waveforms of a battery-fed motor drive system using **(i)** a conventional dc-side battery and a three-phase two-level inverter or **(ii)** a battery-integrated multilevel inverter (BIMI), where each battery cell (or group of battery cells) is equipped with a switching stage, forming a module. The modules are connected in series, forming a string per phase, which can synthesize multilevel phase voltages; note that this phase modularity results in a strong low-frequency ac component of the battery power (shown for unity power factor and full-bridge modules).

Although many BIMI topology variants have emerged in recent years, such as those discussed in [1], the basic idea of equipping each module of a cascaded H-bridge (CHB) converter with a dedicated battery as shown in **Fig. 2** has been proposed already in the 1970s [2]. The field saw renewed momentum in the early 2010s, with several key publications [3]–[5] and patents [6]–[8], and has continued to evolve, particularly in the context of electric transportation, with more recent contributions from both, industry and academia, e.g., [9]–[15].

Advantages of BIMIs discussed in the literature include the use of low-cost low-voltage (LV) silicon power transistors, multilevel (ML) output voltages with low total harmonic distortion (THD), decreased stress on the motor insulation due to low dv/dt, low switching losses, fault tolerance, low-effort assembly, leveraging economies of scale, good maintainability, and the possibility to combine battery cells with different state of health [13], [14]. On the other hand, the system complexity increases significantly as isolated communication with each module is required even when powered from the local battery cells, and, depending on the topology, parallel connecting battery cells with unequal state of charge (SoC) results in high equalizing currents [16], [17]; further, the inherent ac component (at twice the output frequency) of the battery current, see **Fig. 1b.ii**, increases the battery losses, even though there

is an ongoing scientific debate regarding possible adverse or even positive effects of such an ac current component on the battery lifetime [18].

This paper provides a generic comparison between two relevant BIMI topologies and a state-of-the-art system (dc-side battery and three-phase 2L SiC inverter), regarding minimum semiconductor conduction losses under the constraint of equal semiconductor realization effort (i.e., equal embodied carbon footprint or, related, cost), and battery losses. After a brief description of the considered BIMI topologies in **Section II**, **Section III** derives an analytical expression for the minimum semiconductor conduction losses of the considered BIMI topologies, which forms the basis for the comparative evaluation described in **Section IV**. Finally, **Section V** summarizes the quantitative results and discusses further qualitative aspects before **Section VI** concludes the paper.

II. Topologies and Operating Principle

There are various realization options for the modules of a BIMI. In this paper, we consider two salient variants, i.e., a first using full-bridge switching stages (FB) as shown in **Fig. 2** and proposed in the 1970s [2], and a second using the so-called BM3 module topology shown in **Fig. 3**, which bears close structural similarity to solid-state Marx generators [19] and has been initially proposed in [4] for dynamically reconfigurable energy storage systems (without integrated dc-ac conversion) and then taken up for BIMIs in [5], [9].

In case of an FB-BIMI, each battery module[1] is equipped with four LV switches (cf. **Fig. 2**). Each module can thus generate positive and negative output voltages with the levels given by the battery module voltage, or zero volts (bypass). The required instantaneous output voltage of the string defines the number (and polarity) of the inserted battery modules, i.e., nearest-level control (NLC) is used to synthesize a stepped multilevel waveform, whereby a control system ensures permutation of the modules to balance their SoCs over time. Pulse-width modulation (PWM) of individual FB modules could be used to improve the output voltage quality compared to NLC. An advantage of the FB topology is its capability to generate bipolar voltages, which implies that the maximum required number of battery modules is essentially given by the phase voltage *amplitude* (plus some margin). On the other hand, it is not possible to connect individual modules in parallel to each other, which would allow current sharing among battery modules for lower string output voltages.

In contrast, the modules of a BM3-BIMI each contain a battery module and a switching network of just three LV power transistors, and can attain three states (bypassed, series-connected, parallel-connected) as shown in **Fig. 3b**. Accordingly, a string formed by several BM3 modules can synthesize arbitrary *positive* output voltage levels by series-

[1]Note that instead of using a single battery cell per module, clusters of several individual cells (i.e., hardwired series/parallel assemblies of individual battery cells) can be employed to scale the battery capacity (paralleling of cells), reduce the number of modules needed (series connected cells for higher module voltage), and to optimize the overall efficiency [4], [15], [20].

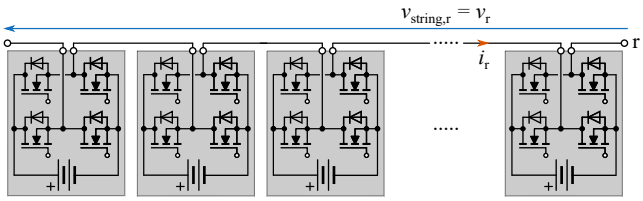

Fig. 2. Single-phase battery-integrated multilevel inverter (BIMI) with full-bridge (FB) cells, i.e., forming a cascaded H-bridge (CHB) structure as proposed in the 1970s [2].

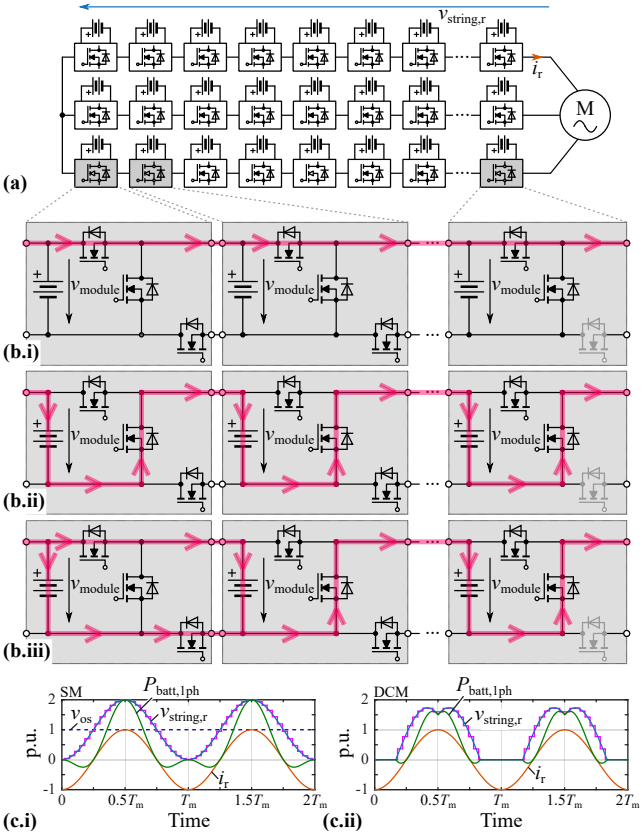

Fig. 3. **(a)** Three-phase BIMI supplying a motor, and **(b)** module configuration of a BM3-BIMI and module states: **(b.i)** bypass, **(b.ii)** series, and **(b.iii)** parallel connection. **(c)** String voltage, current (unity power factor), and power flow of one exemplary phase for **(c.i)** sinusoidal modulation (SM) and **(c.ii)** discontinuous modulation (DCM); both using nearest-level control (NLC).

connecting the required number of battery modules.[2] Compared to an FB-BIMI, thus twice as many battery modules are needed, because the maximum output voltage of a string is essentially given by twice the phase voltage amplitude if sinusoidal modulation (SM) with a dc common-mode (CM) offset equal to the phase voltage amplitude, i.e., $v_{\text{os}} = \hat{V}_{\text{ph}}$ is employed, see **Fig. 3c.i**. Further, note that **Fig. 3c.i** shows intervals with reverse power flow in the battery modules, indicating higher battery losses. Alternatively, a time-varying CM offset, i.e.,

$$v_{\text{os}} = -\min(v_{\text{r}}, v_{\text{s}}, v_{\text{t}}), \tag{1}$$

[2]As described in [21], a BM3-BIMI string can be extended by an additional full-bridge stage (commutator) to enable bipolar output voltage generation. However, the switches of this additional converter stage must essentially be rated for the full phase voltage amplitude, i.e., in addition to the BM3 modules, there are always two HV transistors in the current path. Compared to a standard 2L inverter bridge leg, such a solution is therefore uninteresting from a conduction loss point of view.

could be selected (with v_{rst} indicating the phase voltages) such that a discontinuous modulation (DCM) results, see **Fig. 3c.ii**, which advantageously reduces the maximum voltage that a string must synthesize to $\sqrt{3}/2 \cdot 2 \cdot \hat{V}_{\mathrm{ph}}$ or to 86.6% compared to SM, and further reduces the intervals of reverse power flow to the batteries (note the time intervals with $p_{\mathrm{batt,1ph}} < 0$ in **Fig. 3c**).

III. Conduction-Loss-Optimal Operation

In general, the overall conduction losses can be expressed as the sum of $R_{\mathrm{on}} \cdot i^2$ over all conducting switches. In the following, unless explicitly stated otherwise, SM without third-harmonic injection is considered.

A. Two-Level Inverter

In a 2L converter, the phase current always flows in exactly one power transistor and the per-phase conduction losses are simply $p_{\mathrm{cond}} = R_{\mathrm{on,2L}} \cdot i_{\mathrm{ph}}^2$ for any modulation scheme, where $R_{\mathrm{on,2L}}$ is the on-state resistance of the employed HV SiC MOSFET. The total conduction loss over a mains period can then simply be calculated with $P_{\mathrm{cond}} = R_{\mathrm{on,2L}} \cdot I_{\mathrm{rms}}^2$, assuming constant junction temperature and current independent on-resistance.

B. FB-BIMI

The conditions in an FB-BIMI are similar: there are always two conducting switches per module regardless of the switching state (see **Fig. 2**), and hence the per-phase conduction losses are $p_{\mathrm{cond}} = 2 \cdot N_{\mathrm{FB}} \cdot R_{\mathrm{on,FB}} \cdot i_{\mathrm{ph}}^2$, where N_{FB} is the total number of modules per string and $R_{\mathrm{on,FB}}$ is the on-resistance of the employed LV Si MOSFETs. For equal output voltage capability as a 2L inverter

$$N_{\mathrm{FB}} = \left\lceil \frac{V_{\mathrm{dc}}/2}{V_{\mathrm{module}}} \right\rfloor, \tag{2}$$

where V_{dc} is the dc voltage of the 2L inverter and V_{module} is the battery module dc voltage (assumed constant here). Again, the total conduction loss over one mains period is calculated with $P_{\mathrm{cond}} = 2 \cdot N_{\mathrm{FB}} \cdot R_{\mathrm{on,FB}} \cdot I_{\mathrm{rms}}^2$.

C. BM3-BIMI

In contrast to an FB-BIMI, a BM3-BIMI offers the possibility of also connecting modules in parallel.

1) Optimum Configurations: Specifically, for all output voltages lower than the maximum output voltage, there are some remaining modules that can be connected in parallel to other modules (see **Fig. 3b.iii**), thereby reducing the current stress of the power transistors and the battery cells. Thus, as shown in **Fig. 4**, for each output voltage level, there is at least one optimal configuration of the individual modules (series/parallel) that minimizes the overall conduction losses of the string. In the following, we thus derive analytical expressions for the minimum conduction losses of BM3-BIMIs, assuming equal battery module voltages (perfect balancing).[3]

Qualitatively, due to the dependence of the conduction losses on the sum of the device rms currents squared, minimum overall conduction losses result for configurations with as many series-connected groups consisting of equal numbers of parallel-connected modules as possible, which equalizes the current stress of the devices as much as possible, see example in **Fig. 4**.

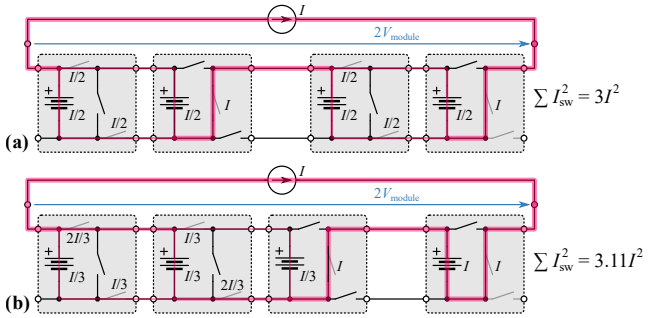

Fig. 4. Two alternative configurations of an exemplary BM3-BIMI with four modules, synthesizing an output voltage of $2V_{\mathrm{module}}$, i.e., **(a)** two groups with two parallel modules each, and **(b)** one group with three parallel modules, and a second "group" with just one module. Minimum overall conduction losses result for configurations that equalize the current stresses as much as possible, i.e., with as many groups consisting of equal number of parallel-connected modules as possible.

The derivation of the minimum achievable conduction losses starts with the notion that the desired (instantaneous) string output voltage level $v_{\mathrm{string}} = v_{\mathrm{ph}} + v_{\mathrm{os}}$ dictates the necessary number of series connected modules as

$$n_{\mathrm{s}} = \left\lceil \frac{v_{\mathrm{string}}}{V_{\mathrm{module}}} \right\rfloor, \tag{3}$$

where $\lceil \cdot \rfloor$ denotes rounding to the nearest integer.

Then, the number of remaining modules n_{p} that can be connected in parallel to the already used modules follows as

$$n_{\mathrm{p}} = N_{\mathrm{BM3}} - n_{\mathrm{s}}, \tag{4}$$

where N_{BM3} is the total number of modules per string. To ensure spreading these n_{p} modules in parallel configuration as equally as possible, the number of parallel modules p connected to each serial module is calculated by

$$p = \left\lfloor \frac{n_{\mathrm{p}}}{n_{\mathrm{s}}} \right\rfloor. \tag{5}$$

Due to the floor operation, there might be further

$$n_{\mathrm{rem}} = n_{\mathrm{p}} - (p \cdot n_{\mathrm{s}}) \tag{6}$$

remaining modules, which are then spread out equally in parallel to the first n_{rem} groups in series configuration. Thus, the the resulting configuration consists of two types of series-connected groups, i.e.:

- Group I: $n_{\mathrm{I}} = n_{\mathrm{s}} - n_{\mathrm{rem}}$ modules in series connection, each of which is connected to p modules in parallel configuration,
- Group II: $n_{\mathrm{II}} = n_{\mathrm{rem}}$ modules in series connection, each of which is connected to $p + 1$ modules in parallel configuration.

Note that a numerical grid-search method exploring all possible configurations for BM3-BIMIs with a lower number of modules has been employed to verify the analytic derivation above.

[3]Note that the control system must ensure very good balancing anyway, as otherwise significant compensation currents would flow upon parallel connection of battery modules with unequal voltages, see [16], [17].

2) Minimum Conduction Losses: The conduction losses for a given instantaneous string output voltage v_{string} (and hence n_{s}, p, n_{I}, and n_{II}) are composed of three contributions, i.e.,

$$p_{\text{s}}(v_{\text{string}}) = n_{\text{s}} \cdot i_{\text{ph}}^2 \cdot R_{\text{on,BM3}}, \tag{7}$$

where $p_{\text{s}}(v_{\text{string}})$ is the conduction loss of all modules connected in series, i_{ph} is the phase-current, and $R_{\text{on,BM3}}$ the on-state resistance of the LV Si power transistors. The losses of the switches in the parallel connected modules of group I are calculated with

$$p_{\text{p,I}}(v_{\text{string}}) = n_{\text{I}} \cdot \sum_{\text{k=1}}^{p} (k \cdot i_{\text{p,I}})^2 \cdot R_{\text{on,BM3}} \text{ with } i_{\text{p,I}} = \frac{i_{\text{ph}}}{p+1}. \tag{8}$$

The +1 in the current equation stems from the fact that for any p modules in parallel configuration that are connected with a module in series configuration, there are in fact $p+1$ modules in parallel. Similarly, the losses of the parallel switches of group II are calculated:

$$p_{\text{p,II}}(v_{\text{string}}) = n_{\text{II}} \cdot \sum_{\text{k=1}}^{p+1} (k \cdot i_{\text{p,II}})^2 \cdot R_{\text{on,BM3}} \text{ with } i_{\text{p,II}} = \frac{i_{\text{ph}}}{(p+1)+1}. \tag{9}$$

The total conduction loss $p_{\text{cond}}(v_{\text{string}})$ is then the sum of the three contributions, i.e.,

$$\begin{aligned} p_{\text{cond}}(v_{\text{string}}) &= p_{\text{s}}(v_{\text{string}}) + p_{\text{p,I}}(v_{\text{string}}) + p_{\text{p,II}}(v_{\text{string}}) \\ &= i_{\text{ph}}^2 \cdot \underbrace{R_{\text{on,BM3}} \cdot \left(n_{\text{s}} + n_{\text{I}} \sum_{\text{k=1}}^{p} \left(\frac{k}{p+1} \right)^2 + n_{\text{II}} \sum_{\text{k=1}}^{p+1} \left(\frac{k}{(p+1)+1} \right)^2 \right)}_{R_{\text{on,eq}}(v_{\text{string}})} \\ &= i_{\text{ph}}^2 \cdot R_{\text{on,eq}}(v_{\text{string}}). \end{aligned} \tag{10}$$

As shown in (10), the instantaneous (minimum) total conduction loss can be expressed by using an equivalent on-state resistance $R_{\text{on,eq}}(v_{\text{string}})$, which, however, varies with the string output voltage that determines how many modules are available for parallel connection, contributing to lowering the effective $R_{\text{on,eq}}$ of the configuration.

For each string output voltage level, there is thus at least one optimal configuration leading to minimal conduction losses. Finally, to obtain the average losses over a fundamental period, $p_{\text{cond}}(v_{\text{string}})$ from (10) must be integrated over that period (or half a period), which is best done numerically due to the nonlinearity introduced by the $\lfloor \cdot \rfloor$ operator in (5).

Note that where redundant optimal configurations exist, they can be varied throughout time to balance the battery cell SoCs [22]. Although the switching losses are considered negligible, the number of switching state changes impacts the switching losses and should thus be incorporated in any potential cell balancing algorithm. Furthermore, voltage balancing requirements may make it impossible to always utilize the minimum-conduction-loss configurations in practical applications, i.e., the conduction losses calculated in the following are an optimistic lower bound.

Assuming unity power factor operation and equal available total semiconductor area, **Fig. 5** shows that the (minimum possible) conduction losses of the BM3-BIMI decrease with lower modulation index (i.e., for lower amplitude of the phase voltage v_{ph}) as more battery modules become available for paralleling during longer phases of the mains period. However, at very low modulation indices, the conduction losses increase again for SM. This can be explained by the fact that the minimum conduction losses are achieved for parallel connections of two modules per group. While parallel connecting additional modules is still preferable to bypassing them (regarding conduction losses), the per-module losses still increase compared to the case of just two parallel connected modules per group due to the asymmetrical current distribution between the switches (see **Fig. 4**). For lower modulation indices, there is thus an increasing number of groups with more than two modules connected in parallel, leading to an increase in conduction losses.

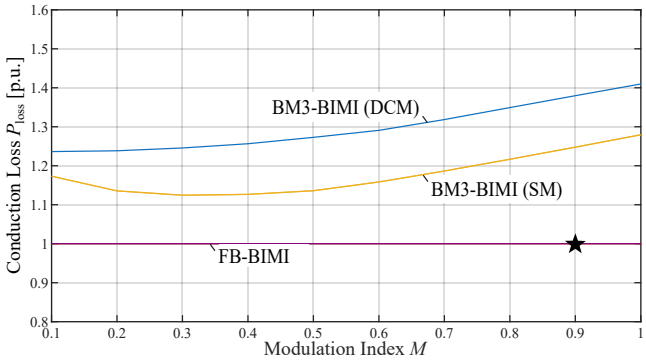

Fig. 5. Minimum conduction losses of BM3- and FB-BIMIs over a whole mains period with equal total silicon chip area for varying modulation index and fixed phase current i_{ph}; normalized to the FB-BIMI losses at the nominal operating point with $M = 0.9$ (see ★).

Interestingly, even though DCM reduces the maximum required string output voltage and thus reduces the conduction losses for high positive phase currents (more modules available for paralleling), this reduction cannot compensate the higher losses that occur during the zero-voltage-interval (cf. **Fig. 3c.ii**), where all battery cells must be bypassed (worse in terms of conduction losses than any parallel-connection) and the current magnitude is also high. In total, the minimum conduction losses achievable with DCM are always higher than with SM.

D. Comparison of FB-BIMI and BM3-BIMI

As discussed above, a BM3-BIMI requires twice the number of modules (with equal V_{module}) compared to an FB-BIMI in order to provide the same phase voltage range, i.e., $N_{\text{BM3}} = 2N_{\text{FB}}$. With four switches per battery module (three for the BM3-BIMI) but only half the modules due to the bipolar string voltage capability, the available chip area per transistor is higher for the FB-BIMI, and thus the on-state resistance $R_{\text{on,FB}}$ smaller, i.e.,

$$\frac{R_{\text{on,FB}}}{R_{\text{on,BM3}}} = \frac{A_{\text{BM3}}}{A_{\text{FB}}} = \frac{A_{\text{chip}}/(3 \cdot 2N_{\text{FB}})}{A_{\text{chip}}/(4 \cdot N_{\text{FB}})} = \frac{2}{3}. \tag{11}$$

Therefore, despite the ability to parallel battery cells at low string voltages, the BM3-BIMI always shows worse conduction losses than an FB-BIMI with the same total silicon chip area, as indicated by **Fig. 5**.

TABLE I: SYSTEM SPECIFICATIONS.

Parameter	Variable	Value	Unit
Nominal ac voltage (line-to-line rms)	v_{ac}	440	V
Nominal modulation index	M	0.9	
Max. ac frequency	f_{ac}	50	Hz
DC voltage	V_{dc}	800	V
Battery module voltage	V_{module}	16	V
Nominal output power	P_{out}	225	kW

IV. COMPARATIVE EVALUATION

Considering exemplary specifications of an EV traction battery/inverter system given in **Tab. I**, a baseline SiC 2L inverter design (based on [23]) employs 1200 V SiC power transistors with $R_{on,2L} = 4\,m\Omega$, resulting in relative nominal conduction losses of around 0.6%. The total per-phase SiC chip area used in the 2L converter is estimated as $A_{chip,SiC} = 2.45\,cm^2$ based on [24], [25].

The manufacturing of SiC devices is much more energy intense than the production of Si devices. While the cost of semiconductor dies depends on many factors, e.g., yield, waver diameter, order quantity, etc., the embodied energy can be used as a rough indication for the cost ratio, resulting in 3...4 times higher cost per chip area for SiC compared to Si [26]. Strongly related to the embodied energy, also the embodied carbon footprint or global warming potential (GWP) per chip area is correspondingly higher for SiC; specifically, [27] estimates a factor of 3.25, which we consider in the following.

Thus, for equal embodied carbon footprint (and similarly, roughly equal cost), a BIMI can use

$$A_{chip,Si} = 3.25 \cdot A_{chip,SiC} \approx 8\,cm^2. \tag{12}$$

The chip areas available per switch of an FB-BIMI and a BM3-BIMI are thus $A_{chip,Si}/(4N_{FB})$ and $A_{chip,Si}/(3N_{BM3})$, respectively. From that, the on-state resistances of the transistors can be estimated: Whereas for higher blocking voltages, the specific on-state resistance of unipolar transistors is close to the "silicon limit" [28], i.e., $R'_{on} \approx 8.3 \cdot 10^{-9} V_B^{2.5} \Omega \cdot cm^2$ with V_B denoting the blocking voltage, for $V_B < 100\,V$ the further reduction of R'_{on} saturates quickly due to the increasing relevance of resistive components from the channel, etc. that do not scale with blocking voltage. Based on literature, the lowest reported R'_{on} for devices with $V_B \approx 30\,V$ are around $0.04\,m\Omega cm^2$ [29]. With that, we find $R_{on,FB} \approx 0.5\,m\Omega$ and $R_{on,FB} \approx 0.75\,m\Omega$, resulting in roughly equal realization effort for the power semiconductors in terms of embodied carbon footprint or cost.

A. Inverter Conduction Losses

With the on-state resistances of the switches known, the minimum conduction losses for the three considered topologies are calculated as described in **Section III**. For simplicity, all calculations consider a fixed junction temperature of 100 °C to take into account the increase of on-state resistances specified for 25 °C junction temperature (by roughly +30% based on similar datasheet values); this overestimates conduction losses at lower phase currents.

For the nominal operating point (225 kW, $M = 0.9$, and 295 A rms phase current; see **Tab. I**), the conventional 2L SiC inverter shows more than a factor five lower conduction losses than an FB-BIMI, which, as discussed earlier, shows lower losses than a BM3-BIMI; this is illustrated by **Fig. 6** and **Tab. II**. Note that this conclusion holds for phase currents other than nominal as well, because the minimum conduction losses of all topologies are expressed by an (equivalent) R_{on} that does not depend on the current (it only depends inconsequentially on M for BM3-BIMIs as discussed below).

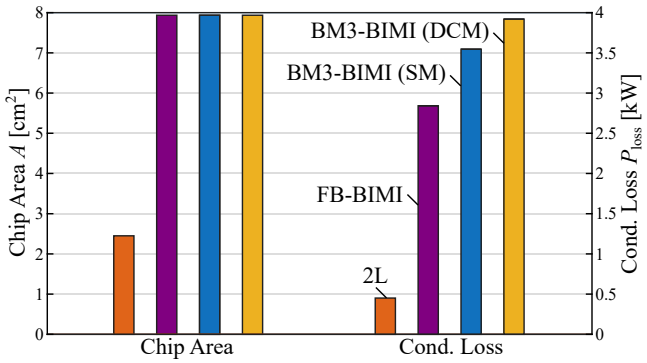

Fig. 6. Comparative evaluation results per phase, $M = 0.9$ and equal power semiconductor realization effort in terms of embodied carbon footprint and, roughly, equal cost (cf. **Tab. I**).

TABLE II: DETAILED PER-PHASE RESULTS FOR EQUAL EMBODIED CARBON FOOTPRINT OF THE POWER SEMICONDUCTORS USED IN ALL REALIZATION OPTIONS, CORRESPONDING TO **FIG. 6**.

Parameter	Variable	2L	FB	BM3		Unit
				SM	DCM	
Chip area	A	2.45	7.94	7.94	7.94	cm^2
Switch res.	R_{on}	4.00	0.51	0.75	0.75	$m\Omega$
Carbon fp.	GWP	22.2	22.2	22.2	22.2	$kgCO_2eq$
Cond. loss	P_{loss}	451	2842	3546	3920	W

Hypothetically, the described modeling procedure can also be applied in reverse, i.e., the conduction loss is kept constant. The results from **Fig. 6** and **Tab. II** clearly indicate that BIMIs achieving the same conduction losses as a 2L SiC inverter (again at the nominal operating point) would require significantly more Si chip area, resulting in clearly higher embodied carbon footprint and, consequently, also higher cost of the power semiconductors. This holds still true if the switching losses of the 2L SiC inverter are included as discussed below.

B. 2L Inverter Switching Losses

Whereas switching losses of a BIMI can be assumed to be negligible (very low switching frequency if NLC is used, very low switched voltage), this is not the case for a 2L SiC inverter. Aiming for a straightforward comparison, we approximate the switching losses from the data sheet of a suitable power module with $R_{on,SiC} = 4\,m\Omega$ [30], assuming a switching frequency of 16 kHz. The switching losses are proportional to the current and for the nominal operation point, a loss distribution of approximately 2:1 results for conduction to switching loss. As shown in **Fig. 6c** and **Tab. IIc**, even with the switching losses included, the realization effort (both, in terms of embodied carbon footprint and cost of the semiconductors) of the 2L SiC

inverter is still significantly lower if equal total losses at the nominal operating point are targeted.

To complete the picture, **Fig. 7a** compares the total losses of the 2L converter (i.e., conduction and switching losses) and the BIMIs (conduction losses only) for a fixed modulation index $M = 0.9$ and varying phase rms current, again considering equal realization effort for the power semiconductors in terms of embodied carbon footprint or cost. For low phase currents, i.e., below 45 A (or 15% of the nominal value), the BIMIs perform better than the 2L inverter due to the latter's switching losses, which is important when considering mission profiles like the worldwide harmonized light vehicles test procedure (WLTP) [31].

Whereas the conduction losses of the FB-BIMI do not depend on the modulation index (always the same number of transistors in the phase current path), BM3-BIMIs show a dependence of the conduction losses on the modulation index as discussed above in the context of **Fig. 5**. Therefore, **Fig. 7b** shows the ratio of the BM3-BIMI (using SM) conduction losses to the total losses (including switching losses) of the 2L SiC inverter over the entire phase voltage / phase current plane, indicating a slight dependence on the modulation index; however, again the 2L SiC inverter shows significantly lower losses over most of the operating range except for low phase currents.

C. Battery Losses

Finally, we provide a brief discussion of the battery losses considering a low-complexity battery model, i.e., the battery losses are modeled with an inner resistance R_{bat} for each battery module. The inherent high frequency (HF) current ripple is assumed to be filtered by adequate capacitors and in the following, only the dc or low-frequency (LF) current is considered. To allow for a fair comparison, the total number of battery modules is kept constant, independent of the required battery voltage (800 V for 2L and BM3-BIMI, and, 400 V for FB-BIMI), facilitating the parallel connection of two batteries per module of the FB-BIMI. Further, the per-phase losses are analyzed, i.e., the dc-side battery of the 2L inverter is assumed to consist of three parallel stacks, each handling one-third of the dc current. Depending on the battery cell voltage, the dc-side battery consists of a certain number of $N_{\text{bat,2L}} = V_{\text{dc}}/V_{\text{module}}$ series-connected battery modules, and the per-phase battery losses are found as

$$P_{\text{bat,2L}} = N_{\text{bat,2L}} R_{\text{bat}} \left(\frac{I_{\text{dc}}}{3}\right)^2 = \frac{V_{\text{dc}}}{V_{\text{module}}} R_{\text{bat}} \left(\frac{P_{\text{out}}}{3V_{\text{dc}}}\right)^2. \quad (13)$$

With $P_{\text{out}} = 3\hat{V}_{\text{ph}}\hat{I}_{\text{ph}}/2$ and $\hat{V}_{\text{ph}} = MV_{\text{dc}}/2$, this leads to

$$P_{\text{bat2L}} = \frac{R_{\text{bat}} V_{\text{dc}}}{16 V_{\text{module}}} \cdot \hat{I}_{\text{ph}}^2 \cdot M^2, \quad (14)$$

i.e., the battery losses decrease quadratically with decreasing modulation index as indicated in **Fig. 8**.

In an FB-BIMI, the total dc voltage is only $V_{\text{dc}}/2$ and hence each module can be equipped with *two* parallel battery modules for the same total number of battery modules as employed in the 2L (per-phase). Further, the number of inserted

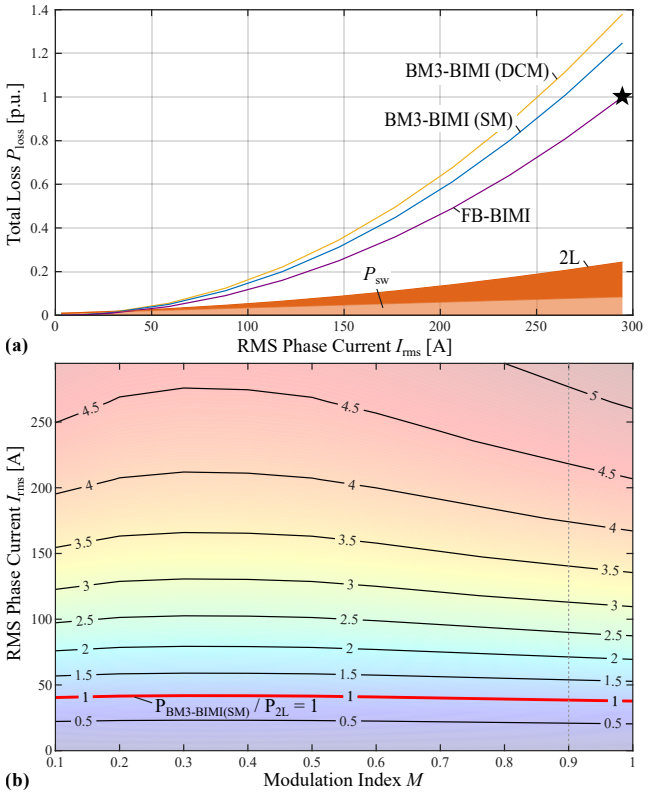

Fig. 7. **(a)** Minimum per-phase losses (including switching losses P_{sw} for the 2L inverter) of all considered topologies with equal realization effort for the power transistors in terms of embodied carbon footprint or cost, depending on the rms phase current for a modulation index of $M = 0.9$, and normalized with respect to the FB-BIMI losses at the nominal current (see ★). **(b)** Ratio of the BM3-BIMI (SM) conduction losses to the total losses (conduction and switching) of a 2L SiC inverter over the full operating area.

modules[4] is proportional to the instantaneous string output voltage (magnitude), and the string current equals the phase current, i.e.,

$$p_{\text{bat,FB}}(t) = n_{\text{ins}}(t) \frac{R_{\text{bat}}}{2} i_{\text{ph}}(t)^2 \quad \text{with} \quad n_{\text{ins}}(t) = \frac{v_{\text{string}}(t)}{V_{\text{module}}}. \quad (15)$$

Assuming unity power factor and sinusoidal modulation, i.e., $v_{\text{string}}(t) = v_{\text{ph}}(t)$ for simplicity, we have

$$\begin{aligned} P_{\text{bat,FB}} &= \frac{R_{\text{bat}}}{2V_{\text{module}}} \cdot \hat{V}_{\text{ph}} \hat{I}_{\text{ph}}^2 \cdot \left(\frac{2}{T_{\text{g}}} \int_0^{T_{\text{g}}/2} \sin^3(2\pi t/T_{\text{g}}) dt\right) \\ &= \frac{R_{\text{bat}} V_{\text{dc}}}{3\pi V_{\text{module}}} \cdot \hat{I}_{\text{ph}}^2 \cdot M, \end{aligned} \quad (16)$$

i.e., the battery losses scale linearly with the modulation index M, which is visible in **Fig. 8**.

Thus, the battery losses in an FB-BIMI with the same total number of battery cells is higher than the battery losses of a 2L inverter, specifically

$$\frac{P_{\text{bat,FB}}}{P_{\text{bat,2L}}} = \frac{16}{3\pi} \cdot \frac{1}{M}, \quad (17)$$

[4]Note that, of course, n_{ins} is an integer number in a real implementation, resulting in a staircase output voltage waveform as shown in **Fig. 1**. However, for the sake of a straightforward calculation, a continuous approximation is used here, corresponding to the assumption $V_{\text{module}} \to 0$ or, equivalently, $N_{\text{FB}} \to \infty$.

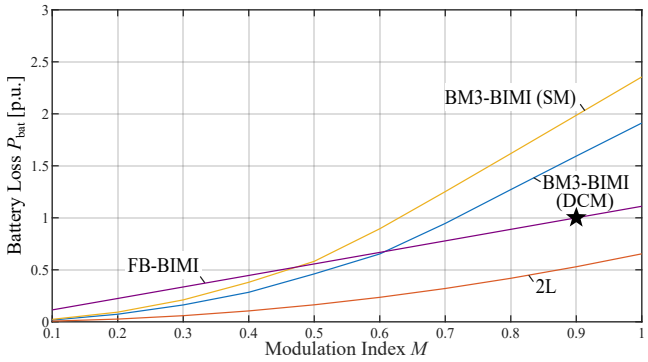

Fig. 8. Minimum per-phase battery losses depending on the modulation index and for nominal phase rms current (note that the absolute phase current does not affect the relative differences in losses); normalized to the FB-BIMI battery losses at the nominal operating point (see ★).

which evaluates to $P_{\text{bat,FB}}/P_{\text{bat,2L}} \approx 1.9$ for $M = 0.9$ and increases for smaller M.

The battery losses of a BM3-BIMI are less intuitive to calculate, as both, parallel and series connection of modules are possible. Therefore, generally, the losses decrease with lower modulation indices, as this allows to parallel more modules. Following a similar approach as discussed in **Section III** for the conduction losses, an equivalent $R_{\text{bat,BM3}}$ can be calculated and from that the total battery losses, which are also indicated in **Fig. 8**.

For modulation indices below 0.45, the BM3-BIMI with SM performs better in terms of battery losses than the FB topology. While all battery modules in the FB-BIMI always see the full phase current, this shows that paralleling battery modules is advantageous in terms of battery losses. Further, using DCM for the BM3-BIMI leads to lower battery losses compared to using SM, which is a consequence of the improved string power profile (less pronounced reverse power flow phases) as shown in **Fig. 3c**. All in all, the 2L SiC inverter still outperforms all considered BIMI variants regarding battery losses.

V. Discussion

Aiming for a clear comparison of two prominent BIMI variants with a conventional 2L SiC inverter, this paper investigates the minimum semiconductor losses for equal realization effort of the power semiconductors in terms of embodied carbon footprint, which also implies roughly equal cost due to the strong relationship between embodied energy, carbon footprint, and cost. First, FB-BIMIs show 10%...30% lower losses than BM3-BIMIs using the optimum series/parallel configurations of its modules (best-case; possibly not reachable in reality due to balancing constraints). Then, compared to the FB-BIMI, a 2L SiC inverter shows about a factor five lower losses at the nominal operating point even if including its switching losses (cf. **Section IV-B**). This comparison is based on only two assumptions: (1) The ratio of embodied carbon footprint and/or cost per chip area for SiC and LV Si power transistors is assumed as 3.25 based on literature [27]. (2) The specific on-state resistance of the LV Si transistors is assumed as $0.04\,\text{m}\Omega\text{cm}^2$ based on reported best-case values for 30 V devices [29] and on the observation that a further reduction of blocking voltage only leads to a marginal reduction of the specific on-state resistance—unlike at higher voltages, where $R_{\text{on}} \propto V_{\text{b}}^{2.5}$ ("silicon limit") [28]. However, given the difference in losses between the BIMIs and the 2L SiC inverter found herein, either of these assumptions could be off by factors without affecting the main conclusion, i.e., that a 2L SiC inverter clearly exhibits lower losses than a BIMI over a wide range of the output voltage/current plane if equal power semiconductor realization effort is considered; only for relatively low output power (< 15% nominal current) do BIMIs outperform a 2L SiC inverter due to the latter's switching losses—of course, this might be relevant for certain specific mission profiles.

It is important to note that the switching losses are influenced by the required output voltage quality, which in turn affects the harmonic losses in a connected motor or the filtering effort in grid-connected applications. Future research should include electromagnetic interference (EMI) considerations, the output voltage quality and/or motor losses in the comparative evaluation; it might turn out that, for comparable output voltage quality, a 2L SiC inverter would require a higher switching frequency than assumed herein, shifting the phase current boundary below which a BIMI shows lower overall losses to higher values. Also, for a comprehensive comparison, the switching losses of the BIMIs should be considered. Despite the low blocking voltage and switching frequency, the sheer number of switches and cell balancing requirements may lead to a non-negligible switching loss, especially at high phase currents.

Further, assuming the same total number of battery cells, we find that a 2L inverter with a dc-side battery shows only half the battery losses compared to a FB-BIMI at the nominal operating point, less for lower output voltages. These are a direct consequence of the BIMIs' inherent phase-modularity and the resulting twice-mains frequency power pulsation and does not require any other assumptions. For low modulation indices, the BM3-BIMI shows lower battery losses than an FB-BIMI due to the ability of paralleling battery modules at low output voltages, but still always higher battery losses than the 2L inverter. However, for non-ideal battery modules, high equalizing currents may flow when paralleling [16], [17], which must be avoided.

VI. Conclusion

Comparing a 2L SiC inverter with a dc-side battery against FB-BIMIs and BM3-BIMIs under the constraint of equal power semiconductor realization effort in terms of embodied carbon footprint, and roughly equivalently, cost, this paper finds that the 2L SiC inverter shows about a factor five lower losses at the nominal operating point, and the BIMIs show lower overall losses only for very small phase currents (< 15%) because of the 2L inverter's switching losses. Furthermore, BIMIs introduce a twice-mains pulsation of the battery power flow due to their phase-modular nature, which we find to result in about twice the battery losses compared to a 2L-based system at the nominal operating point (more for lower output voltages).

Of course, the aspects discussed herein are not the only ones relevant for holistically comparing the two approaches. For example, a BIMI also clearly shows higher complexity

regarding control, signal distribution to the modules requiring galvanic isolation, and, in EV applications, a difficulty to supply two independent traction motors (one per axle).

On the other hand, it is possible to extend the functional integration of the battery and the inverter forming a BIMI to include also (non-isolated) on-board charger functionality, which, however, today is not yet widely accepted. Further, the high degree of modularity of a BIMI comes with advantages regarding economies of scale and flexibility: A BIMI can deal with battery cells of different aging state and possibly even different chemistry, offer a certain fault tolerance by bypassing faulty modules, simplifies assembly and maintenance [14], and improves worker safety as no high battery voltage is present [9]. In addition, BIMIs are ideal candidates for systems where battery cell stacking is necessary, e.g., for utility-scale storage in medium-voltage applications. There is an ongoing scientific debate regarding possible adverse or even positive effects of the pulsating battery power regarding the battery lifetime [18]. Such topics should be addressed in future research aiming at a holistic comparative evaluation of these interesting BIMI concepts.

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