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Voltage/Current Measurement Performance and Power Supply Rejection in All-Digital Class-D Power Amplifiers

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Abstract— Low-noise and low-distortion voltage and current acquisition circuits, both analog and digital, are required for the control systems of precision, high-power switch-mode (Class-D) amplifiers used in nanometer-accuracy mechatronic systems. In this paper, the achievable linearity and noise of analog signal processing elements, such as sensors or active filters, is investigated and their performance in a closed-loop control system is demonstrated. Resistive voltage dividers are sufficiently linear but are subject to resistor noise. Nonetheless, a signal-to-noise ratio (SNR) of 130 dB is achievable. Shunt resistors can achieve a total harmonic distortion (THD), limited by self-heating, of $< -120 \, dB$, whereas galvanically isolated, industrial current sensors achieve an insufficient THD of \approx -90 dB. High-order active op-amp filters, which are used, e.g., to amplify and condition a shunt resistor voltage, can achieve a THD of $-120 \, dB$. Furthermore, as a subsequent signal digitization is required for the control system, it is shown how the SNR of analog-to-digital converters can be improved sufficiently for the discussed application by oversampling, and how this process affects the feedback system's phase margin. In order to reveal the performance of a closed-loop system employing the key parts of the signal acquisition components, the results of the sensor analysis are implemented in a comprehensive computer simulation model of a digitally controlled switch-mode power amplifier. The analyzed 400 V, 500 VA converter system achieves a THD <-117 dB and an SNR (DC-10 kHz) >110 dB while operating at switching frequencies up to 500 kHz.

I. INTRODUCTION

Amplifiers capable of providing high-precision (i.e., lownoise and low-distortion) voltage or current signals at frequencies from DC to several kHz are used in different applications like medical imaging, robotics or mechatronic motion systems for integrated circuit manufacturing. In the latter, such amplifiers drive single- and three-phase actuators like voice coils, magnetic bearings or linear permanent magnet synchronous machines in semiconductor wafer positioning or exposure processes with continuous output powers of up to 2 kVA [1]. Their output signal is a high-quality torque-(and hence, motion-) producing actuator current, i.e., with a signal-to-noise ratio SNR > 100 dB, and total harmonic distortion THD < $-110 \,\mathrm{dB}$, at output current fundamental frequencies from DC to $\approx 50 \,\mathrm{Hz}$ [2]. The signal quality is critical in a bandwidth from DC to 10 kHz, as the mechanical motion system provides sufficient attenuation at higher frequencies due to its inertia, which attenuates erroneous torque components.

Currently, high-power precision amplifiers are often constructed in a hybrid fashion, where the low-quality, but highpower output of a switch-mode converter is improved by a low-power linear amplifier [3]. As such setups are complex,



Fig. 1: Switch-mode amplifier system providing a high-precision output current for a three- or single-phase load. The closed-loop control system attenuates disturbances such as noise originating from the non-ideal power supply, or low-frequency harmonics generated in the switching stage.

inefficient and the dynamic interactions between the switchmode and linear amplifier are difficult to tune, a purely switchmode and digitally controlled amplifier is desired. Fig. 1 illustrates a setup of a switch-mode amplifier providing a controlled output current to a three- or single-phase resistiveinductive load, as they occur in mechatronic systems [1]. Apart from the illustrated buck-type topology, different switching stage topologies can be used, such as the dual buck topology, which can achieve lower harmonic distortion [2]. The switching stage is supplied by a non-ideal voltage source, which forms the amplifier input voltage $u_{I}(t)$ and includes a source of different disturbing spectral components, $u_{\rm NH}(t)$, and an inductive-resistive series impedance Z_{I} . In order to attenuate unwanted spectral components originating from the non-ideal supply or other sources of distortion in the amplifier's output, feedback control is commonly employed. Therefore, different system states (i.e., voltages and currents) are measured and a control law is applied. Naturally, both voltage and current measurements must provide the required performance in terms of noise, linearity and bandwidth such that the controlled signals can achieve the desired specifications, as undesired components in the sensor outputs cannot be compensated.

In Section II, it is shown how measurement circuits, such as resistive voltage dividers, shunt resistors and operational amplifier (op-amp) filter circuits can achieve sufficiently low distortion and noise for the mentioned high-precision application. Additionally, in digital control systems, where the control law is executed at regular sampling instants and computed with quantized signals, the measurements must be converted from the analog to the digital domain using analog-to-digital converters (ADCs) [4]. Such devices have a limited amplitude resolution and hence, a limited SNR [5]. However, oversam-

pling, a digital signal processing technique, can be employed to increase the SNR of an ADC, such that it is sufficient for the discussed application. The main drawback of this technique, which is an increased signal delay time, and its implications for the feedback loop performance of the control system, are investigated. **Section III** focuses specifically on the linearity and noise of different types of current sensors.

Finally, in **Section IV**, a comprehensive computer simulation model of a digitally controlled amplifier, which also incorporates the results from the voltage and current sensor analysis, is used to demonstrate the achievable power supply rejection and output signal quality. Amplifier output voltage SNR figures in excess of 110 dB and THDs of less than -115 dB are obtained. **Section V** presents a summary and an outlook. Throughout this work, the definitions of THD and SNR are identical to the ones presented in [2] and [6].

II. VOLTAGE MEASUREMENT PERFORMANCE

Voltage processing circuit elements (e.g., amplifiers, filters or ADCs) are key elements to any feedback system. This section analyzes the noise and distortion of analog voltage sensing and filtering circuits as well as ADCs.

A. Analog Voltage Sensing

Voltage signals are commonly processed with resistive dividers or op-amp circuits. Resistive dividers are used to reduce a voltage to a lower level, e.g., to measure a high-voltage signal with low-voltage processing circuit. If the power dissipation of the resistors and hence their resistance variation is kept low (i.e., several mW), such dividers can achieve a high linearity (cf. sec. III). However, resistors generate electrical noise, mainly thermal noise and excess/flicker noise, which limits the achievable SNR at the divider's output [7]. Fig. 2 exemplarily illustrates a frequency-compensated divider that allows to measure voltages up to 400 V with 3.3 V circuits, as such voltage levels occur in the investigated mechatronic amplifiers. The divider achieves an SNR of 130 dB (DC-10 kHz) at its output and its linearity is ensured by the low thermal dissipation of 10 mW per resistor [7]. The parallel capacitors are used to compensate parasitic capacitances such that the divider achieves a flat frequency response in a wide bandwidth [8].

$$U_{out} 3.2 V$$

$$U_{in} 1.2 M\Omega 1.2 M\Omega 1.2 M\Omega 1.2 M\Omega 36 k\Omega$$

$$430 V 100 pF 100 pF 100 pF 100 pF 3.3 nF$$

Fig. 2: A compensated high-voltage divider with an SNR of $130 \, dB$ and a maximum power loss of $10 \, mW$ per resistor.

If analog voltages need to be amplified for further processing, as it is, e.g., required for low (mV) voltage drops of current measurement resistors, integrated op-amps are commonly used. Their noise performance can generally be determined from their datasheets, contrary to their linearity, which depends on numerous factors such as internal construction, external circuit configuration or input and output impedances [7], [9]. Therefore, the linearity of different op-amps is evaluated experimentally. **Fig. 3** (a) illustrates the utilized non-inverting amplifier circuit. The gain is fixed at G = 20 V/V. Note that the non-inverting

configuration is more susceptible to introduce distortion than the inverting configuration, as both op-amp inputs swing with the input signal, which changes the operating point of the opamp input stage, whereas in the inverting configuration, they are fixed at $\approx 0 V$ [10].



Fig. 3: (a): Non-inverting amplifier circuit for comparing different op-amps. (b): 6^{th} order Butterworth filter with G = 1 V/V, $f_{\text{pass}} = 300 \text{ kHz}$, $f_{\text{stop}} = 2.5 \text{ MHz}$. $A_{\text{stop}} = 100 \text{ dB}$. Op-amp: *AD8620*.

Fig. 4 shows the THD at the input and output of a selection of single-ended precision op-amps. Fully-differential amplifiers are expected to perform even better [11]. For this measurement, a low-distortion signal generator as well as high-resolution spectrum analyzer is required [9], [12]. For amplifier input voltages $V_{\rm in} < 0.3$ V, a THD of the amplified signal below 110 dB can be achieved. Note that the output THD can be below the input THD in such a measurement, as two nonlinear systems (the signal generator and the amplifier) are connected in series, i.e., the harmonics already present in the input signal can cancel the harmonics introduced by the nonlinearities of the op-amp [9], [13].



Fig. 4: Comparison of low-distortion op-amps. Fig. 3 (a) illustrates the circuit. THD is measured at the amplifier output and includes the first 5 harmonics. The input signal is provided by a low-distortion sine generator. The prominent increase in THD shown by some op-amps at higher output levels is due to limited op-amp output swing capabilities. Signal source and spectrum analyzer is a *Rohde&Schwarz UPV*.

Op-amp circuits are also used in analog filters. **Fig. 3** (b) exemplarily illustrates a 6th order Butterworth low-pass filter implemented with a multi-feedback (MFB) filter topology. With regards to distortion, the MFB topology is better suited than the also widely used Sallen-Key filter topology, as the op-amps are in the inverting configuration [10]. Such a filter can be used as the analog anti-alias filter of an ADC, and hence, it should add only little distortion or noise to the signal. **Fig. 5** illustrates the THD and SNR at the input and output of the filter for different amplitudes and frequencies. The filter adds $\approx 5 \, dB$ to the THD at its output over a wide operating range. On the other hand, the SNR is nearly identical at the input and output.



Fig. 5: THD and -SNR at the output of the MFB low-pass filter (cf. Fig. 3 (b)). THD includes the first 9 harmonics and SNR is evaluated from 100 Hz to 20 kHz. The frequency for the input voltage sweep is 1 kHz and the input RMS amplitude for the frequency sweep is 2 V. The plot lines are slightly smoothed using spline interpolation. The decrease in SNR at ≈ 3.5 V is due to a range switch in the source.

The presented analyses demonstrate the performance with respect to linearity and noise of common analog voltage processing elements, which are also required in conjunction with digital signal processing circuits (e.g., ADC anti-aliasing filters). In the following section, the performance of ADCs is investigated.

B. Digital Voltage Sensing

Analog-to-digital converters quantize an analog voltage signal to obtain a digital signal with an amplitude resolution of mbits (2^m quantization levels) at a (constant) sampling rate f_S . Due to the limited amplitude resolution, wideband quantization noise is added to the digitized signal which limits its SNR [5], [6]. The SNR in a frequency band from DC to $f_S/2$ of an amplitude quantized sinusoidal digital signal with a resolution of m bits can be approximated by [5]

$$SNR = 6.02m + 1.76 \text{ dB.}$$
 (1)

However, ADC devices show SNR figures (SNR_{ADC}) worse than what eq. (1) suggests, due to additional noise sources and fabrication constraints of integrated circuits. **Tab. I** lists the THD and SNR of selected high-resolution ADCs as stated in their datasheets.

Part	Bits m	$f_{\rm S}$ (MHz)	THD (dB)	SNR_{ADC} (dB)	<i>SNR</i> (eq.(1), dB)
ADS1675	24	2	-103	97	146.2
ADS9110	18	2	-118	100	110.1
AD7960	18	5	-117	99	110.1
AD7961	16	5	-116	95.5	98
AD7915	16	1	-118.5	94	98

TABLE I: Datasheet performance of selected precision ADCs. SNR is measured from DC to $f_{\rm S}/2$.

Fig. 6 (a) and (b) illustrate the basic analog-to-digital conversion system, whose goal it is to replicate signals in the frequency band from DC to $f_{\rm B}$ (the baseband). It operates with a sampling rate $f_{\rm S} = f_{\rm NS}$, which is close to the Nyquist frequency of $2f_{\rm B}$, and the resulting SNR is limited to $SNR_{\rm ADC}$.

In order to prevent unwanted signal components due to aliasing, an analog low-pass filter (LPF) with an attenuation A at $f_{\rm NS}/2$, that exceeds the ADCs dynamic range, is placed at the input of the ADC [5]. The sampling frequency must be slightly higher than $2f_{\rm B}$ such that the anti-aliasing filter can roll off in the frequency interval from $f_{\rm B}$ to $f_{\rm NS}/2$. The quantization noise (due to the limited amplitude resolution of m bits) is evenly distributed in a band from DC to $f_{\rm NS}/2$ (cf. eq. (1)).



Fig. 6: Two ADC sampling strategies. (a): Nyquist-sampling with $f_{\rm NS}$. (b): Spectrum with Nyquist-sampling. (c): Oversampling at $f_{\rm OS} > f_{\rm NS}$ increases the resolution and lowers the order of the analog filter. (d): Spectrum of an oversampled ADC system. The quantization noise energy is spread over a wider bandwidth.

If the SNR of a given ADC is insufficient, oversampling, where $f_{\rm S}$ is chosen higher than necessary, can be employed to increase the measured signal's SNR [5]. Fig. 6 (c) and (d) illustrate this approach. As the sampling frequency $f_{\rm S} = f_{\rm OS}$ is now higher, the energy of the quantization noise is spread over a larger bandwidth (from DC to $f_{\rm OS}/2$) and hence, the SNR in the baseband increases. Furthermore, the analog lowpass filter can roll off in a wider band and can thus be of a smaller order, requiring less components (e.g., op-amps), which reduces signal distortion and noise (cf. sec. II-A). However, as the subsequent processing system still operates at the lower frequency $f_{\rm NS}$, which is, e.g., a power converter's fixed PWM frequency, the ADC's sampling frequency f_{OS} must be reduced (downsampling). In order to achieve this, the digital signal must be low-pass filtered by a decimation filter in order to prevent spectral aliasing components in the output signal, before the sampling rate can be reduced [14]. Afterwards, the digital signal has a higher resolution of n > m bits, that corresponds to an increased SNR_{OS}, which, for an oversampling ratio $(OSR = f_{OS}/f_{NS})$, is given by

$$SNR_{\rm OS} = SNR_{\rm ADC} + 10\log_{10}(OSR) \,\mathrm{dB},\tag{2}$$

which holds from DC to $f_{\rm OS}/(2OSR) = f_{\rm NS}/2$ [5]. The disadvantage of the oversampling technique is the phase lag introduced to the measured signal by the digital decimation filter, which, if it is part of a feedback loop, is detrimental for the loop's stability margins. This phase lag is further investigated in the following.

1) Digital Decimation Filter Delay: The digital decimation low-pass filter in an oversampled ADC system, which, ideally, provides an attenuation of $A > SNR_{OS}$ at $f_{OS}/(2OSR)$ in order to fully prevent aliasing, can show a considerable phase lag [14]. Digital IIR filters are preferred for this application as they can realize a given filter specification with less stages than FIR filters and consequently, they show a smaller phase lag, which, at low frequencies (i.e., in the baseband), increases nearly linear with frequency. Thus, in the following, their performance is assessed by the constant signal delay $T_{\rm IIR}$ corresponding to this linear phase.



Fig. 7: Oversampled SNR and the delay of digital decimation filters for different (integer) OSR. The colored points are for a 16 Bit, 5 MHz ADC. The dashed lines are the Pareto fronts of different ADC configurations.

In Fig. 7, different digital IIR low-pass filter implementations, operating at different OSR, are compared with respect to their delay [14]. The amplitude resolution and sampling rate f_{OS} of the oversampled system are given by a certain ADC, e.g., 16 Bit and 5 MHz. Consequently, SNR_{OS} can be evaluated according to eq. (2) for different OSR (different $f_{\rm NS}$), with the assumption that $SNR_{\rm ADC}$ follows eq. (1). The low-pass decimation filters must provide an attenuation A_{stop} of at least SNR_{OS} at $f_{stop} = f_{OS}/(2OSR)$. However, lower stopband attenuations also sufficiently suppress aliasing components [14]. For this analysis, A_{stop} is fixed at 80 dB. The passband frequency f_{pass} is allowed to range from $20\,\mathrm{kHz}$ to $f_{\rm stop}$. In order to restrict the filter complexity, only filter orders up to 30 are allowed. The passband ripple (where applicable) is set to $0.0001 \,\mathrm{dB}$. The resulting filter delay T_{IIR} is plotted for every viable filter configuration. Each plotted point in Fig. 7 corresponds to a possible filter for a 16 bit, 5 MHz ADC, operating at different OSR. The Pareto front for this ADC configuration, as well as for different sampling configurations as indicated, are plotted with dashed lines.

The analysis shows how, with a rising OSR (and hence, a rising SNR_{OS}), the delay of the filter increases. The *Chebyshev Type 2* filters offer the best performance while also featuring no passband ripple [14]. Note that the resulting filter complexities are considerable, with orders up to 30, and thus require digital processing systems that are capable of implementing such filters (e.g., FPGAs). In sec. IV, the filter delays as investigated here are considered in the analysis of a feedback system, which reveals the impact on the feedback loop performance.

III. CURRENT MEASUREMENT PERFORMANCE

This section analyzes the linearity and noise of different types of current sensors as they are commonly used in power electronics converters. A shunt resistor provides a simple means of measuring a current, as the voltage drop across it is, ideally, proportional to the resistor current $i_{\rm S}$. However, as the resistance $R_{\rm S}$ is nonzero and many resistive materials show a temperature dependence of $R_{\rm S}$, the shunt voltage $u_{\rm S} = R_{\rm S} i_{\rm S}$ is a function of the associated momentary thermal loss $p(t) = R_{\rm S} i_{\rm S}(t)^2$, as it alters the shunt's temperature $T_{\rm S}$ [15]. Consequently, the resistor's linearity depends mainly on the temperature coefficient α , i.e., $R_{\rm S} = R_{\rm nom}(1 + \alpha(T_{\rm S} - T_{\rm a}))$, with $T_{\rm a}$ being the ambient temperature, as well as the thermal impedance $Z_{\rm S}$ of the resistor, which defines its temperature in dependence of the momentary thermal power loss p(t): $T_{\rm S} =$ $Z_{\rm S}p(t) + T_{\rm a}$. Using this set of equations, the shunt voltage $u_{\rm S} = R_{\rm S} i_{\rm S}$ is

$$u_{\rm S}(t) = \frac{R_{\rm nom} i_{\rm S}(t)}{1 - \alpha R_{\rm nom} Z_{\rm S} i_{\rm S}^2(t)}.$$
(3)

If a sinusoidal current $i_{\rm S}(t) = \hat{i} \sin(\omega t)$ is assumed, then the THD of $u_{\rm S}$ can be numerically derived from eq. (3). Using $Z_{\rm S} = 2 \,{\rm K} \,{\rm W}^{-1}$, $\alpha = 2 {\rm e}^{-6}$, $R_{\rm nom} = 10 \,{\rm m}\Omega$ and $\hat{i} = 10 \,{\rm A}$, which are values achieved by commercial shunt resistors [16], the resulting THD of $u_{\rm S}$ is $-120 \,{\rm dB}$. A lower value for $R_{\rm nom}$ further improves the THD. However, subsequent amplifiers used to process $u_{\rm S}$ then require more gain which could result in more distortion originating from these circuits. Note that α and $Z_{\rm S}$ are usually not constant, as they can also vary with temperature and time. Nonetheless, this analysis shows that shunt resistors can provide a sufficiently high linearity in current ranges up to $\approx 10 \,{\rm A}$, as it is required for the investigated mechatronic current amplifiers.

If a galvanically isolated current measurement is required, commonly used sensors, which provide an output voltage or current signal and frequently include integrated processing electronics, often rely on magnetic effects [17]. Unfortunately, there is typically no distortion data of such sensors available and hence, a precision current source is used in the following to investigate the THD of different types of galvanically isolated current sensors, as listed in **Tab. II**.

Nr.	Technology	Output Type	$I_{\rm nom}$ (A _{RMS})	$f_{\rm BW}$ (kHz)	Linearity (% I _{nom})
$ \begin{array}{c} 1 \\ 2 \\ 3 \\ 4 \\ 5 \\ 6 \end{array} $	AMR, CL AMR, CL Hall, OL Hall, CL Hall, CL Fluxgate, CL	Voltage Current Voltage Voltage Current Current	15 15 20 15 25 60	200 400 50 200 200 800	$\begin{array}{c} \pm 0.1 \\ \pm 0.2 \\ \pm 1 \\ < 0.1 \\ < 0.2 \\ \pm 0.0001 \end{array}$

TABLE II: Galvanically isolated current sensors with different sensing principles such as the anisotropic magnetoresistive effect (AMR) or open/closed-loop (OL/CL) circuits involving Hall sensors. The fluxgate principle excites a magnetic core and utilizes its saturation in combination with a compensation principle [17]. $f_{\rm BW}$ is the sensor's bandwidth. Linearity is the integral nonlinearity error, i.e., the max. deviation from the ideal transfer curve.

Fig. 8 depicts the schematic of the low-distortion current source. An industrial voltage amplifier (*AE Techron 7224*) is

used to drive the reference current i_{Ref} . A feedback system, composed of a reference shunt R_{Ref} (*Burster 1282*, 10 m Ω) and a Type-III (lead-lag) compensator, is used to attenuate harmonics in i_{Ref} originating from the non-ideal power amplifier. R_{L} is used to bias the power amplifier into a suitable operating point (i.e., stable and low harmonics). The low-distortion reference signal u_{Ref} is provided by the high-precision measurement system, which is also used to analyze the amplified shunt voltage $u_{\text{S},\text{A}}$ and the current sensor's output voltage u_{Sens} [12].



Fig. 8: Precision current source. U_1 operates as a Type-III compensator. U_2 provides the amplified feedback signal $u_{S,A}$. All op-amps are *LT1028A*.

Fig. 9 illustrates the THD (first 4 harmonics) and SNR (100 Hz-20 kHz) of the different sensor output voltages (u_{Sens}) as a function of the measured current, at a fundamental frequency of 35 Hz. The measurement shows that the investigated current sensors can only achieve a THD of \approx -90 dB, whereas their output noise is also significantly increased. The same current source was also used to investigate shunt resistors. As expected, no increase in THD or SNR in the shunt output voltage can be observed. Consequently, if currents are to be measured with low sensor-induced distortion, as required by the discussed mechatronic application, shunt resistors deliver a superior performance over integrated, galvanically isolated sensors.

In the following, the obtained results from the voltage and current sensor analysis are incorporated in a simulation of a controlled converter system to investigate the overall achievable converter output noise and distortion.



Fig. 9: THD and -SNR of different galvanically isolated current sensors as listed in **Tab. II**. A low-distortion current source (cf. **Fig. 8**) supplies the reference current (measured as $u_{S,A}$).

IV. POWER SUPPLY REJECTION AND CLOSED-LOOP PERFORMANCE

The supply of a power amplifier is usually not ideal, as there is often wideband noise or grid harmonics present in the supply voltage's spectrum. Additionally, there is a series impedance Z_I , which causes a current dependency of the supply voltage $u_I(t)$. The amplifier is required to sufficiently attenuate any supply distortion components at its output, and, in order to avoid harmonic distortion, it must compensate for a drooping supply voltage [2]. Precision amplifiers often consist of a combination of a switch-mode power converter and a linear amplifier. Such hybrid concepts benefit from the high efficiency of the switchmode converter, whereas the output quality is improved by the linear amplifier. There are different circuit topologies of hybrid amplifiers [3], [18].

Fig. 10 (a) illustrates a hybrid amplifier structure which delivers a precision output current. The non-ideal supply of the switch-mode amplifier is modelled as an ideal voltage source $U_{\rm DC}$ in series with a voltage source $u_{\rm NH}(t)$ that supplies noise and different unwanted spectral components such as grid harmonics, and a resistive-inductive series impedance Z_{I} . The linear amplifier is used, together with a precision current sensor, to attenuate the ripple and other unwanted components in the output current $i_{\rm O}$. As the switch-mode stage delivers the most output current, the linear amplifier can operate at a lower power level. This facilitates the design of a low-noise power supply $U_{\rm A}$ for the linear power amplifier. If the switch-mode converter already delivers an output of sufficiently high performance, the hybrid approach depicted in Fig. 10 (b) can be employed [19]. Here, the linear amplifier simply provides a stabilized supply voltage $U_{\rm S}$ for the switch-mode power amplifier.



Fig. 10: Two hybrid amplifier structures. (a): The linear power amplifier attenuates undesired current components in the output current. (b): The linear power amplifier provides a stabilized, low-noise supply voltage $U_{\rm S}$ for the precision switch-mode power amplifier.

Linear power amplifiers (together with analog control) can achieve a high loop gain over a wide bandwidth which makes them well suited to attenuate distortion components. However, their efficiency is limited and consequently, their usage is restricted to low output powers [3]. Furthermore, the combined action of the control systems of the switch-mode amplifier and the linear stage must be well tuned in order to ensure control stability over a wide operating range [20].

Consequently, this work proposes the use of only switchmode conversion stages. Fig. 11 illustrates a possible concept, in which a switch-mode supply filter provides a stabilized and adjustable supply voltage $U_{\rm S}$ for the switch-mode amplifier,



Fig. 11: A precision switch-mode converter provides a stabilized, filtered supply voltage $U_{\rm S}$ for the switch-mode power amplifier which delivers the precision output current $i_{\rm O}(t)$.

which provides the high-precision output current $i_{\rm O}$. Using this approach, the supply voltage of the power amplifier can be varied and hence, its performance can be adapted for different operating conditions, e.g., if high output dynamics are required, $U_{\rm S}$ can be increased whereas the remaining switching components in $i_{\rm O}(t)$ can be reduced by lowering $U_{\rm S}$. However, depending on the application, the switch-mode amplifier stage alone could provide sufficient power supply rejection and dynamic performance and thus, the switch-mode supply filter converter would not be required.

Due to the advent of WBG semiconductors, especially gallium nitride (GaN) enhancement FETs [21], which enable high switching frequencies and thus high controller sampling rates, the control system of switched converters can achieve the desired performance, as shown in the following. If a (voltage/current) controller crossover frequency of $5 \text{ kHz} \dots 20 \text{ kHz}$ is targeted for a mechatronic amplifier, the sampling rate of the control system, which is the converter switching frequency $f_{\rm PWM}$, must be $\approx 100 \text{ kHz} \dots 600 \text{ kHz}$ in order to achieve a high control performance [4].

In order to demonstrate the feasibility of this power supply rejection approach, a detailed circuit simulation model of a low-noise and low-distortion switch-mode amplifier has been developed. The simulation system also incorporates realistic sensing technology models as they were investigated in the foregoing sections in order to reveal achievable performance figures of the discussed amplifier.

A. Digitally Controlled Converter Performance

A circuit simulation is used which models a realistic switching stage as well as the digital controllers and important non-idealities and noise sources [22]. **Fig. 12** illustrates the simulation setup and the proposed control structure, composed of two cascaded controllers, which is expected to deliver a high performance [23]. The system is operated as a DC to AC converter, which allows the assessment of the harmonic distortion contribution originating from the switching stage of the converter, which is not possible for a DC output. **Tab. III** lists the configuration of the simulation model.

For the power stage, a conventional buck converter is used, although this topology is expected to generate a considerable amount of harmonics due to the dead time interval required when changing the switching state of the two transistors (T_1 , T_2) to prevent a bridge leg shoot-through [2]. Nonetheless, it is employed here in order to demonstrate the distortion attenuation capability of the control system. In order to reduce the complexity of the simulation model, only a single-phase system with one switching leg is considered, whereas a singlephase load is usually connected to two switching legs in order



Fig. 12: Simulation model block diagram. The ADCs, the analog and digital filters, as well as the time-discrete controllers are modelled in detail and include important noise and distortion sources.

to increase the available voltage at the load and to reduce power supply interaction [24]. In this analysis, the second half-bridge is modeled as a constant voltage source $U_{\rm DC}/2$.

The voltage and current measurement ADCs have a resolution of 16 bit and are operated using oversampling in order to increase their SNR. Noise of uniformal spectral distribution is added at the ADC outputs such that it matches the noise level of the AD7961 (SNR_{ADC} = $95.5 \,\mathrm{dB}$). Additionally, distortion is created at the output of the ADC with a function $y = 1x + A_3 x^3$, with the coefficient A_3 designed such that a THD of $-116 \,\mathrm{dB}$ (at full scale input) results, as it is the case with the considered ADC (AD7961). As shown in sec. II and III, shunt resistors, voltage dividers and active analog filters can achieve a higher THD than the ADC and are thus considered as ideally linear. The analog low-pass anti-aliasing filters and the digital decimation filters are implemented in the digital simulation using the IIR filter topology and secondorder-sections, in order to ensure their numerical stability [14]. The analog anti-aliasing filter is a Butterworth filter with a pass band frequency $f_{\rm p,AA}$ selected as high as possible in order to minimize its phase delay, but with the filter order being fixed to 6, such that the complexity of the analog filter (and thus, its distortion and noise) is limited (cf. sec. II-A). The stop band attenuation is 98 dB and the stop band frequency is $f_{\rm S,ADC}/2$. The digital decimation filter is a Chebyshev Type 2 filter and selected according to the optima for each OSR as derived in Fig. 7, i.e., with the pass band frequency $f_{p,Dec}$ as high as possible in order to minimize $T_{\rm IIR}$, without exceeding the maximum filter order of 30. The lower stop band frequency of this filter is $f_{\mathrm{S,ADC}}/(2OSR)$ and the stop band attenuation is fixed to 80 dB.

The digital noise shaper structure as described in [6] is employed in order to achieve a high PWM signal SNR with the given $f_{\rm PWM}$, while limiting digital PWM counter frequencies to ≈ 250 MHz, as this frequency is constrained by digital logic. This noise shaper is, despite using a low-resolution PWM modulator, capable of generating high-SNR modulation signals in the baseband (DC-10 kHz).

The switching transistors are modeled with a constant drainsource capacitance $C_{\rm DS}$, a constant channel resistance $R_{\rm DS,on}$ and a body diode forward drop of 3 V, which can be expected from GaN transistors [2]. For simplicity, the gate drivers are assumed ideal, i.e., the switches turn on and off ideally fast (note that the drain-source capacitance $C_{\rm DS}$ nonetheless ensures

Name	Parameter	Value			
$R_{\rm DS,on}$	HEMT channel resistance	$80\mathrm{m}\Omega$			
$u_{ m F}$	HEMT body diode fwd. drop	$3\mathrm{V}$			
$\bar{C}_{\rm DS}$	HEMT drain-source capaci-	$100\mathrm{pF}$			
	tance				
$T_{\rm D}$	Half-bridge dead time	$50\mathrm{ns}$			
$R_{\rm LF}$	Series resistance of $L_{\rm F}$	$50\mathrm{m}\Omega$			
$C_{\rm LF}$	Parasitic capacitance of $L_{\rm F}$	$100\mathrm{pF}$			
$C_{\rm F}$	Filter capacitor	$27\mu\mathrm{F}$			
$R_{\rm ESR}$	Series resistance of $C_{\rm F}$	$20\mathrm{m}\Omega$			
$U_{\rm DC}$	DC-link voltage	$400\mathrm{V}$			
$u_{\rm NH}(t)$	Noise and harmonic source	See text.			
Z_{I}	Supply series impedance	$0.1 \Omega + 100 \mathrm{nH}$			
$u_{\rm Ref}(t)$	Output voltage reference	$\frac{U_{\rm DC}}{2} + 0.8 \frac{U_{\rm DC}}{2} \sin(2\pi 40t)$			
$R_{ m L}$	Load resistance	- 30 Ω			
$m_{ m ADC}$	ADC resolution	16 Bits			
SNR_{ADC}	ADC SNR, from AD7961	$95.5\mathrm{dB}$			
THD_{ADC}	ADC THD, from AD7961	$-116\mathrm{dB}$			
$u_{ m ADC}$	Voltage ADC range	0V430V			
$i_{ m ADC}$	Current ADC range	-50A50A			

TABLE III: Circuit simulation setup. These values are identical in all simulations. The transistors are modelled after E-mode GaN HEMT.

a nonzero transition time of the switched half-bridge voltage). In order to realize high $f_{\rm PWM}$ and thus also high controller execution frequencies, the output power is set to $\approx 500 \,\mathrm{W}$, which is expected to allow switching frequencies up to several hundred kHz without excessive transistor switching losses [21].

The output filter capacitance $C_{\rm F}$ is chosen such that the power factor at the half-bridge output is $\lambda > 0.98$, whereas the output filter inductance value $L_{\rm F}$ is designed such that the maximum current ripple (peak-peak) in the inductor is $\approx 10 \%$ of the RMS output current of 4.2 A (cf. **Tab. III**). Electromagnetic interference is not considered in this simulation. A second filter stage would be required to further provide high-frequency attenuation.

Two cascaded controllers are utilized (cf. **Fig. 12**). For the current controller, a lead compensator is used (cf. eq. (4)), whereas the output voltage $u_{\rm O}$ is controlled by a Type-III (lead-lag) compensator (cf. eq. (5)).

Both controllers are tuned to provide a phase margin of at least 50° and a gain margin of more than 7 dB. They are implemented as time-discrete controllers and executed with $f_{\rm PWM}$. The reference output voltage and the measured output voltage are used as feedforward terms to improve the controller's dynamic behavior [25].

$$G_{\text{Lead}} = A_{\text{DC}} \frac{1 + \frac{s}{\omega_z}}{(1 + \frac{s}{\omega_{r1}})(1 + \frac{s}{\omega_{r2}})}$$
(4)

$$G_{\text{TIII}} = A_{\text{DC}} \frac{\left(1 + \frac{\omega_{\text{L}}}{s}\right)\left(1 + \frac{s}{\omega_{\text{z}}}\right)}{\left(1 + \frac{s}{\omega_{\text{trans}}}\right)\left(1 + \frac{s}{\omega_{\text{trans}}}\right)}$$
(5)

The supply consists of a series-connection of an ideal voltage source $U_{\rm DC} = 400 \,\mathrm{V}$ and a source $u_{\rm NH}(t)$ which provides wideband noise and other spectral components. The spectrum of $u_{\rm NH}(t)$ is modeled to represent the spectra of different switch-mode laboratory supplies with output powers of $1 \,\mathrm{kW}$ to $10 \,\mathrm{kW}$. Its spectrum is illustrated in Fig. 13.

Tab. IV lists individual simulation configurations and their results. Apart from the THD and SNR, the signal-to-noise-and-distortion-ratio (SINAD) is also provided, which is similar



Fig. 13: Voltage spectra of the supply $(U_{\rm DC} + u_{\rm NH}(t))$, including wideband noise and different spectral spurs, and the amplifier output. Switching frequency $f_{\rm PWM} = 500 \, \rm kHz$, ADC sampling rate $f_{\rm S,ADC} = 5 \, \rm MHz$. $SNR = 110.2 \, \rm dB$, $THD = -117.6 \, \rm dB$.

to the SNR, except that the power of the harmonics is also considered [5]. **Fig. 13** also illustrates the spectrum of the amplifier output for $f_{\rm PWM} = 500 \,\rm kHz$ and $f_{\rm S,ADC} = 5 \,\rm MHz$. It shows that the spectral components and noise originating from the supply are significantly attenuated ($A > 40 \,\rm dB$) by the converter and only the harmonics of the fundamental remain. The sensitivity of the amplifier output to the supply voltage could be even further ameliorated by measuring the supply voltage and using it as a feedforward term for the control system [26].

The results show that oversampling improves the amplifier output noise, as the SNR of the sensors is improved. Furthermore, an increased switching frequency enables a higher voltage controller open-loop crossover frequency $f_{c,u}$ (frequency where the open-loop gain becomes 0 dB), which allows a better attenuation of disturbing harmonics and noise by the feedback system. Despite using an inferior converter topology (conventional buck converter instead of a dual buck converter), the remaining noise and distortion at the amplifier output is compellingly attenuated by the digital feedback system.

In this analysis, the spectrum of the output voltage at a resistive load is investigated. If this output voltage were applied to a resistive-inductive load, as they are common for mechatronic actuators, noise and distortion in the output current would be even lower, due to the increasing load impedance with frequency.

Although the simulations are performed with an output power of <500 VA, the addition of a second switching leg, as it is usually done for single-phase loads, will double the achievable load voltage. Furthermore, by interleaving several switching legs and operating them with a phase-shifted modulation carrier, the output power, as well as the effective output ripple frequency, can be further increased [25].

V. CONCLUSION & OUTLOOK

This paper reveals the noise and distortion performance of voltage and current acquisition elements, both analog and digital, as they are important for the feedback control systems of low-noise and low-distortion power amplifiers used in mechatronic applications.

It is shown how resistive high-voltage (400 V) dividers, as well as analog amplifiers and active filters employing operational amplifiers, can achieve very low noise and distortion

$f_{\rm PWM}$ (kHz)	$f_{ m S,ADC}$ (MHz)	OSR ()	n _{PWM} (Bit)	$L_{ m F}$ ($\mu { m H}$)	$f_{ m p,AA}$ (kHz)	$f_{ m p,Dec}\ (m kHz)$	$T_{ m IIR}$ (µs)	$f_{ m c,u}$ (kHz)	THD (dB)	SNR (dB)	SINAD (dB)
100	1	10	10	2400	80	49	18.8	2.2	-108.2	104.3	102.8
100	2	20	10	2400	160	46.5	20	2.4	-116.3	106.5	106.1
100	5	50	10	2400	380	45	20.8	2.7	-115.1	108.3	107.5
250	1	4	9	1000	80	122	7.1	4.3	-116.1	101.8	101.6
250	5	20	9	1000	380	112	8.0	6.0	-118.0	108.7	108.2
500	1	2	8	470	80	253	2.9	5.7	-113.8	100.9	100.7
500	5	10	8	470	380	205	4.0	9.0	-117.6	110.2	109.5
750	1	1	7	330	80	n/a	0	5.5	-110.8	100.4	100.0
750	5	6	7	330	380	370	2.4	14.2	-117.1	112.6	111.3

TABLE IV: Simulation results. SNR and SINAD are measured from DC to 10 kHz and the THD considers the first 5 harmonics.

figures. It is demonstrated that a 6th order analog anti-alias filter can show a THD $< -120 \, \text{dB}$.

A high-precision current source is used to investigate the performance of different types of galvanically isolated, industrial current sensors, both in terms of noise and distortion. The best achieved THD is $-90 \,\mathrm{dB}$, which is insufficient for the discussed application. Therefore, shunt resistors, which can provide a very low-distortion (THD < -120 dB) and low-noise current measurement, are preferred.

Furthermore, by employing oversampling, the SNR of ADCs can be sufficiently increased and enables digital control in ultra low-noise applications.

Finally, these results are incorporated in an extensive computer simulation model which employs all main nonlinearities and noise sources, in order to demonstrate the feasibility and performance of a digitally controlled, switch-mode power amplifier operating with a non-ideal supply. The presented system achieves a high power supply rejection ratio (> $40 \, \text{dB}$), and, despite using an inferior switching stage topology (conventional buck converter), the resulting output voltage THD is below -117 dB at output powers of 500 W. Voltage SNR figures in excess of $110 \, dB$ are also achieved. The use of an interleaved topology can increase the output power as well as the effective switching frequency, leading to a more dynamic system behavior.

In summary, based on the proposed digitally controlled switch-mode amplifier, it is shown how low distortion, low noise and a high power supply rejection can be achieved. This obviates more complex hybrid amplifier topologies, leading to more efficient and cost-effective solutions. A hardware demonstrator will be used for verification in subsequent research work.

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