VIENNA Rectifier II – A Novel Single-Stage High-Frequency Isolated Three-Phase PWM Rectifier System

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Abstract – Based on an analysis of basic realization possibilities the structure of the power circuit of a new single-stage three-phase boost-type PWM rectifier system (VIENNA Rectifier II) is developed. This system has continuous sinusoidal time behavior of the input currents and high-frequency isolation of the output voltage which is controlled in a highly dynamic manner. As compared to a conventional two-stage realization, this system has substantially lower complexity and allows to realize several isolated output circuits with minimum effort.

The basic function of the new PWM rectifier system is described based on the conducting states occurring within a pulse period. Furthermore, a straightforward space vector oriented method for the system control is proposed which guarantees a symmetric magnetization of the transformer. Also, it makes possible a sinusoidal control of the mains phase currents in phase with the associated phase voltages. By digital simulation the theoretical considerations are verified and the stresses on the power semiconductors of the new converter system are determined. Finally, problems of a practical realization of the system are discussed, as well as the direct start-up and the short circuit protection of the converter. Also, the advantages and disadvantages of the new converter system are compiled in form of an overview.

Index Terms – Three-Phase High Power Factor Rectifier, High-Frequency Isolation, Single-Stage AC-to-DC Power Conversion, VIENNA Rectifier.

1 Introduction

Three-phase power supply modules for telecommunications systems are designed in a two-stage concept in most cases [1]. This means that the partial tasks

- power factor correction (ideal sinusoidal control of the mains phase currents in phase with the associated phase voltages, i.e. resistive fundamental behavior and low THD and/or guaranteeing electromagnetic compatibility concerning low-frequency mains current harmonics [2], [3]) and
- rectification

are realized by a three-phase PWM rectifier input stage and the tasks

- high-frequency isolation of the output voltage and
- matching of the input and output voltage levels (rated voltage of the European low-voltage mains: $400\,V_{rms}$ line-to-line, rated DC output voltage: 48V or 60V) via winding ratio of the transformer and
- tight, highly dynamic control of the output voltage and/or of the power flow on the output side (avoidance of low-frequency harmonics in the output quantities and/or of psophometric noise)

are handled by a DC/DC converter output stage connected in series. The advantages of this concept are:

- separate optimizability of the converter stages concerning operational mode and dimensioning (e.g., applicability of already proven control methods, power supply to the output stage with constant voltage, independent of mains voltage variations, etc.),
- simple buffering of short mains failures due to providing a capacitor of appropriate capacity in the voltage DC link (at high voltage level) and
- possibility of a separate development of the input and output stages.

However, the following disadvantages have to be mentioned:

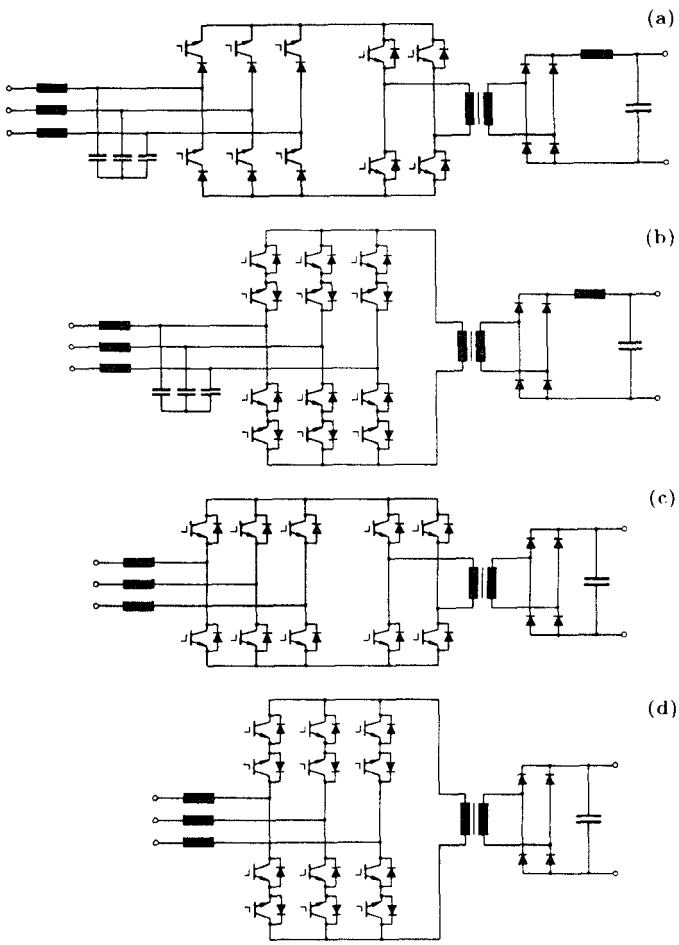

Fig.1: Basic structures of three-phase single-stage high-frequency isolated PWM rectifier systems. **(a)** and **(b)**: quasi-single-stage buck-derived bridge and single-stage buck-derived matrix PWM rectifier system accorcing to [11]. **(c)** and **(d)**: quasi-single-stage boost-derived bridge and single-stage boost-derived matrix PWM rectifier system according to [12] (naming of the systems according to [10]). As opposed to conventional two-stage realizations the filter elements in the DC link (of the two-stage solution) are omitted for single-stage converter topologies; for the systems according to (a) and (b) (buck-derived) the current switched and being injected into the mains by the switching elements on the primary is impressed by the output inductance; for the systems according to (c) and (d) (boost-derived) the voltage being required for controlling the mains current is impressed by the output capacitor (no output inductor has to be provided). For small output voltages and/or high output currents (e.g., for telecommunications power supply modules of higher power) the secondary circuit is realized in most cases as center-tapped circuit and not as full bridge circuit (reduction of the conduction losses).

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- relative high complexity of the entire power and control circuit (high number of power semiconductors and filter elements, separate controls for each converter stage), meaning a relative high realization effort and
- two-fold power conversion and, therefore, possibly reduction of the efficiency of the overall system.

Due to the requirements being characteristic for telecommunications power supplies

- high efficiency of the energy conversion (low energy costs for continuous operation and low effort for airconditioning of the power supply apparatus and/or switching centers),
- high power density (W/cm^3) and/or low specific weight (W/kg) and/or low space requirement and/or simple portability,
- high reliability and
- low production costs,

it, therefore, seems to be obvious to consider possibilities of a realization of *single-stage* three-phase AC-to-DC converters with *high-frequency* isolation of the output voltage.

Remark: Basically the isolation of the output circuit also could be achieved by a mains-side transformer. As shown in [4], this would make realizable a single-stage AC-to-DC converter with a sinusoidal input current shape in an elegant way. However, because especially for telecommunications systems a high power density is desired, in the case at hand only circuit concepts with high-frequency isolation are considered. Also, with regard to high power density the further considerations are limited to direct three-phase systems. This is the case because three-phase converters built up of 3 two-stage [5] or single-stage [6] converters arranged in star or delta connection show a relatively low utilization of the power semiconductors and of the transformers due to the power flow of each phase pulsating with twice the mains frequency (cf. section II-A in [7] and [8]).

Topologies of single-stage, high-frequency isolated three-phase PWM rectifier systems can be formed (as proposed in [9]) by replacing of the input part of basic DC-to-DC converter structures by a three-phase six-switch boost or a six-switch buck PWM rectifier system (self-commutated three-phase bridge circuits with voltage and/or current output, cf. Fig.1 in [10]). There, with consideration of the blocking voltage stress on the valves, especially the combinations with DC-to-DC converter bridge circuits (as proposed and analyzed in principle in [11] and [12]) are of interest (quasi-single-stage bridge PWM rectifier systems, cf. **Figs.1**(a) and (c)). As further alternate circuit variants with the same basic function we want to mention the three-phase buck-derived isolated matrix PWM rectifier system [11] as shown in Fig.1(b) and the three-phase boost-derived isolated matrix PWM rectifier system [12] as shown in Fig.1(d). There, the primary winding of the high-frequency transformer is fed via a three-phase to single-phase AC-to-AC matrix converter with voltage or current output. This converter is built up with turn-off bidirectional and bipolar (four-quadrant) power switching elements. (An interesting alternate realization of a three-phase to single-phase AC-to-DC converter with exclusive application of 12 bidirectional unipolar turn-off power semiconductors – IGBTs with antiparallel free-wheeling diodes – has been proposed in [13]. This, however cannot be treated here in more detail for the sake of brevity.)

For the realization of a single-stage three-phase AC-to-DC converter with high-frequency isolation one basically could use (besides the already mentioned circuit concepts) also the Cuk-based oder SEPIC-based single-switch converters as proposed in [14], [15] and [16] or single-switch three-phase flyback convertes as proposed in [17]. These converters show a very simple structure of the power and control circuits which is paid for, however, by a high voltage and current stress on the devices [18] and by a relatively high filtering effort for suppressing electromagnetic interferences [19] (discontinuous input current shape). The systems are economically applicable, therefore, only for output power levels $< 5\,kW$ and/or they are of minor importance for the realization of high-power telecommunications power supply modules (output power typically $6\ldots12\,kW - 60\,V/100\ldots200\,A$). Therefore, they are not described in greater detail in this paper.

Details of the operation, the control and the dimensioning of the buck-derived single-stage matrix PWM rectifier system are discussed in [20], [21] and [22]. The buck-derived isolated quasi-single-stage bridge PWM recitifier system according to Fig.1(a) is treated in [10] in detail. On the other hand, three-phase isolated (quasi-) single-stage *boost*-derived bridge PWM rectifier systems have not been analyzed in detail so far. This is explained in [10] by the

- higher blocking voltage stress on the valves,
- the problem of start-up of the converter systems (lack of the voltage required for the control and/or limitation of the input current in case of output capacitor not charged) and
- the problem of overload protection (current limitation for short circuit of the output voltage) or of overcurrent limitation for mains overvoltages.

However, boost-derived converter systems show a series of advantages as compared to buck-derived systems, such as

- continuous shape of the input current (therefore, no input filter capacitors have to be provided),
- direct control of the mains current, i.e. of the input quantity being of special interest with regard to effects on the mains (the input current of buck-derived PWM rectifier systems is defined indirectly, i.e., via the difference between mains voltage and the controlled input filter capacitor voltage),
- no danger of a direct short circuit of a mains line-to-line voltage,
- impressed transformer primary current; therefore, contrary to buck-derived converter structures, no danger of high overcurrent spikes due to magnetic core saturation or high reverse recovery time of the diodes on the output side and
- direct voltage output (no output inductor required and/or simple realizablity of several isolated output circuits); the output voltage directly defines the blocking voltage across the diodes on the secondary (the blocking voltage is independent of the input voltage).

These advantages ultimately form the basis for the wide appplicability of this circuit type in connection with *single-phase* single-stage [23], [24], [25] and two-stage power factor correction [26].

Based on this contradiction, a closer and objective analysis and assessment of the practical applicability of three-phase boost-derived single-stage isolated PWM rectifier systems seems of special interest.

In this paper based on a step-by-step simplification of the circuit proposed in [12] (cf. Fig.1(c)) a new topology of a three-phase single-stage high-frequency isolated PWM rectifier system (VIENNA Rectifier II, cf. Figs.2(d) and 3) with minimum complexity of the power circuit is derived (cf. **section 2**). In **section 3**, the basic function of the PWM rectifier system is described based on the conduction states occurring within a pulse period. Furthermore, a straightforward space vector oriented method for the system control is proposed which guarantees a symmetric magnetization of the transformer. Also, it makes possible a sinusoidal control of the mains phase currents in phase with the associated phase voltages (cf. **section 4**). There, the amplitude of the phase currents is given by the output voltage control system. By digital simulation (cf. **section 5**) the theoretical considerations are verified and in **section 6** the stresses on the power semiconductors of the new converter system are calculated in analytical form. Finally, in **section 7** problems of a practical realization of the system, i.e., possibilities of a low-loss limitation of switching overvoltages occurring due to non-ideal coupling of the primary and secondary windings of the transformer are discussed, as well as the direct start-up and the short circuit protection of the converter. Also, the advantages and disadvantages of the new converter system are compiled in form of an overview (cf. **section 8**).

2 Derivation of the Circuit Topology

A three-phase boost-type AC-to-DC converter system with sinusoidal current input and high-freuency isolation of the output voltage is realized, as already mentioned in section 1 in the conventional way as two-stage voltage DC link converter, i.e., by coupling on the DC side of a PWM rectifier system and of a DC-to-DC converter system (cf. **Fig.2**(a)).

As proposed in [12], the structure of this relatively complex system can be simplified by omitting the DC link capacitor C. Then, the DC-to-DC converter stage is operated with impressed current and not with impressed voltage. Therefore, at the output of the DC-to-DC converter no inductor L_O is required to handle the difference between transformed DC link voltage and output voltage (cf. Fig.2(b)). (It is important to note that the DC link capacitor serves only for smoothing power oscillations with switching frequency for three-phase systems and sinusoidal shape of the input quantities. I.e., the resulting

quasi-single-stage converter system has (ideally) a time-constant power flow for averaging over processes with switching frequency despite lacking DC link

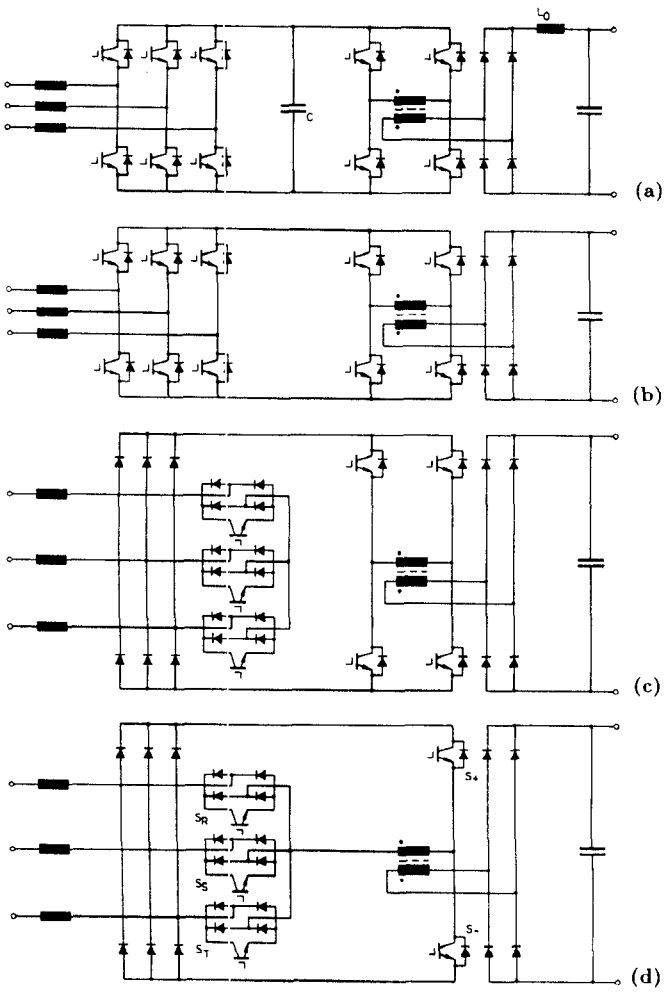


Fig.2: Derivation of the basic structure of a new single-stage boost-type high-frequency isolated PWM rectifier system (cf. **(d)**) based on a conventional two-stage converter system with voltage DC link (cf. **(a)**); **(b)**: by omitting the DC link capacitor C and of the output inductor L_O a quasi-single-stage converter system is formed according to [12]; **(c)**: replacement of the bidirectional input stage of the system according to (b) by a unidirectional PWM rectifier system according to Fig.2 in [27]; **(d)**: the function of one bridge leg of the circuit shown in (c) is taken over by the input stage; this results in a new *single-stage* converter structure which allows (with the exception of a ripple with switching frequency) a sinusoidal mains current control in phase with the mains voltage; accordingly, an (ideally) constant output power results.

capacitor.) However, this circuit modification does not reduce the number of turn-off power semiconductors. Therefore, the system realization is still connected with a relatively high effort and possibilities of a further reduction of the circuit complexity have to be searched for.

A starting point for this is given by the fact that the PWM rectifier stage basically would allow a reversal of the power flow (energy feedback from the DC link into the mains); the system operation is limited to rectifier operation, however, due to the unidirectionality of the DC-to-DC converter output stage. Therefore, the input stage can be replaced by a unidirectional PWM rectifier system as proposed in [27] (cf. Fig.2 in [27]); this allows to halve the number of turn-off power semiconductors of the rectifier stage (cf. Fig.2(c)). Furthermore, this leads to a higher utilization of the power semiconductors because each power transistor of a phase participates in conducting current during the positive *and* negative and not only during one current halfe wave.

Due to the structure of the circuit received thereby it is obvious to transfer partially the function of the DC-to-DC converter output stage to the input stage in a further step. I.e., the switch-over of a terminal of the primary winding of the transformer between positive and negative DC link bus will be performed by the input stage. The now resulting novel topology of a *single-stage* (because sections of the mains phase currents are fed directly via the primary winding and the energy is transferred directly to the secondary) boost-derived three-phase AC-to-DC converter with high-frequency isolation is shown in Fig.2(d).

One has to note, however, that the reduction of the complexity of the power circuit as compared to the circuit according to Fig.2(b) and the transition to direct and/or single-stage energy transfer results in higher complexity of the system control because now the switches S_R, S_S, S_T and S_+ and S_- have to guarantee (in immediate interaction) a sinusoidal mains current shape and a pure alternating magnetization with switching frequency for the transformer magnetic core.

For the derivation of a control law for the circuit shown in Fig.2(d) in the following the space vectors $\underline{u}_{U,j}$ of the rectifier input voltage, resulting for the different switching states j, and the variation of the transformer magnetization are analyzed. There, a modified realization of the proposed circuit is taken as reference (cf. **Fig.3**) which is being obtained by the integration of the four-quadrant switches into the bridge legs of the input diode bridge [28]. The advantage of this realization variant is (as compared to the circuit of Fig.2(d)) that it allows a limitation of the blocking voltages of all valves by a simple overvoltage limitation circuit situated between positive and negative DC link bus (cf. section 7). Furthermore, one can then obtain a free-wheeling of the transformer magnetizing current (and of the mains phase currents) by switching on the switches S_+ and S_-; one is not constrained by the switching state of the switching elements S_i, $i = R, S, T$ (cf. section 4.2), simplifiying the system control.

3 Basic Principle of Operation

Because a mains phase current $i_{N,i}$, $i = R, S, T$, flows through the associated free-wheeling diode $D_{F+,i}$ for turned-off power transistor S_i and through $D_{F-,i}$ for $i_{N,i} < 0$, the voltage generation at the input side of the system is determined not only by the switching states of the power transistors but also by the signs and (as shown in the following) also by the ratios of the phase current magnitudes. The same is true for the polarity if the voltage across

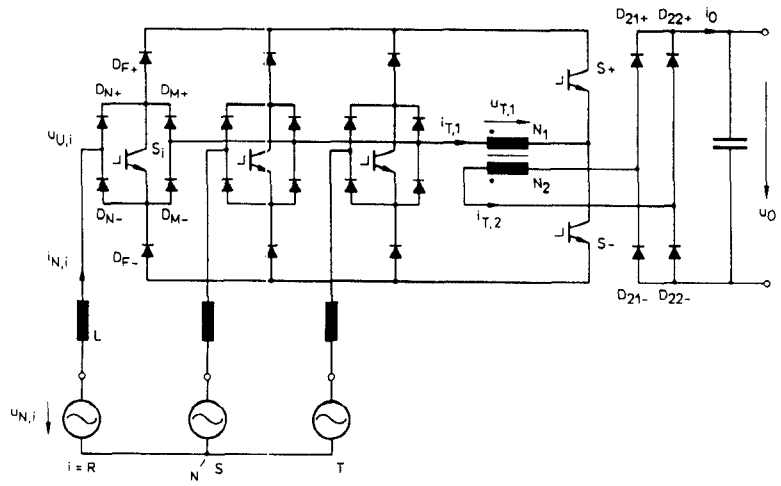


Fig.3: The considerations of this paper are based on the shown realization variant of the proposed three-phase single-stage high-frequency isolated boost-type PWM rectifier system. The circuit is obtained by the integration of the four-quadrant switches of the circuit according to Fig.2(d) into the bridge legs of the input diode bridge (the basic system function is not influenced by this modification). The topology of the input stage is then identical with a three-level PWM rectifier system which has been proposed in [29] (cf. Fig.9 in [29]) and which has been introduced in the literature as VIENNA Rectifier. Accordingly, the circuit proposed here will be called *VIENNA Rectifier II*. However, it has two-level (and not three-level) characteristic concerning voltage generation at the input contrary to the system described in [29]. The feeding three-phase mains is shown in form of voltage sources $u_{N,i}$, $i = R, S, T$.

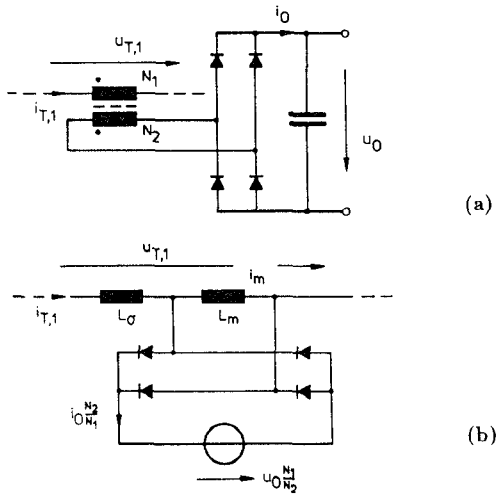


Fig.4: Idealizations of the transformer and the output circuit of the system assumed for the basic considerations of this paper. (**a**): real system, (**b**): idealized system; the isolation of primary and secondary circuit does not influence the basic system behavior and therefore is omitted in (b); the stray inductance L_σ is neglected, for the magnetizing inductance L_m we assume $L_\mathrm{m} \rightarrow \infty$ (with exception of sections 4.1 and 4.2) and/or the magnetizing current i_m is neglected ($i_\mathrm{m} \rightarrow 0$). The output voltage u_O is assumed impressed and constant $u_O = U_O$. Furthermore, the output diodes are assumed ideal (i.e., especially the forward drop is neglected).

the power transformer being defined by the sign of the primary current $i_{T,1}$ (which is formed from sections of the phase currents). However, due to the symmetries of the circuit and of the feeding three-phase voltage system $u_{N,i}$ for analyzing of a sign combination of the phase currents (e.g., $i_{N,R} > 0$, $i_{N,S} < 0$, $i_{N,T} < 0$ being valid within a $\frac{\pi}{3}$-wide interval of the mains period) the relationships within the entire mains period are covered.

3.1 Assumptions

In the following the stationary relations for $i_{N,R} > 0$, $i_{N,S} < 0$ and $i_{N,T} < 0$ and/or for an angle interval $\varphi_N = (-\frac{\pi}{6}, +\frac{\pi}{6})$ are considered. There, the considerations are based on purely sinusoidal mains current shapes

$$\begin{aligned} i_{N,R} &= \hat{I}_N \cos(\varphi_N) \\ i_{N,S} &= \hat{I}_N \cos(\varphi_N - \frac{2\pi}{3}) \\ i_{N,T} &= \hat{I}_N \cos(\varphi_N + \frac{2\pi}{3}) \end{aligned} \tag{1}$$

where

$$\varphi_N = \omega_N t \tag{2}$$

($\omega_N = 2\pi f_N$ denotes the mains angular frequency) in order to limit the derivations to the essentials. This means that the mains current ripple is neglected and only the fundamental is considered. Furthermore, resistive mains fundamental behavior is assumed, i.e., currents $i_{N,i}$, $i = R, S, T$, and mains phase voltages $u_{N,i}$ (having also a purely sinusoidal shape) are in phase. Then, we have for the space vector of the mains current and voltage

$$\begin{aligned} \underline{i}_N &= \hat{I}_N \exp j\varphi_N \\ \underline{u}_N &= \hat{U}_N \exp j\varphi_N \ . \end{aligned} \tag{3}$$

Remark: The space vector related to a triple of phase quantities is calculated according to the defining equation (shown for the example of the mains voltage)

$$\underline{u}_N = \frac{2}{3}(u_{N,R} + \underline{a}\, u_{N,S} + \underline{a}^2 u_{N,T}) \qquad \underline{a} = \exp j\frac{2\pi}{3} \ . \tag{4}$$

The transformer is assumed ideal, i.e., stray inductance L_σ, magnetizing current i_m (with the exception of section 4.2), winding resistances and winding capacitances are neglected. This means that the real transformer is replaced by an ideal transformer with a transformation ratio being equal to the turns ratio $\frac{N_1}{N_2}$ (cf. **Fig.4**). Furthermore, parasitic capacitances of the valves are neglected and/or, in general, idealized valves are assumed (no forward voltage drop, negligible switching times, especially no reverse recovery current for diodes etc.). Then, the analysis of oscillations following switching processes between L_σ and parasitic capacitances and the inclusion of an overvoltage limitation circuit (cf. section 7) can be excluded from the considerations. Furthermore, the output voltage u_O is assumed to be impressed and constant $u_O = U_O$.

3.2 System Switching States and Voltage Generation

For the denomination of the switching state of the power transistors S_R, S_S, S_T and S_+, S_- switching functions s_R, s_S, s_T and s_+, s_- are used in the following. There, $s_i = 1$ corresponds to the on-state and $s_i = 0$ to the off-state. A characterization of the switching state of the overall system can then be made in a clear form by using the combinations $j = (s_R s_S s_T)_{s_+ s_-}^{\mathrm{sign}\{u_{T,1}\}}$. It represents, besides the switching state of the transistors, also a characterization concerning the direction of the current flow $i_{T,1}$ in the primary N_1 of the transformer and/or the sign of the voltage $u_{T,1}$ across N_1 (given by $\mathrm{sign}\{u_{T,1}\} = +$ oder $-$; for $u_{T,1} = 0$, $\mathrm{sign}\{u_{T,1}\} = 0$ is defined).

As becomes immediately clear, the control of the power transistors S_+ und S_- has to be performed dependent on the sign of the phase currents $i_{N,i}$. E.g., for turning off of a switch S_i conducting positive current $i_{N,i} > 0$ one has to turn on S_+ in any case and S_- for turning off a switch S_i conducting negative current $i_{N,i} < 0$ (s_+ bzw. $s_- \rightarrow 1$) in order to guarantee a continuous flow of the phase currents $i_{N,i}$ (which are impressed by the mains side inductances L) via $D_{F+,i}$ and S_+ or D_{F-} and S_-.

Based on this consideration the switching state combinations compiled in **Tab.1** and/or the system conduction states shown in **Fig.5** result.

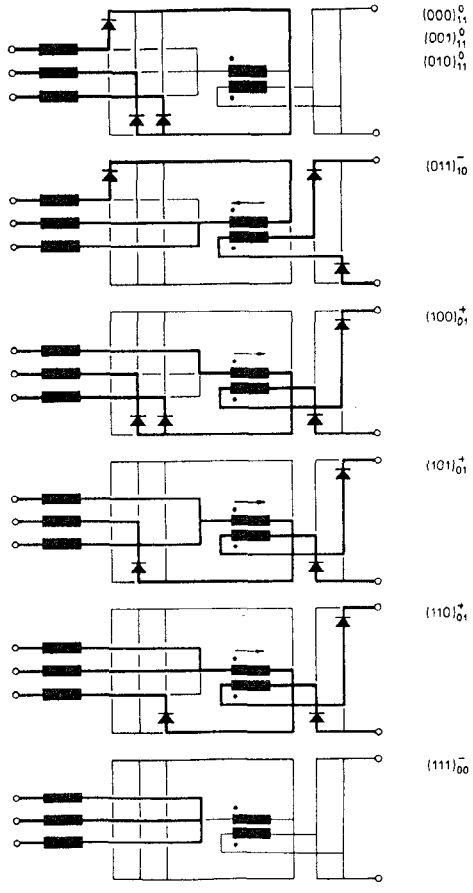


Fig.5: Conduction states of the PWM rectifier system for the possible switching states j according to Tab.1 (valid for $i_{N,R} > 0$, $i_{N,S}, i_{N,T} < 0$). For the sake of clearness the on-states are shown for the circuit according Fig.2(d) for which the connections of the phase switching elements S_R, S_S and S_T with the primary winding N_1 of the transformer are realized separately for each phase. For $j = (110)_{(01)}^{+}$ there results a positive current $i_{T,1} = -i_{N,T}$ due to $|i_{N,R}| > |i_{N,S}|$ and, therefore, a positive sign, $\mathrm{sign}\{u_{T,1}\} = +$, of the primary voltage $u_{T,1}$. Therefore, as mentioned at the beginning of this paper, also the orders of magnitude (besides the signs) of the phase currents take influence on the voltage generation.

s_R	s_S	s_T	s_+	s_-	$\underline{u}_{U,j}$	sign$\{u_{T,1}\}$
0	0	0	1	1	0	0
0	0	1	1	1	0	0
0	1	0	1	1	0	0
0	1	1	1	0	$\frac{2}{3}\frac{N_1}{N_2}U_O$	−
1	0	0	0	1	$\frac{2}{3}\frac{N_1}{N_2}U_O$	+
1	0	1	0	1	$-\underline{a}\frac{2}{3}\frac{N_1}{N_2}U_O$	+
1	1	0	0	1	$-\underline{a}^2\frac{2}{3}\frac{N_1}{N_2}U_O$	+
1	1	1	0	0	0	−

Tab.1: Switching states, related voltage space vectors $\underline{u}_{U,j}$ and signs sign$\{u_{T,1}\}$ of the transformer primary voltage $u_{T,1}$ for $\varphi_N \in (-\frac{\pi}{6}, +\frac{\pi}{6})$.

Besides the possible switching states we also have given in Tab.1 the respective voltage space vectors $\underline{u}_{U,j}$ and the resulting signs sign$\{u_{T,1}\}$ of the transformer primary voltage $u_{T,1}$. E.g., for $s_R = 1, s_S = 0, s_T = 0, s_+ = 0, s_- = 1$, $i_{N,R}$ flows in positive direction in N_1. The current loop is closed via S_- and diodes $D_{F-,S}$ and $D_{F-,T}$ as phase currents $i_{N,S}$ and $i_{N,T}$. Due to $i_{T,1} = i_{N,R} > 0$ there results a current $i_{T,2} = \frac{N_2}{N_1} i_{N,R}$ at the transformer output via D_{22+} and D_{21-} and the output voltage U_O. Therefore, on the primary a voltage $u_{T,1} = +\frac{N_1}{N_2}U_O$ (sign$\{u_{T,1}\} = +$) results and/or the rectifier input phase voltages related to a ficticious center tap of the winding N_1 has the values $u_{U,R} = +\frac{1}{2}\frac{N_1}{N_2}U_O$, $u_{U,S} = -\frac{1}{2}\frac{N_1}{N_2}U_O$ and $u_{U,T} = -\frac{1}{2}\frac{N_1}{N_2}U_O$. Therefore, according to Eq.(4) a space vector $u_{U,(100)^+_{01}} = \frac{2}{3}\frac{N_1}{N_2}U_O$ is formed at the input of the rectifier system. **Fig.6** shows the complete set of the voltage space vectors resulting for the different switching states j which lie symmetrical around the angle interval $\varphi_N \in (-\frac{\pi}{6}, +\frac{\pi}{6})$ of the current space vector $\underline{i}_N$ being associated with $i_{N,R} > 0, i_{N,S} < 0, i_{N,T} < 0$.

For $s_+ = s_- = 1$ ($(s_R s_S s_T) = (000)$ or (001) or (010)) and $s_R = s_S = s_T = 1$ ($s_+ s_- = 00$) for $\varphi_N \in (-\frac{\pi}{6}, +\frac{\pi}{6})$ there follows $\underline{u}_{U,j} = 0$; therefore, these switching states do represent non-active or free-wheeling states of the converter. Besides the switching state combination $s_+ s_- = 00$ shown in Tab.1 one can basically also set $s_+ s_- = 01, 10$ or 11 for $s_R = s_S = s_T = 1$ because for the current flow on the mains side always a closed path via S_R, S_S and S_T exists. The specific choice of $s_+ s_-$ does not have any influence on the voltage generation at the input side of the rectifier system. However, the change of the magnetizing state of the transformer is influenced by $s_+ s_-$ as will be explained in more detail in section 4.2. In this respect also the redundancy of the switching states $j = (100)^+_{(01)}$ and $(011)^-_{(10)}$ concerning voltage generation $\underline{u}_{U,j}$ is of special importance.

4 Mains Current Control and Transformer Volt Second Balancing

4.1 Mains Current Control

For a sinusoidal shape of the mains current one has to form a fundamental (designated by an index (1)) $\underline{u}_{U,(1)}$ of the rectifier input voltage by a current control in such a way that in connection with the mains voltage a current space vector $\underline{i}_N$ (cf. Eq.(3)) lying in phase with $\underline{u}_N$ results,

$$\underline{u}_{U,(1)} = \underline{u}_N - j\,\omega_N L\,\underline{i}_N \ . \tag{5}$$

The fundamental voltage drop $j\,\omega_N L\,\underline{i}_N$ resulting across the mains side series inductances L can be neglected in a first approximation for high switching frequencies $f_P \gg f_N$ (and/or small inductances L). Therefore, for the further considerations

$$\underline{u}_{U,(1)} = \hat{U}_{U,(1)} \exp j\varphi_U \approx \underline{u}_N = \hat{U}_N \exp j\varphi_N \ . \tag{6}$$

is assumed. Therefore, full system controllability is linked to a minimum output voltage value

$$U_O > \frac{N_2}{N_1}\sqrt{3}\,\hat{U}_N \ . \tag{7}$$

As shown in Fig.6, we have for the generation of $\underline{u}_{U,(1)}$ (in the average over a pulse half period) for each sign combination of the phase currents space vectors $\underline{u}_{U,j}$ lying symmetrically around the center axis of the possible positions of the curent space vector $\underline{i}_N$ (and/or of $\underline{u}_{U,(1)}$ or $\underline{u}_N$, cf. Eqs.(3) and (6)). For a minimum ripple of the phase currents only space vectors $\underline{u}_{U,j}$ lying in immediate neighbourhood of $\underline{u}_{U,(1)} \approx \underline{u}_N$ are incorporated into the switching state sequence of a pulse period. With regard to a switching loss minimization they are arranged in such a manner that the transition to the respective following switching state requires the switching of only one phase (and, possibly, of one of the switches S_+ or S_-). Now, for the position of $\underline{u}_{U,(1)}$ shown in in Fig.6 there results the switching state sequence

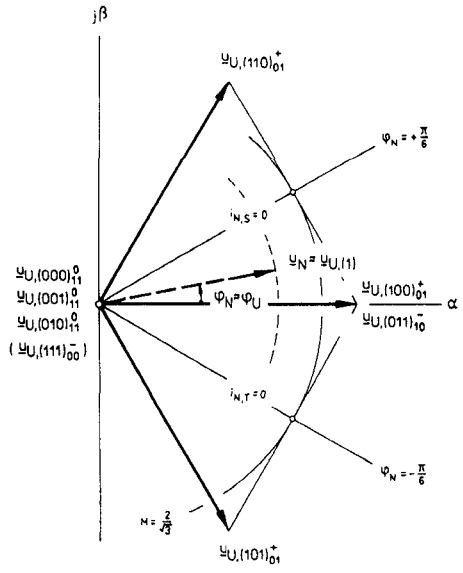


Fig.6: Space vectors $\underline{u}_{U,j}$ of the input voltage associated with the switching states j of the PWM rectifier system according to Tab.1 (based on $i_{N,R} > 0$, $i_{N,S}, i_{N,T} < 0$ and/or $\varphi_N \in (-\frac{\pi}{6}, +\frac{\pi}{6})$).

$$\ldots|_{t_\mu=0}(100)^+_{01} - (110)^+_{01} - (111)^0_{11} - (011)^-_{10}|_{t_\mu=\frac{1}{2}T_P}$$
$$(011)^-_{10} - (111)^0_{11} - (110)^+_{01} - (100)^+_{01}|_{t_\mu=T_P} \ldots . \tag{8}$$

(t_μ denotes a local time being counted within a pulse period T_P). The relative on-time δ_j of the switching states j can be calculated considering Fig.6 and considering the relation

$$\underline{u}_{U,(1)} = \delta_{(110)^+_{01}}\,\underline{u}_{U,(110)^+_{01}} + (\delta_{(100)^+_{01}} + \delta_{(011)^-_{10}})\,\underline{u}_{U,(100)^+_{01}} \tag{9}$$

which is obtained by integration of the different space vectors $\underline{u}_{U,j}$ to the average voltage generation $\underline{u}_{U,(1)}$ within a pulse half period; with simple geometrical considerations one receives

$$\begin{aligned} \delta_{(110)^+_{01}} &= \frac{\sqrt{3}}{2} M \sin(\varphi_U) \\ \delta_{(100)^+_{01}} + \delta_{(011)^-_{10}} &= \frac{\sqrt{3}}{2} M \sin(\frac{\pi}{3} - \varphi_U) \\ \delta_{(111)^0_{11}} &= 1 - (\delta_{(110)^+_{01}} + \delta_{(100)^+_{01}} + \delta_{(011)^-_{10}}) \ . \end{aligned} \tag{10}$$

($\varphi_U \approx \varphi_N$, cf. Eq.(6)). There,

$$M = \frac{\hat{U}_{U,(1)}}{\frac{1}{2}\frac{N_1}{N_2}U_O} \tag{11}$$

designates the modulation depth $M \in (0, \frac{2}{\sqrt{3}})$ of the system.

By the switching states $(100)^+_{01}$ and $(011)^-_{10}$ identical space vectors $\underline{u}_{U,(100)^+_{01}} = \underline{u}_{U,(011)^-_{01}}$ are formed (cf. Fig.6). However, there result transformer primary voltages with inverse signs as denoted by the indexes. This redundancy existing concerning voltage formation can (as shown in the following) be used for obtaining a purely alternating transformer magnetization with switching frequency.

4.2 Transformer Volt Second Balancing

In order to avoid the occurrence of low-frequency components of the transformer primary voltage one has to basically generate an equilibrium of the positive and negative volt seconds resulting within each pulse half period across the transformer primary (and/or secondary). Related to the switching state sequence Eq.(8) as considered here, this leads to the relation

$$\delta_{(100)^+_{01}} + \delta_{(110)^+_{01}} = \delta_{(011)^-_{10}} \ . \tag{12}$$

Thereby, in connection with Eq.(10), one receives for the relative on-time of the redundant switching states

$$\delta_{(100)^+_{01}} = \frac{3}{4}M\sin(\frac{\pi}{6}-\varphi_U)$$
$$\delta_{(011)^-_{10}} = \frac{\sqrt{3}}{4}M\sin(\varphi_U+\frac{\pi}{3})\,. \qquad (13)$$

It is important to point out that – so far – always the switching state $(111)^0_{11}$ and not the switching state $(111)^-_{00}$ given in Tab.1 has been incorporated into the switching state sequence considered. For $s_+s_- = 11$ one has (independently of s_R, s_S, s_T) a short circuit of the primary leading via the diodes $D_{M+,i}$, $D_{F+,i}$ and S_+ or $D_{M-,i}$, $D_{F-,i}$ and S_-. Therefore, the secondary remains without current. The mains current is fed partially via S_R, S_S and S_T and partially via S_+ and S_-. There, the specific current distribution is determined by the forward voltage drop of the valves. The magnetizing state $i_m = \frac{1}{L_m}\int u_{T,1}\,dt$ of the transformer is not changed (according to the neglection of the winding resistances and of the valves forward voltage drops). The magnetizing current path is leading for $i_m > 0$ via S_- and the diodes $D_{F-,i}$ and $D_{M-,i}$, for $i_m < 0$ via S_+ and $D_{F+,i}$ and $D_{M+,i}$.

As opposed to this, the magnetizing current for $s_+s_- = 00$ ($s_R = s_S = s_T = 1$) is conducted only on the secondary of the transformer and, therefore, is decreasing according to the secondary voltage. (On the primary then there is no closed current path for i_m.) i_m then has possibly a discontinous shape because the output diodes do not allow a current sign reversal. The mains currents have free-wheeling paths via S_R, S_S and S_T.

Therefore, besides the distribution of the relative on-times of the switching states $(100)^+_{01}$ and $(011)^-_{10}$ one could also influence the transformer magnetization via appropriate choice of the free-wheeling states. For the sake of brevity, here, this will not be treated in more detail. Only the transformer operation with continuous magnetizing current shape is analyzed and/or only $(111)^0_{(11)}$ is taken as free-wheeling state.

Remark: As mentioned in section 3.1, the power semiconductors are assumed ideal in this paper and also the transformer winding resistances are neglected. For a detailed analysis of the magnetization one would have to consider these parasitic quantities, however, similar to the analysis of a push-pull center tapped DC-to-DC converter in [30]). The magnetizing acting voltage is then dependent not only on the sign but (to a minor extent) also on the actual value of the secondary current.

The control method considered so far can be realized in a simple way by a ramp-comparison current controller (cf. [31] or Fig.14 in [32]) in connection with a direct control of the mains phase currents (cf. Fig.8). As shown in Fig.8(b), then the switching instants of the power transistors S_i are determined via the intersection of the sum of the current control error $\Delta i_{N,i}$ (dynamically weighted by a current controller $G(s)$) and a pre-control signal m_i. There, one has to consider the dependency of the voltage generation $u_{U,i}$ (mentioned in section 3.2) on the sign of the associated phase current $i_{N,i}$ by inversion

$$s_i = \begin{cases} s'_i & \text{if } i^*_{N,i} \geq 0 \\ \text{NOT}\, s'_i & \text{if } i^*_{N,i} < 0 \end{cases} \qquad (14)$$

of the switching decision

$$s'_i = \begin{cases} 0 \text{ if } i_D < m_i - \Delta i_{N,i} \\ 1 \text{ if } i_D > m_i - \Delta i_{N,i} \end{cases} \qquad (15)$$

of the pulse width modulator for $i_{N,i} < 0$; there $\Delta i_{N,i} = i^*_{N,i} - i_{N,i}$, $i^*_{N,i}$ denotes the phase current reference value.

By the pre-control signals m_i there

- shall be obtained the distribution of the switching states which are redundant with respect to the voltage generation (between the begin and end of each pulse half interval) required for a symmetric transformer magnetization and
- already for $\Delta i_{N,i} = 0$ at the system input a voltage having a fundamental $\underline{u}_{U,(1)}$ equal to the mains voltage $\underline{u}_N$ shall be formed. Thereby, the current controller has to provide only the relative small fundamental voltage drop across the series inductances L. Furthermore, despite the fact that the gain of an integral acting component of $G(s)$ is limited to finite values for mains frequency variations, the control error is limited to small values (cf. Fig.22 in [33]).

The signal shape

$$\varphi_U \in (0, +\frac{\pi}{6}): \qquad m_R = \frac{\sqrt{3}}{2}M\hat{I}_D\sin(\varphi_U+\frac{\pi}{3}) - \hat{I}_D$$

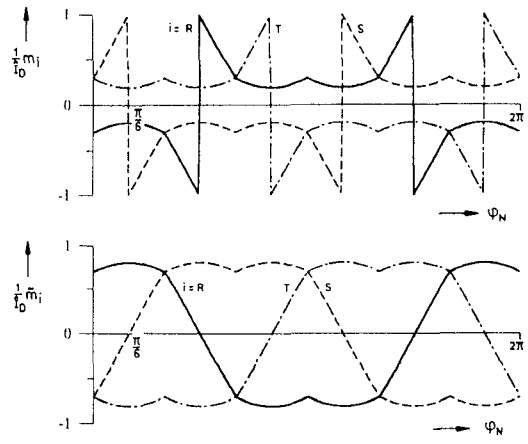


Fig.7: Shape of the pre-control signals m_i of the ramp-comparison control within a mains period (cf. (a)) rated with respect to $\hat{I}_D$. The continuous shape $\tilde{m}_i$ of the pre-control signals as shown in (b) can be obtained based on (a) by addition of rectangular signals according to Eq.(17).

$$m_S = \hat{I}_D - \frac{3}{2}M\hat{I}_D\sin(\frac{\pi}{6}-\varphi_U)$$
$$m_T = \hat{I}_D - \frac{\sqrt{3}}{2}M\hat{I}_D\sin(\varphi_U+\frac{\pi}{3}) \qquad (16)$$

being directly calculable based on Eqs.(10) and (12) (the shape in the other intervals of the mains period follows simply by symmetry considerations) is shown in **Fig.7**(a). For the sake of brevity, a more detailed description of the derivation of Eq.(16) is omitted here. We only want to point out that by subtraction

$$\tilde{m}_i = \begin{cases} m_i - \hat{I}_D & \text{if } m_i \geq 0 \\ m_i + \hat{I}_D & \text{if } m_i < 0 \end{cases} \qquad (17)$$

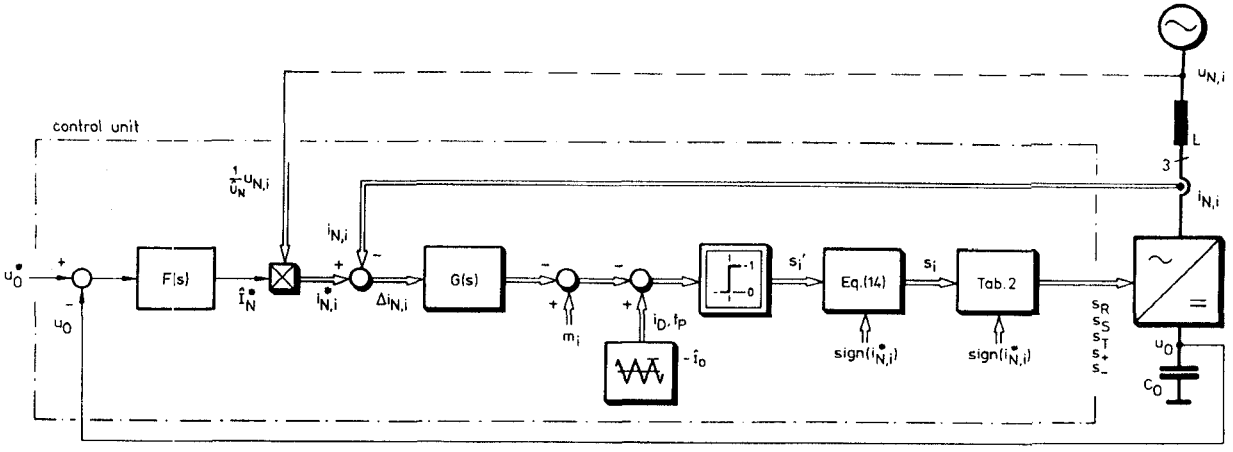
of a rectangular function (defined via the sign of m_i and/or of $u_{N,i}$) of the amplitude $\hat{I}_D$ a continuous shape $\tilde{m}_i$ of the pre-control signals can be obtained (cf. Fig.7(b)). Surprisingly, thereby a signal shape results which is known from the modulation functions for space vector modulation for bidirectional six-switch boost-type voltage DC link PWM rectifier systems (cf. Fig.7(b) and Fig.12 in [34]).

4.3 Overall Structure of the System Control

The block diagram of a two-loop system control with output voltage controller as master control and ramp-comparison current control as slave control is shown in **Fig.8**.

The phase current reference values $i^*_{N,i}$ have a shape proportional to the associated mains phase voltages $u_{N,i}$ (resistive fundamental mains behavior). The reference value of the amplitude $\hat{I}^*_N$ of the mains phase currents is set by the output voltage controller $F(s)$ in dependency on the control error of the output voltage $u^*_O - u_O$. As described in section 4.2, the influence of the mains phase voltages on the current control is compensated by pre-control signals m_i which also guarantee a symmetric magnetization of the transformer magnetic core. Based on the switching decisions s'_i of the modulator stage of the current controller the phase switching functions s_R, s_S and s_T are generated according to Eq.(14) as well as the related switching states s_+s_- are formed by a combinatorial logic circuit according to Tab.1. There, as mentioned before, the free-wheeling state is represented by $(111)^0_{11}$ and not by $(111)^-_{00}$. Into the combinatorial logic also the correction (as described in section 4.4) of dynamically occurring erroneous switching states of the current controller are included.

Figure 8 shows the derivation of the phase switching functions s_i via intersection of the triangular carrier wave i_D with the pre-control signals m_i for stationary operation and for one pulse period T_P. If, e.g., the current control error $\Delta i_{N,R} = +\Delta i_N$, $\Delta i_{N,S} = \Delta i_{N,T} = -\frac{1}{2}\Delta i_N$ occurs (as shown by dashed lines), the relative on-time of the switching state $(111)^0_{(11)}$ is increased and the relative on-time of the switching states $(100)^+_{(01)}$ and $(011)^-_{(10)}$ is reduced accordingly. This leads to an increase of the absolute value i_N of the mains current space vector by $\underline{u}_N$ ($L\frac{di_N}{dt} = \underline{u}_N - \underline{u}_{U,(111)^0_{11}}$, $\underline{u}_{U,(111)^0_{11}} = 0$), eliminating the control error Δi_N.



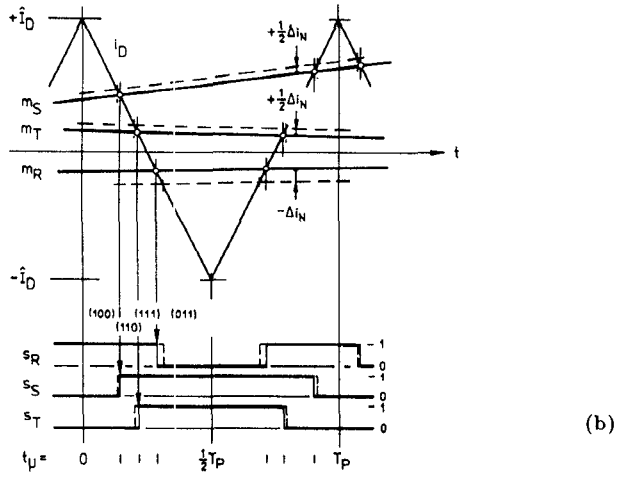


Fig.8: Block diagram of the two-loop control (cf. **(a)**) of the proposed PWM rectifier system (shown schematically); for the sake of clearness, signal paths being equal for all phases are combined in double lines; **(b)**: time behavior of the triangular carrier wave i_D of the ramp-comparison current controller, of the pre-control signals m_i, of a superimposed current control error $\Delta i_{N,R} = +\Delta i_N$, $\Delta i_{N,S} = \Delta i_{N,T} = -\frac{1}{2}\Delta i_N$ and of the control signals s_i generated within a pulse period T_P. The signals $\Delta i_{N,i}$ are shown constant over T_P for a clear representation; in reality, however, a variation in the control errors will take place due to the changes of the system switching state.

4.4 Correction of Dynamically Occurring False Switching Decisions of the Current Controller

According to Eq.(8) within the angle interval $\varphi_N \in (0, +\frac{\pi}{6})$ (considered in conection with Fig.6) in the stationary case only switching states $(s_R s_S s_T) = (100), (110), (111), (011)$ and in $\varphi_N \in (-\frac{\pi}{6}, 0)$ only $(100), (101), (111), (011)$ are applied for voltage generation. The switching states remaining in comparison to Tab.1 result only for the dynamic case (as a more detailed analysis of the selected current control concept shows), e.g., for a high step change of the reference value $\hat{I}_N^*$ of the mains current amplitude.

If, e.g., based on the relations shown in Fig.8(b), the tip of the mains current space vector $\underline{i}_N$ shall be guided by $\Delta\underline{i}_N$ in the direction of the negative phase axis R and/or the absolute value i_N of $\underline{i}_N$ shall be reduced, then the switching state $(000)_{11}^0$ and/or $\underline{u}_{(000)_{11}^0}$ is generated by the current controller for sufficiently large Δi_N. (For $(\Delta\underline{i}_N = \Delta i_{N,R} < 0$ there follows $\Delta i_{N,S} = \Delta i_{N,T} = -\frac{1}{2}\Delta i_{N,R} > 0$ due to $\Delta i_{N,R} + \Delta i_{N,S} + \Delta i_{N,T} = 0$.) Due to the mains voltage $\underline{u}_N$ there would result an *increase*, however, and not a decrease of i_N, which has to be avoided by recoding of $(000)_{11}^0$ in $(100)_{01}^+$ or $(011)_{10}^-$ (cf. **Tab.2**).

The further corrections of false switching decisions given in Tab.2 could be derived in a similar manner by assuming a step change of $\underline{i}_N$ in positive direction of the phase axis S, $\Delta\underline{i}_N = \Delta i_{N,S} > 0, \Delta i_{N,R} = \Delta i_{N,T} = -\frac{1}{2}\Delta i_{N,S} < 0$, and/or the phase axis T, $\Delta\underline{i}_N = \Delta i_{N,T} > 0, \Delta i_{N,R} = \Delta i_{N,S} = -\frac{1}{2}\Delta i_{N,T} < 0$.

controller output		applied switching state
$(000)_{11}^0$	$\rightarrow$	$(100)_{01}^+$ or $(011)_{10}^-$
$(001)_{11}^0$	$\rightarrow$	$(101)_{01}^+$
$(010)_{11}^0$	$\rightarrow$	$(110)_{01}^+$

Tab.2: Correction of the dynamically occurring false switching decisions of the current controller for $\varphi_N \in (-\frac{\pi}{6}, +\frac{\pi}{6})$.

In general, the switching states corresponding to a false switching decision of the current controller are determined by the signs of the phase currents. The corrections to be taken for the $\frac{\pi}{3}$-wide intervals of the mains period not treated here can simply be derived by considerations analogous to the considerations described so far. For the sake of brevity, a more detailed discussion shall be omitted here.

5 Simulation Results

The theoretical considerations of the previous sections have been verified by digital simulation for the following operating parameters (which are typical for a system application as high-power telecommunications power supply module):

$U_{N,\mathrm{rms}}$	= 230 V	f_N	= 50 Hz
$\frac{N_1}{N_2}U_O$	= 700 V	L	= 1 mH
$\hat{I}_N$	= 18 A	L_m	= 5 mH

The switching frequency has been set to $f_P = 16\,\mathrm{kHz}$ under consideration of the duration of a simulation run. For a practical realization and for the requirement of high power density, f_P would have to be selected higher by at least a factor of 2 (reduction of the inductances L and L_m being relatively high in the case at hand). Thereby, however, in general a reduced efficiency of the energy transformation results due to the higher switching losses. For the sake of brevity $G(s)$ has been set to 1 and/or the output voltage has been assumed impressed. Therefore, the dimensioning of the output voltage controller $F(s)$ could be omitted. The triangular carrier wave i_D has been set to $\hat{I}_D = 10\,\mathrm{A}$.

Based on the parameters previously compiled, the modulation depth according to Eq.(11) follows as

$$M = 0.934\ .$$

Thereby, a sufficiently large distance from the modulation limit $M = \frac{2}{\sqrt{3}} \approx 1.15$ is guaranteed and high control dynamics is given. The simulation results are shown in Figs. 9 and 10.

Figure 9 shows a detail of the shape of the phase switching functions s_i, $i = R, S, T$, and of the control signals s_+ and s_-. Furthermore, the transformer primary current $i_{T,1}$ formed from mains phase current sections and the resulting transformer primary voltage $u_{T,1}$ are shown. The equilibrium of the positive and negative volt seconds across the transformer and/or the symmetric magnetization of the transformer magnetic core becomes clear via the shape of the magnetizing current i_m. A change of the i_m results only for the active switching states $(100)_{01}^+$, $(110)_{01}^+$ and $(011)_{10}^-$; for free-wheeling $(111)_{11}^0$ i_m remains constant due to the then given short circuit of the primary winding. The shape of the secondary current $\frac{N_2}{N_1}i_O$ can be derived from $i_{T,1}$ by subtraction of the magnetizing current and rectification (cf. Fig.4(b)).

In **Fig.10**(a) the shapes of the currents and voltages on the primary and of the output current within a mains period are shown. One has to point out especially there that the system current consumption is almost purely

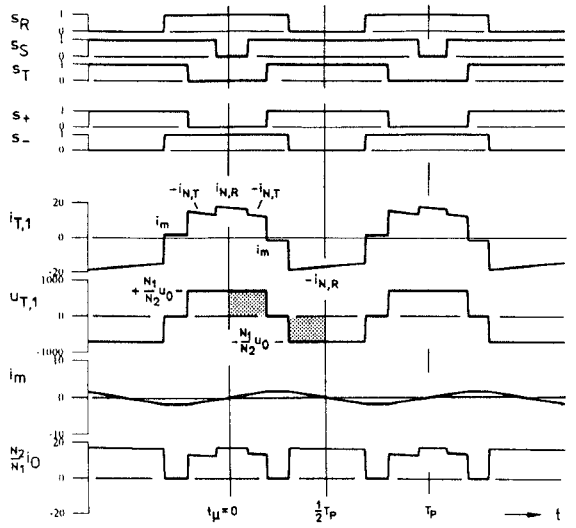


Fig.9: Detail of the time behavior of the control signals s_i, s_+ and s_-, of the transformer primary current $i_{T,1}$, of the transformer primary voltage $u_{T,1}$, of the magnetizing current i_m and of the transformed output current $\frac{N_2}{N_1} i_O$ for $\varphi_N \approx \frac{\pi}{12}$ ($i_{N,R} > 0$, $i_{N_S} < 0, i_{N,T} < 0$). The positive and negative volt seconds across the transformer within a pulse half period are pointed out by dotted areas.

sinusoidal (in phase with the mains voltage) despite the simple current control concept used. After filtering out the harmonics with switching frequency this results in an approximately constant power flow to the output. The low frequency harmonics existing in the spectrum of the mains phase current and of the output current (cf. Fig.10(b)) now have very small amplitudes related to the fundamental $\hat{I}_N$ and/or to the average value $I_O = \frac{3}{2} \frac{\hat{U}_N \hat{I}_N}{U_O}$ (suppressed in Fig.10(b)).

6 Stresses on the Components

If the switching overvoltages are neglected, the blocking voltage stress on all semiconductors on the primary is determined by the transformed output voltage $\frac{N_1}{N_2} U_O$. The blocking voltage stress on the output diodes is defined directly by the output voltage U_O.

The current stress on the power devices can be determined with very good accuracy by analytical calculation [34]. This shall not be treated in detail here, however. In the following, only the average and the rms current values for the power transistors S_i, $i = R, S, T$, and S_+ and of the current in the freewheeling diode $D_{F+,i}$ are given (S_- and S_+ and $D_{F+,i}$ and $D_{F-,i}$ have identical current stresses) as they are of special interest for a first assessment and a first comparison of the system with alternative concepts

$$
\begin{aligned}
I_{S_i,\mathrm{avg}} &= \frac{\sqrt{3}M}{2\pi} \hat{I}_N & I^2_{S_i,\mathrm{rms}} &= \frac{M}{\pi}\left(\frac{23\sqrt{3}}{24} - 1\right)\hat{I}^2_N \\
I_{D_F,\mathrm{avg}} &= \frac{1}{\pi}\left(1 - \frac{\sqrt{3}}{4}M\right)\hat{I}_N & I^2_{D_F,\mathrm{rms}} &= \left(\frac{1}{4} - \frac{M}{6\pi}\left(\frac{23\sqrt{3}}{8} - 3\right)\right)\hat{I}^2_N \\
I_{S_+,\mathrm{avg}} &= \frac{3}{\pi}\left(\frac{1}{4} - \frac{\sqrt{3}}{4}M\right)\hat{I}_N & I^2_{S_+,\mathrm{rms}} &= \left(\frac{1}{2} + \frac{3\sqrt{3}}{4\pi} - \frac{M}{8\pi}(12 - \sqrt{3})\right)\hat{I}^2_N \,.
\end{aligned}
\tag{18}
$$

The equations compiled here are valid for the assumption that within the free-wheeling state $(111)^0_{(11)}$ only the power transistors S_+ and S_- conduct current; furthermore, the magnetizing current i_m has been neglected for the calculations.

For the simulation parameters selected in section 5 there follows then

$$
\begin{aligned}
I_{S_i,\mathrm{avg}} &= 4.6\,\mathrm{A} & I_{S_i,\mathrm{rms}} &= 8.0\,\mathrm{A} \\
I_{D_F,\mathrm{avg}} &= 3.4\,\mathrm{A} & I_{D_F,\mathrm{rms}} &= 7.0\,\mathrm{A} \\
I_{S_+,\mathrm{avg}} &= 10.2\,\mathrm{A} & I_{S_+,\mathrm{rms}} &= 13.1\,\mathrm{A}\,.
\end{aligned}
$$

Therefore, a current stress on the power transistors S_i results which is relatively low in relation to the rms value $I_{N,\mathrm{rms}} = 12.7\,\mathrm{A}$ and the average absolute value $I_{N,\mathrm{avg}} = 11.5\,\mathrm{A}$ of the mains current. For the valves S_+ and S_- which are realized advantageously as IGBT bridge half leg the current stress can be set equal to the mains current characteristic values in a first approximation.

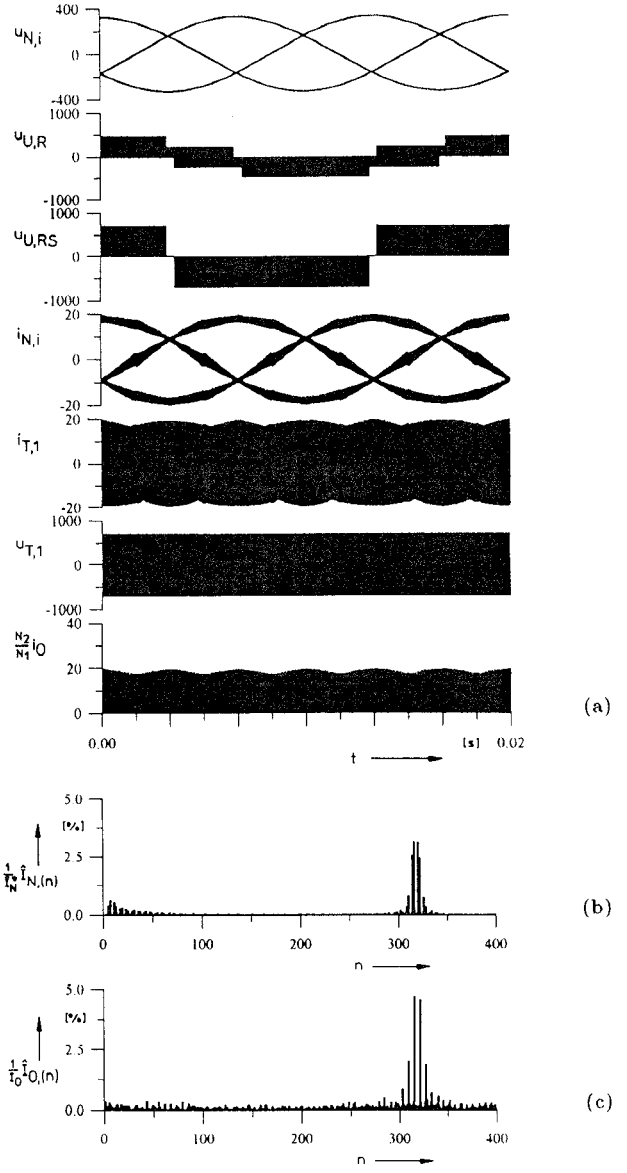


Fig.10: Digital simulation of the time behavior of the mains phase voltages $u_{N,i}$, $i = R, S, T$, of the line-to-line rectifier input voltage $u_{U,RS}$, of the rectifier input phase voltage $u_{U,R}$ related to the mains star point N, of the mains phase currents $i_{N,i}$, of the transformer primary current $i_{T,1}$, of the transformer primary voltage $u_{T,1}$ and of the load current i_O within a mains period; for a clear representation of the conditions, $L_\sigma = 0$ and $L_\mathrm{m} \to \infty$ have been assumed. Furthermore shown are the rated spectrum of the mains current (cf. **(b)**, fundamental component $\hat{I}_N$ suppressed) and of the output current i_O (cf. **(c)**, DC value I_O suppressed); n denotes the order of the harmonics related to the mains frequency f_N.

Regarding the remaining stresses on the devices (being of importance for the dimensioning) we want to refer the reader to a publication being in preparation at present.

7 Aspects of a Practical Realization

7.1 Overvoltage Limitation

A problem of practical realization of the proposed circuit consists in the fact that the transformer is operated not voltage-fed (as for the buck-derived converter systems) but current-fed. Naturally thereby, every change of the switching state and/or of the transformer primary current is connected with the occurrence of an overvoltage. This overvoltage has to be limited by an overvoltage limitation circuit D_cl, U_cl (cf. **Fig.11**), e.g., between the positive

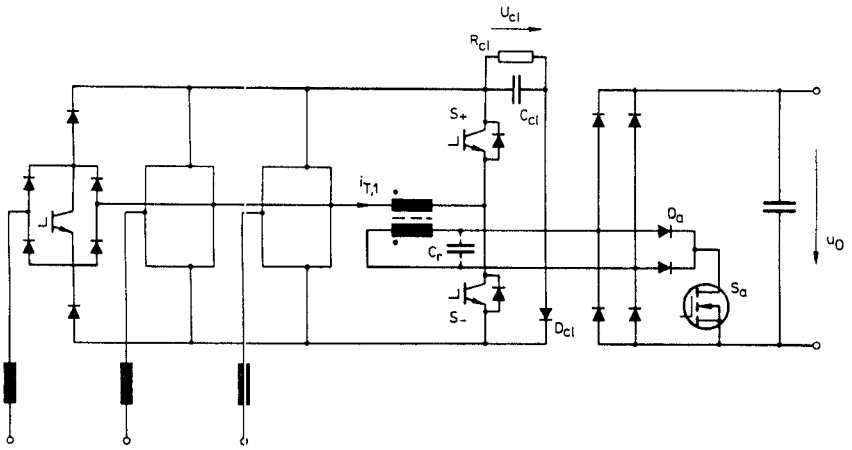


Fig.11: Circuit measures for limiting the switching overvoltages occurring due to the transformer stray inductance. Due to the overvoltage limitation circuit D_{cl}, C_{cl}, R_{cl} the overvoltages (resulting for a step change of $i_{T,1}$) of all valves on the primary are limited to U_{cl}. R_{cl} has to be replaced by a low-power isolated DC-to-DC converter delivering the limitation power to the output U_O if a high efficiency is required. A reduction of the limitation power can can be obtained by an auxiliary switch S_a on the secondary. A basically lossless system operation is possible if one changes from hard- to soft-switching operation by connecting a capacitor C_r in parallel to the secondary; in this case, the switching state sequence of each pulse period has to be extended as compared to hard switching.

and negative DC link voltage bus. Only by this exceeding of the maximum allowable blocking voltage stress on the power semiconductors can be avoided. As a more detailed analysis by digital simulation shows, the power fed into U_{cl} amounts to about 2...4% of the output power P_O for low-stray winding design ($\frac{L_\sigma}{L_m} = 0.005...0.01$). Thereby, a pronounced dependency on the level of the limiting voltage $U_{cl} > \sqrt{3}\hat{U}_N$ exists (the numbers mentioned so far are valid for the operating parameters given in section 5 and for a limiting voltage $U_{cl} = 900\,V$ which allows a realization of the power transistors by IGBTs with a blocking voltage capability of $V_{CES} = 1200\,V$). In order to obtain high efficiency of the energy conversion, in practice U_{cl} is realized by a storage capacitor C_{cl} and a (low-power) DC-to-DC converter lying in parallel. The latter transfers the power pulses fed into the limitation circuit continuously and with low loss to the secondary (cf. p. 152 in [35]).

An essential reduction of the limitation power can be obtained by a switch S_a (and decoupling diodes D_a) on the secondary. This has been proposed in [17] in connection with a single-switch three-phase flyback converter topology and also has been analyzed in [36]. By S_a the secondary is shortened during changes of the primary current as forced by switching state charges of the system. Thereby, the full limitation voltage is available for obtaining of a new stationary current value which is delayed by the stray inductance and not only the difference of the limitation voltage and the voltage coupled into the transformer primary. The time interval for the current commutation is substantially shortened thereby and/or the power fed into the limitation circuit is substantially reduced.

A further alternative is given by the transfer to a soft-switching system operation. Thereby, the stray inductance L_σ can be incorporated into the system function. For this, in analogy to Fig. 4.16 in [35] one has to provide a capacitor C_r across the output terminals of the transformer. Furthermore, then the switching state sequence according to Eq.(8) has to be extended to $(100)^+_{01} - (110)^+_{01} - (111)^+_{00} - (000)^+_{11} - (011)^-_{10} - (111)^-_{00} - (000)^-_{11} - (100)^+_{01}$. (Then, the magnetizing voltage is defined by C_r and, therefore, maintained also for blocking output diodes.) For the sake of brevity, further details are omitted here. The soft-switching operation shall be described in greater detail in a future paper.

7.2 System Start-Up and Overload Protection

As mentioned in [10], the start-up and the overload protection (short circuit of the output voltage) represent critical operating conditions for a single-stage boost-derived converter system. In both cases, the voltage coupled into the transformer primary (which guides the mains current) is missing . The current being driven by the mains voltage cannot be limited, therefore, independently of the converter switching state, i.e., also for the active switching states $(100)_{01}$, $(011)_{10}$, $(110)_{01}$ and $(101)_{01}$ (in $\varphi_N \in (-\frac{\pi}{6}, +\frac{\pi}{6})$) being voltage forming during regular operation. In case of a short circuit of the output voltage ($U_O = 0$) one has to block, therefore, immediately all power transistors ($s_i, s_+, s_- \rightarrow 0$). The energy stored in the mains side inductances is then fed into the limitation circuit U_{cl}; this has to be taken into consideration for dimensioning the storage capacitor C_{cl}. Then, finally, the phase currents $i_{N,i}$ become 0. Therefore, a limitation circuit is required also in such cases when no overvoltages result for regular operation (i.e., e.g., for soft-switching operation).

The system start-up can be realized such that C_{cl} is charged (with blocking power transistors $s_i = 0$ and $s_+ = s_- = 0$) via diodes D_{N+}, D_{F+}, D_{F-} and D_{N-} to the peak value of the line-to-line voltage. Then, in a second step the output capacitor (for turned-off load circuit) is charged by the DC-to-DC converter which for regular operation discharges the limitation capacitor. Then, the output voltage being required for current control is available; the voltage and current control can be enabled and the load can be connected.

8 Conclusions

In this paper a novel topology of a single-stage three-phase AC-to-DC converter with sinusoidal input current shape and high-frequency isolation of the controlled output voltage has been proposed.

The system has (especially as compared to buck-derived topologies [37]) the following advantages and disadvantages. (The general advantages of single-stage as compared to two-stage converter systems already mentioned in section 1 are not discussed in detail here again.)

Advantages:

- simple structure of the power and control circuits (the control described can be realized in purely analog fashion)
- continuous sinusoidal input current shape (reduction of the filtering effort required on the mains side and/or lower electromagnetic influence on other systems)
- according to the constant power flow at the input for sinusoidal current shape there are no low-frequency harmonics of the output current (low psophometric noise)
- impressed transformer primary current and/or dynamic limitation of the input current (e.g., for saturation of the magnetic circuit of the transformer due to control unsymmetries); furthermore, thereby current spikes on the primary resulting from reverse recovery currents of the output diodes for buck derived converter systems are avoided; also, a conduction overlap of the power transistors, i.e., switching state $s_- = s_+ = 1$ and/or $s_R = s_S = s_T = 1$ becomes admissible and does not lead to a short circuit of the line-to-line voltage
- the maximum volt seconds resulting across the transformer are limited and are defined by the pulse period and the output voltage (and not by the mains voltage as for buck-derived converter systems). Therefore, also for heavily varying mains voltage a good transformer utilization can be obtained (for approximately constant output voltage)
- the blocking voltage of the output diodes is defined by the output voltage (with low inductance) and is independent of the mains voltage. This is of special advantage for wide input voltage range and constant output voltage and/or, in general, for high output voltages. (For buck-type converters the blocking voltage stress on the output diodes is defined by the mains voltage.) Due to the stray inductance and due to the output inductance one has no voltage level for a direct limitation of the blocking voltage; this is in analogy to the limitation of the voltages on the primary for boost-derived converter systems (cf. section 7)
- good cross-regulation for more than one output voltage under the assumption of close coupling of the secondary currents (cf. p.1 in [37]) because no filter inductances are in series with the different output

voltages. (A similar system behavior can be obtained for buck-type converters only for magnetic coupling of the output inductances. This involves a relatively high realization effort, however.)

Disadvantages:

- discontinuous output current shape and/or relatively high current stress on the output capacitors and on the output diodes
- right-half plane zero of the transfer function between modulation depth of the converter (according to the duty ratio for DC-to-DC converters) and the average output current
- limitation of the transformer primary voltage and/or the blocking voltage across the power semiconductors on the primary is required because, otherwise, the transformer stray inductance would lead to high overvoltages for a change of the converter switching state and/or a step change of the transformer primary current
- unfavorable transformer dimensioning for a wide variation range of the input and output voltages because the transformation ratio $\frac{N_1}{N_2}$ has to be selected such that for minimum output voltage still a primary voltage can be generated which balances the maximum input voltage
- in general, no direct start-up and no direct current limitation for an output voltage short circuit is possible; more complex start-up than for buck-derived converter systems; the basic reason is that the system function is dependent on a minimum value of the output voltage (which in turn is dependent on the input voltage).

As becomes clear by the list given, the converter system proposed has a number of advantages which motivate a closer investigation going beyond the basic considerations of this paper. Here, especially the soft-switching operation and the possibility of operating the system with low pulse rate (as proposed in [38] and [39] for the conventional VIENNA Rectifier) shall be investigated. Furthermore, the establishment of guidelines for converter dimensioning and an experimental analysis based on a laboratory model are planned.

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