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***Abstract*—Due to the increasing power consumption of data centers, efficient dc power distribution systems have become an important topic in research and industry over the last years. Furthermore the power consumed by data centers is an economic factor, which implies that all parts of the distribution system should be designed to minimize the life cycle cost, i.e. the sum of first cost and the cost of dissipation. This paper analyzes a three-phase buck-type PFC rectifier with integrated active 3rd harmonic current injection for dc distribution systems. Switching frequency, chip area and magnetic components are selected based on a life cycle cost optimization, showing that a peak efficiency of 99 % is technically and economically feasible with state-of-the-art SiC MOSFETs and magnetic components. Measurements taken on an 8 kW, 4 kW dm^{-3} hardware prototype demonstrate the validity and feasibility of the design.**

I. Introduction

Information and communication technology equipment has become a significant consumer of electric power in recent years. In 2007, for example, the related annual consumption in Germany alone was 55 TW h which equaled approximately 10 % of the countries total consumption, where the annual power consumption of data centers located in Germany is approximately constant at ≈ 10 TW h since 2008 [1].

Therefore, the cost for electric energy is becoming a significant economic factor. Given some basic economic parameters the capital-equivalent worth of a continuously dissipated watt of ac power can be estimated. In 2008 the authors of [2] estimate an average value of $14 per watt for the US market and 15 years of service life, which implies that up to $14 could be invested now in order to reduce the equipment's power consumption by one watt over the next 15 years. Even-though the prices for electric power show a considerable geographical variation (approximately a factor of 5 in the US), the authors conclude that the cost of dissipation significantly overshadows the first cost for telecom power supplies.

In conventional data centers using ac distribution systems, as shown in **Fig. 1 a)**, up to 50 % of the total energy consumed is used for air conditioning, distribution and conversion losses [3]. Compared to this, distribution systems based on a dc bus with a nominal voltage of 380 V offer significantly higher efficiency, improved reliability and reduced capital cost and floor space, cf. **Fig. 1b)** [4]. Furthermore they allow a direct connection of lead acid batteries, consisting of 168 cells connected in series, with a typical floating cell voltage of ≈ 2.26 V, which results in a nominal bus voltage of 380 V. Accordingly, standards and components for dc distribution systems have been developed in recent years [5, 6].

Normally a boost-type power factor correction (PFC) stage is used to convert the 400 Vac mains into a dc voltage which is higher than the full-wave rectified ac input voltage, typically in the range of 700 V to 800 V. A subsequent buck converter is then required to connect the PFC output to the dc distribution bus. This configuration is also used for fast chargers of Electric Vehicle batteries which are powered from the three-phase ac mains [7]. As an alternative, a single-stage conversion between the three-phase mains and a dc bus with lower voltage can be achieved with buck-type PFC converters, like the SWISS Rectifier, the six-switch buck rectifier or Integrated Active Filter rectifier [8, 9].

A. Buck-Type PFC Rectifiers

In **Fig. 2a)** the basic schematic of the six-switch rectifier, consisting of an ac input filter, six fully controllable (i.e. reverse blocking) switches and a dc output filter is shown. An additional diode $D_{\bar{n}\bar{p}}$ can be used to lower the conduction losses in the free wheeling state. Note that similar PWM rectifiers, implemented with thyristors, have been used as early as 1979 [10]. Several modifications of the basic circuit topology, reducing the number of active switches, reducing conduction losses and for buck-boost operation have been described [11–13].

An alternative buck-type PFC converter, called SWISS rectifier, is shown in **Fig. 2b)**. It consists of an ac input filter, an Input Voltage Selector (IVS) built of a line-commutated full-wave diode rectifier $D_{\bar{k}x}$, $D_{z\bar{k}}$ $\bar{k} \in \{\bar{a}, \bar{b}, \bar{c}\}$ and three four-quadrant switches $S_{\bar{k}y\bar{k}}$ and two buck converters which

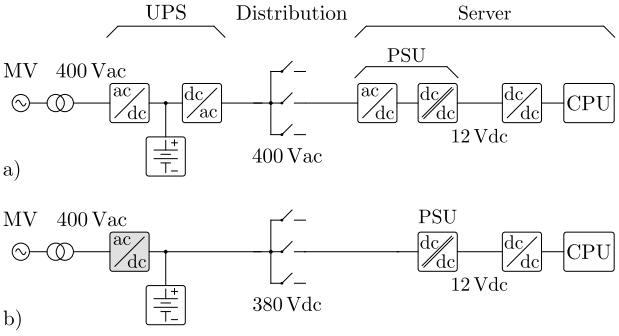

Fig. 1. Data center power distribution concepts: **a)** Conventional 400 Vac distribution, using an ac Uninterruptible Power Supply (UPS). Similar concepts can be used with 480 Vac. **b)** Facility level dc distribution system based on a 380 Vdc bus which allows a direct connection of backup batteries [3].

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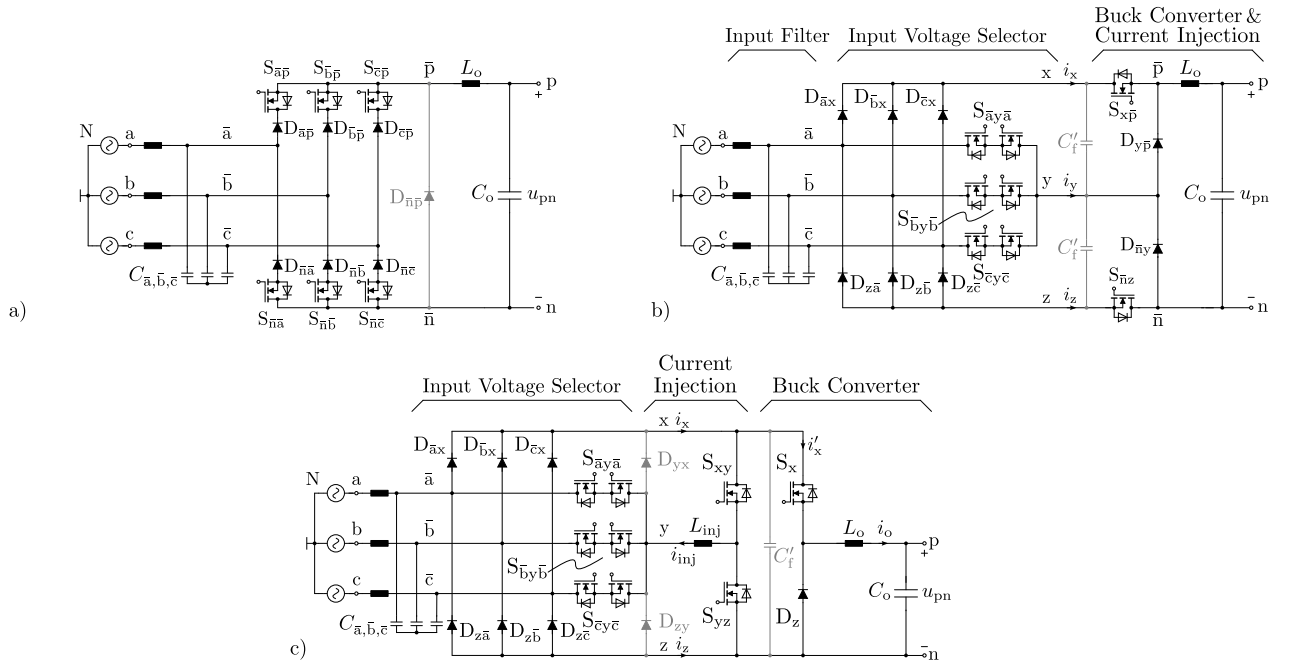

Fig. 2. Three-phase buck-type PFC rectifier topologies: **a)** Conventional six-switch rectifier consisting of an input filter, six reverse blocking switches and a dc link inductor L_o. An additional free wheeling diode $\mathrm{D}_{\bar{\mathrm{n}}\bar{\mathrm{p}}}$ can be used to lower the conduction losses. **b)** SWISS rectifier consisting of an input filter, an Input Voltage Selector (IVS) commutated at mains frequency and two buck converters. **c)** Integrated Active Filter rectifier (IAF), using the same input stage as the SWISS rectifier, combined with a single buck converter providing the output current i_o and a dedicated current injection converter which serves as active harmonic filter for achieving sinusoidal input currents.

provide a constant dc output voltage. Note that the IVS switches and diodes are commutated at mains frequency only which implies that almost no switching losses occur in the IVS. This allows the usage of rectifier diodes $\mathrm{D}_{\bar{\mathrm{k}}\mathrm{x}}$, $\mathrm{D}_{\mathrm{z}\bar{\mathrm{k}}}$ which are optimized for a low forward voltage drop. Two additional capacitors C'_f can be used to shorten the commutation paths of the dc-dc converters.

The circuit topology of the Integrated Active Filter (IAF) buck-type PFC rectifier, shown in **Fig. 2c)**, was first introduced in [14] for three-phase solar inverters. A similar circuit was also proposed for drive systems with small dc-link capacitors [15]. Three major blocks can be identified in the IAF schematic: an Input Voltage Selector which is identical to the SWISS Rectifier, a current injection circuit S_xy, S_yz, L_inj and a dc-dc buck converter S_x, D_z, L_o which provides the constant dc output voltage u_pn. Typically a small capacitor C'_f is required to ensure a valid conduction path during the commutation of S_xy, S_yz and S_x.

For this paper, the Integrated Active Filter buck-type PFC rectifier was selected as starting point for further analysis in **Section II** as only two line-commutated diodes $\mathrm{D}_{\bar{\mathrm{k}}\mathrm{x}}$, $\mathrm{D}_{\mathrm{z}\bar{\mathrm{k}}}$ and one power transistor S_x are in its main conduction path [8]. Using the capital equivalent worth of a watt and component cost models a non-isolated 8 kW PFC rectifier for 380 Vdc distribution systems is designed in **Section III**. This allows selecting cost optimal components such as semiconductors, inductors and transformers achieving an economically optimal converter which minimizes life cycle cost, i.e. the sum of first cost of the converter hardware and the cost of dissipation during the service life. Measurements taken on a hardware prototype are presented in **Section IV**.

TABLE I
CONVERTER SPECIFICATIONS

Input Voltage (Line-to-Neutral)	$U_1 = 230\,\mathrm{V}$ rms
Input Frequency	$\omega_1 = 2\pi\,50\,\mathrm{Hz}$
Switching Frequency	$f_\mathrm{s} = 27\,\mathrm{kHz}$
Nominal Output Voltage	$U_\mathrm{pn} = 400\,\mathrm{V}$
Nominal Output Power	$P_\mathrm{o} = 8\,\mathrm{kW}$

II. CIRCUIT TOPOLOGY

Simulation results for a 8 kW IAF buck-type PFC system (cf. **Fig. 2c**) are shown in **Fig. 3**, for the system specifications given in **Table I**. In the IAF, the current injection circuit and the buck converter can be analyzed, optimized and operated almost independently of each other. As the dc output is provided by the buck converter (S_x, D_z, L_o), the output current i_o and voltage u_pn can be controlled independently of the injection circuit. This can be seen from the simulation results in **Fig. 3**: During $\omega t < 180°$ the current injection circuit is turned off, i.e. $i_\mathrm{inj} = 0$. As the buck converter creates a constant output current i_o it consumes constant power from the ac input. Hence non-sinusoidal ac input currents $i_\mathrm{a,b,c}$ result and only two ac input phases $i_\mathrm{a,b,c}$ conduct current at a time.

For $\omega t > 180°$ the injection circuit is used to create a current i_inj which is proportional to the voltage u_yN:

$$i_\mathrm{inj}(\omega t) = -\hat{I}_1 \, \frac{u_\mathrm{yN}(\omega t)}{\hat{U}_1} \tag{1}$$

where $\hat{I}_1$ is the peak value of the rectifier's ac input current and $\hat{U}_1$ is the ac phase-to-neutral voltage amplitude. This results in sinusoidal ac input currents as shown in **Fig. 3**.

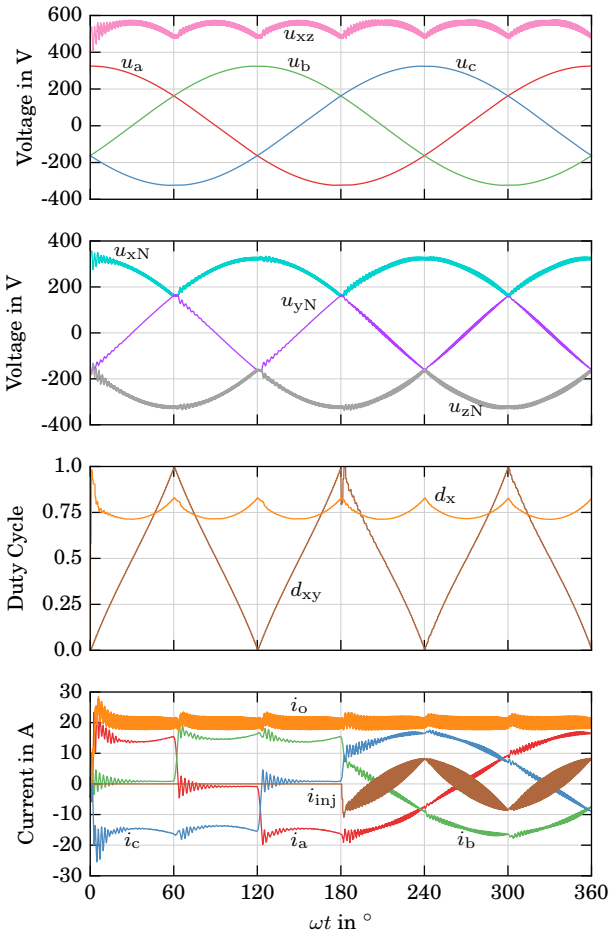

Fig. 3. Simulation results for an Integrated Active Filter (IAF) buck-type PFC rectifier as in **Fig. 2c)**, showing the ac input voltages $u_{a,b,c}$, the IVS output voltages u_{xN}, u_{yN} and u_{zN}, the buck converter duty cycle d_x, duty cycle d_{xy} of switch S_{xy}, the output current i_o, the injection current i_{inj} and the ac input currents $i_{a,b,c}$. During $\omega t < 180°$ the injection circuit is disabled (i.e. $i_{inj} = 0$) which results in non-sinusoidal mains currents $i_{a,b,c}$.

A more detailed description of the modulation and control strategy can be found in [8].

A. Input Voltage Selector

As described above, the IAF rectifier uses an Input Voltage Selector, which connects each ac input phase a, b, c to either node x, y or z. This implies that the voltages u_{xN}, u_{yN} and u_{zN} are piecewise sinusoidal, which allows to move the ac filter capacitors $C_{\bar{a},\bar{b},\bar{c}}$ from nodes $\bar{a}, \bar{b}, \bar{c}$ to nodes x, y, z as shown in **Fig. 4**. This shortens the commutation paths of the buck converter and the injection switches. Additionally the ripple of the diode bridge currents i_x and i_z reduces which reduces the conduction losses in full-wave diode bridge $D_{\bar{k}x}$, $D_{z\bar{k}}$ [16].

B. Buck Converter

It can be seen in **Fig. 2c)** that the buck converter's input is connected to u_{xz} which is a six-pulse shaped voltage provided by the IVS' full bridge rectifier, cf. **Fig. 3**. Neglecting any

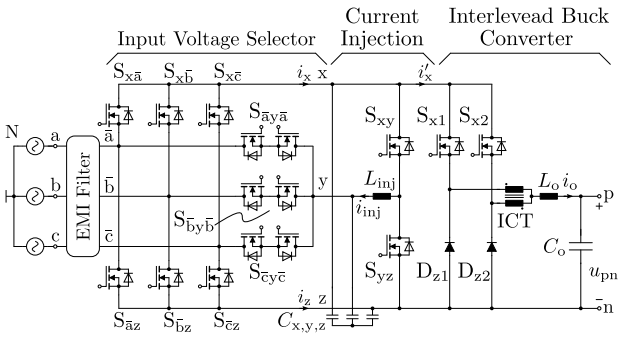

Fig. 4. Schematic of the IAF rectifier where the input filter capacitors have been moved from the ac side ($\bar{a}$, $\bar{b}$, $\bar{c}$) of the IVS to its output side (x, y, z), which reduces the conduction losses [16]. The diodes $D_{\bar{k}x}$, $D_{z\bar{k}}$ are replaced with SiC MOSFETs $S_{x\bar{k}}$, $S_{\bar{k}z}$ operating as synchronous rectifiers to further increase the efficiency. An interleaved buck converter with cells S_{x1}, D_{z1} and S_{x2}, D_{z2} is used where S_{x1} and S_{x2} are controlled with 180° phase shifted PWM signals. This lowers the current ripple in i'_x which leads to a lower voltage ripple at the input filter capacitors $C_{x,y,z}$. The buck converter output inductors are implemented as a close-coupled inter-cell transformer (ICT) and single output inductor L_o.

voltage drops across the semiconductors and inductors, the dc output voltage u_{pn} can be expressed as:

$$u_{pn} = \frac{3}{2}\,\hat{U}_1\,M \quad M \in [0,1] \tag{2}$$

where $\hat{U}_1$ is the ac phase-to-neutral voltage amplitude and M is the converter's modulation index. Note that this relationship is valid for all three buck-type topologies shown in **Fig. 2** [8].

A small distortion of the output current occurs at every 60° sector of the ac input voltage, ie. at the intersection of two phase voltages $u_{a,b,c}$. This is most likely due to the switching frequency ripple of the filter capacitor voltages u_{xN}, u_{yN}, u_{zN} as similar disturbances exist in the SWISS rectifier [16].

If a conventional single-phase buck converter is used as shown in **Fig. 2c)** a discontinuous input current i'_x results which causes a switching frequency voltage ripple across the input filter capacitors $C_{x,y,z}$. As these capacitors are connected to the three-phase ac input of the converter they generate reactive power and hence reduce the rectifiers power factor. Therefore, the reactive power is typically limited to 5 % to 10 % of the converter's active power rating.

C. Interleaved Buck Converter

In order to reduce the input current ripple and hence the electromagnetic noise emission of the rectifier, an interleaved buck converter can be used, as shown in **Fig. 4**. By modulating the switches S_{x1} and S_{x2} with 180° phase shifted PWM signals the peak-to-peak ripple in i'_x is reduced by approximately a factor of two and the ripple frequency is twice the switching frequency due to the cancellation of harmonics.

The dc output filter for the interleaved buck converter can be implemented by a combination of a close-coupled inter-cell transformer (ICT) and a single inductor instead of two separate inductors. Using ICTs for interleaved dc-dc converters has been extensively described in literature and it has been shown to result in a reduction of the magnetic component's volume, losses and weight [17–19].

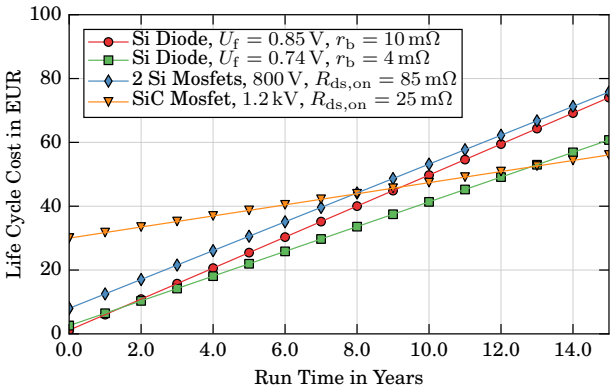

Fig. 5. Comparison of life cycle cost for different implementations of the six-pulse rectifier $D_{\bar{k}x}$, $D_{z\bar{k}}$ with $I_{rms} = 8.1\,A$, $I_{avg} = 4.6\,A$ ($P_o = 8\,kW$) and a capital equivalent worth of EUR 0.12 per kW h [2]. Switching losses are neglected as the IVS commutates at twice the mains frequency only. It can be seen that the significantly higher first cost of a SiC MOSFET is compensated by the reduced conduction losses of the device achieving roughly the same total life cycle cost as Si diodes and Si MOSFETs for run times of approximately ten years, assuming continuous operation at rated power.

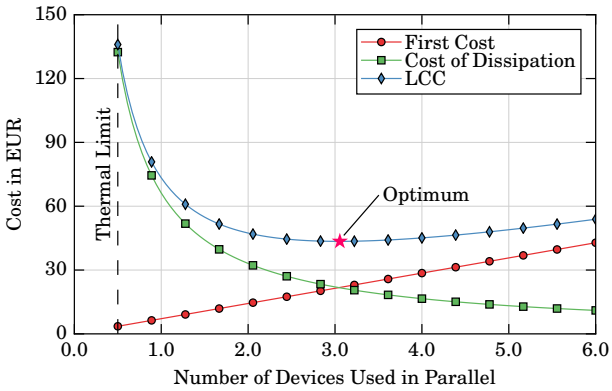

Fig. 6. First cost, cost of dissipated energy and life cycle cost (LCC) as a function of the number of devices connected in parallel for the six-pulse rectifier $S_{x\bar{k}}$, $S_{\bar{k}z}$ at nominal operation with $I_{rms} = 8.1\,A$ ($P_o = 8\,kW$). A SiC MOSFET with $R_{ds,on} = 96\,m\Omega$ and a cost of EUR 7.14 is considered as unit device together with a capital equivalent worth of $\gamma =$ EUR 0.12 per kW h and a run time of $t_r = 10$ years.

III. Design and Optimization

As described in [2] the capital equivalent worth of one watt of continuous dissipation can be used to select components in order to minimize the total life cycle cost. Combined with component cost models, the switching frequency, semiconductors and magnetic components are selected to achieve minimal life cycle cost for a given service life time assuming continuous operation at rated power [20]. A hard switching converter design was chosen for the analysis because of the simpler modulation and control, the lower noise emission, the lower peak and rms currents in the switches and magnetics and the comparatively low switching losses of modern SiC semiconductor devices.

A calculation example for the input voltage selector diodes $D_{\bar{k}x}$, $D_{z\bar{k}}$ is shown in **Fig. 5**, where a capital equivalent worth of $\gamma =$ EUR 0.12 per kW h (approximately USD 0.13 at time of publication) is assumed. Neglecting switching losses in the IVS, the device losses can be directly determined from the rms and average currents found by numerical simulation, resulting in $I_{rms} = 8.1\,A$ and $I_{avg} = 4.6\,A$ for an 8 kW system. Assuming a service life time of 10 years or more, a SiC MOSFET with a high initial cost of approximately EUR 30 and low on state resistance achieves the same or lower life cycle cost than conventional Si diodes with an initial cost of EUR 2.6. The same holds for a parallel connection of two Si MOSFETs with a first cost of approximately EUR 8. Note that all devices are operated far below their thermal limits, 1.7 W of conduction losses result for the SiC MOSFTEs, $\approx 4\,W$ for the Si diodes and Si MOSFETs while all devices are rated for more than 100 W of continuous power dissipation. Therefore the full wave rectifier in the IVS is implemented with SiC MOSFETs operated as synchronous rectifiers as shown in **Fig. 4**.

A. Minimizing Life Cycle Cost

The life cycle cost shown in **Fig. 5** is based on a selection of standard semiconductor devices. Using more than one device in parallel reduces the total on-state resistance $R_{ds,on}$ of MOSFETs or the bulk resistances r_b of diodes which lowers the conduction losses. This reduces the cost of dissipation during system operation, but increases the first cost as more devices are used. This implies that the resulting life cycle cost is a function of the number of devices used in parallel. For a MOSFET continuously conducting the current I_{rms} for the run time t_r without switching losses the corresponding LCC Λ can be expressed as:

$$\Lambda_M(n) = \underbrace{\gamma \frac{R_{ds,on}}{n} I_{rms}^2 t_r}_{\text{Cost of Dissipation, } \Gamma_M} + \underbrace{\sigma_M n}_{\text{First Cost, } \Sigma_M} , \qquad (3)$$

where σ_M is the cost of a single MOSFET device with an on-state resistance $R_{ds,on}$ and n is the number of devices connected in parallel. A plot of the resulting values for $t_r =$ 10 years and a SiC MOSFET with $R_{ds,on} = 96\,m\Omega$ and $\sigma_M =$ EUR 7.14 is shown in **Fig. 6**. For a given device technology and a run time t_r an optimal number of devices n_{opt}, which achieves minimal life cycle cost, can be derived by minimizing (3) with respect to n:

$$n_{opt} = \sqrt{\gamma\, t_r \frac{R_{ds,on}}{\sigma_M}}\, I_{rms} , \qquad (4)$$

$$\Gamma_{M,opt} = \Sigma_{M,opt} = \sqrt{\gamma\, t_r\, R\, \sigma_M}\, I_{rms} , \qquad (5)$$

$$\Lambda_{M,opt} = \Gamma_{M,opt} + \Sigma_{M,opt} = 2\sqrt{\gamma\, t_r\, R\, \sigma_M}\, I_{rms} . \qquad (6)$$

This implies that n is not a free parameter of a converter design if LCC is considered. For a given run time t_r an optimal n exists which corresponds to an optimal $R_{ds,on}$.

Note that a certain minimum n_{min} exists due to the thermal limits of the device and the cooling system as indicated in **Fig. 6**. However, even for short run times of $t_r \approx 1$ year the optimal n is typically larger than n_{min}. Furthermore n does not necessarily have to be an integer number as semiconductor devices are usually available in a range of different chip sizes and hence $R_{ds,on}$ values in the same package. As the obtained LCC function $\Lambda(n)$ is flat around the optimum (cf. **Fig. 6**) one or more devices suitable for an implementation can typically be found.

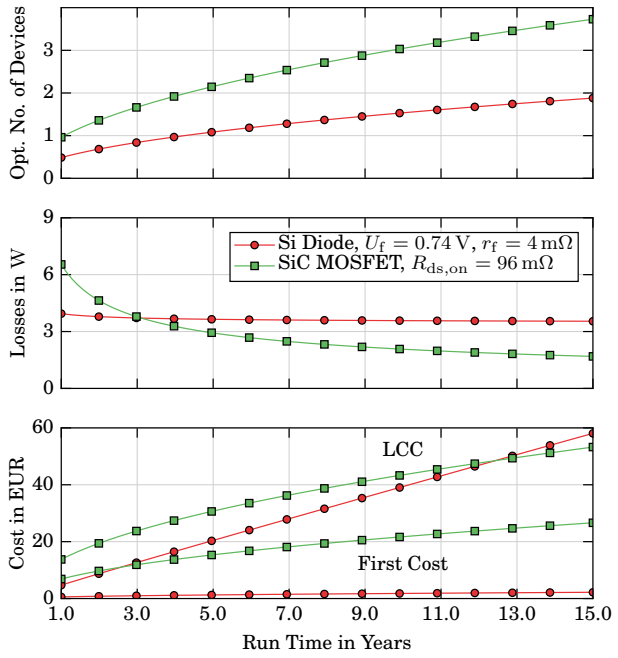

Fig. 7. Optimization results for Si Diodes and SiC MOSFETs showing the optimal (lowest LCC) number of parallel devices, resulting devices losses, first and life cycle cost as a function of the total run time t_r in years. The same parameters as in **Fig. 6** are used.

This optimization can be extended from MOSEFTs to diodes modeled by a constant forward voltage drop U_f connected in series with a bulk resistance r_b. In this case the optimal number of diodes connected in parallel does not depend on U_f, however the losses and hence the cost of dissipation Γ increases. An example calculation for different run times is shown in **Fig. 7** where a $96\,m\Omega$ SiC MOSFET and Si diode with $U_f = 0.74\,A$ and $r_b = 4\,m\Omega$ are considered as unit elements. For both, MOSFETs and diodes the optimal n increases proportional to $\sqrt{t_r}$, however for Si diodes the resulting losses show little variation due to U_f. As the first cost of the considered diode is ≈ 6 times lower than the MOSFET's the Si diodes achieves lower LCC for small t_r while the SiC MOSFET achieves lower LCC for $t_r \geq 12.5$ years.

B. Global Optimization Algorithm

The algorithm outlined above can also be extended to include switching losses of the semiconductors and to magnetic components. The basic optimization procedure for a full rectifier system then works by sweeping over all relevant switching frequencies f_{sw} and considered run times t_r. For each tupel (f_{sw}, t_r) and all components k of the system an optimal relative size $n_{k,opt}$ can be determined which achieves minimal life cycle cost $\Lambda_{k,opt}$ for component k. This implies that all components (e.g. switches, inductors, etc.) can be designed independently of each other which simplifies the optimization procedure. Once all components have been selected, their life cycle costs can be summed up which yields the system's LCC for the considered (f_{sw}, t_r):

$$\Lambda_{sys}(f_{sw}, t_r) = \sum_k \Lambda_{k,opt}(f_{sw}, t_r) \tag{7}$$

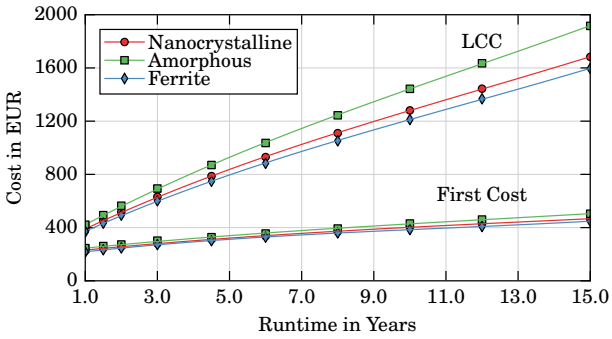

Fig. 8. Minimal achievable life cycle cost and according first cost of optimal converter designs as a function of run time for different inductor core materials. It can be seen that for a run time of ten years, the first cost is $< 30\,\%$ of the total life cycle cost. The optimization results in similar first costs for all three core materials, however the life cycle cost of designs with ferrite and nanocrystalline inductors is slightly lower compared to solutions with amorphous cores.

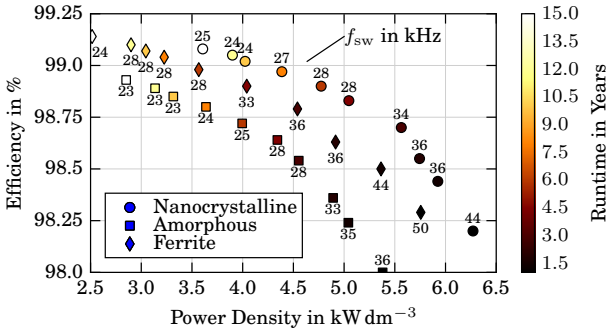

Fig. 9. Optimization results showing power density, efficiency and switching frequency f_{sw} of designs achieving minimal life cycle cost for different run times and inductor core materials of ICT, L_{inj} and L_o.

Once all designs have been calculated the switching frequency achieving lowest overall LCC is selected for each t_r considered in the analysis:

$$\Lambda_{sys,opt}(t_r) = \min_{f_{sw}} \Lambda_{sys}(f_{sw}, t_r) \tag{8}$$

C. Semiconductors

As shown in **Fig. 5** SiC MOSFETs achieve similar life cycle cost as Si devices for a run time of approximately 10 years if only conduction losses are considered. This implies that SiC MOSFETs clearly outperform Si devices for the hard switching elements S_{xy}, S_{yz} and $S_{x1,2}$. Therefore, SiC MOSFETs were considered for the IVS components and active switches in the buck converter and the current injection circuit. SiC Schottky diodes are considered for the buck converter free wheeling diodes $D_{z1,2}$.

D. Magnetic Components

The dimensioning of magnetic components is performed with a similar algorithm: for a given switching frequency the current and voltage stresses created by the converter can be determined. For a given core material, shape and size the optimal number of turns, which minimizes the sum of core and winding losses, can then be found by numerical optimization methods. Using the losses and cost models for core and winding materials the inductor's life cycle cost can

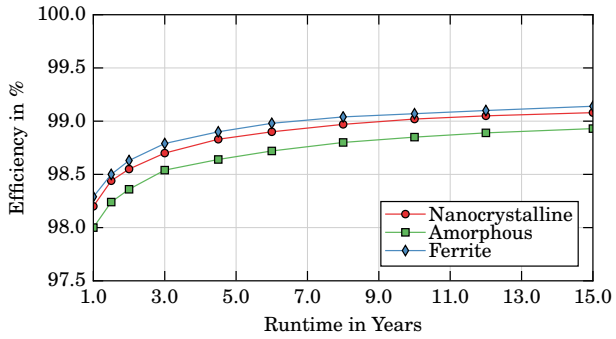

Fig. 10. Efficiency of life cycle cost optimal converter designs for different run times and core materials.

be calculated, which allows the selection of an optimal core size achieving minimal LCC for the given design point.

Note that different core and winding materials can only be compared at the full system level as the resulting losses depend strongly on design parameters such as the switching frequency. Ferrites, for example, typically feature lower core losses but also lower saturation flux densities than tape wound cores which makes ferrite more suited for higher switching frequencies. In this paper amorphous and nanocrystalline tape wound cores with helical windings made from rectangular wire as well as ferrite cores with solid round wire have been considered.

E. Auxiliary Components

The losses, volume and cost of other components, such as gate drive circuits, DSP/FPGA, capacitors, PCBs, heat sinks, fans, EMI filter, etc have to be considered as well. While their contribution to the overall converter volume, and life cycle cost can be significant, they are almost independent of the design point in the considered application. Therefore auxiliary components have been considered in the design but were not part of the optimization.

F. Optimization Results

Fig. 8 shows the achievable minimal life cycle cost $\Lambda_{sys,opt}(t_\mathrm{r})$ and the resulting first cost $\Sigma_{\mathrm{sys,opt}}(t_\mathrm{r})$ as a function of run time as calculated by the optimization outlined above. It can be seen that the first cost of the optimal systems is less than 30 % of the total life cycle cost for a run time of 10 years or more. Furthermore, the life cycle cost is comparable for all three core materials considered in the optimization. Designs using amorphous cores are expected to have slightly higher LCC than systems with nanocrystalline or ferrite cores, which is due to the higher core losses of amorphous materials.

However, the volumes and switching frequencies of the designed converters differ significantly as shown in **Fig. 9**, the resulting efficiency as function of t_r is shown in **Fig. 10**. For short run times (≤ 2 years) converters with high switching frequencies and high power densities achieve minimal LCC as opposed to long run times (≥ 10 years) where designs with approximately half the switching frequency, twice the volume and half the losses result. Furthermore, these results show that very high efficiencies of up to 99 % are economically feasible with available state-of-the-art SiC switches and core materials. Note that three-phase rectifiers based on Si and SiC MOSFETS with slightly lower efficiencies have been reported in the literature [21, 22], however without considering cost.

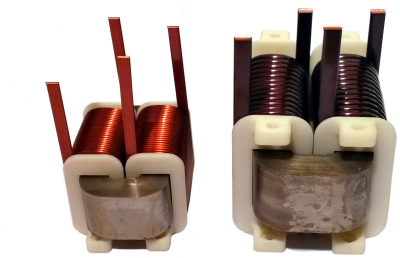

Fig. 11. Picture of L_inj and L_o, implemented using nanocrystalline C cores and helical windings. A boxed volume of 88 cm^3 and 249 cm^3 results for the two inductors.

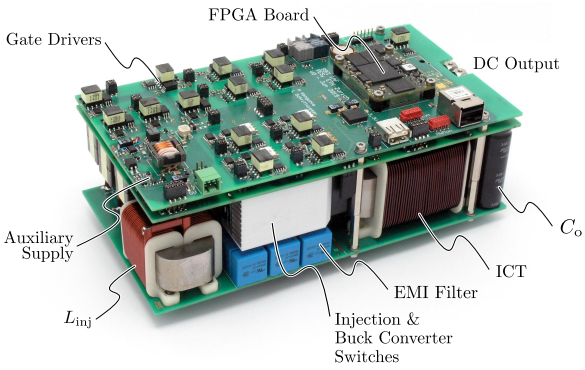

Fig. 13. Picture of the hardware prototype, measuring 220 mm x 118 mm x 77 mm (8.66 in x 4.65 in x 3.03 in). This results in a power density of 4.0 kW dm^{-3} (65 W in^{-3}).

G. Selected Design

Based on the numerical optimization results the design point with $t_\mathrm{r} = 10$ years, $f_\mathrm{sw} = 27$ kHz, a power density of 4.0 kW dm^{-3} and an efficiency of 99 % was selected to implement a hardware prototype. *FINEMET* nanocrystalline cores with helical windings (cf. **Fig. 11**) are used as they achieve considerably higher power density compared to designs based on ferrite. Detailed design results are shown in **Fig. 12**: for systems with a run time of 10 years or more, it can be seen that the semiconductors and heat sinks contribute about half of the first cost, life cycle cost and losses, but only about 10 % to 20 % of the total volume. Furthermore, the auxiliary components, such as PCBs, gate drivers, FPGA/DSP etc. have a significant contribution to both first cost and life cycle cost which implies that they cannot be neglected in the design process.

IV. Hardware Prototype

Using the optimization results presented in the previous chapter an 8 kW, prototype rectifier with a switching frequency of $f_\mathrm{sw} = 27$ kHz, according to the specifications given in **Table I**, was implemented. A picture of the hardware is shown in **Fig. 13**.

A more detailed distribution of the calculated component losses for the implemented prototype at nominal operating conditions and the corresponding component volumes are shown in **Fig. 14**. About 50 % of the total losses occur

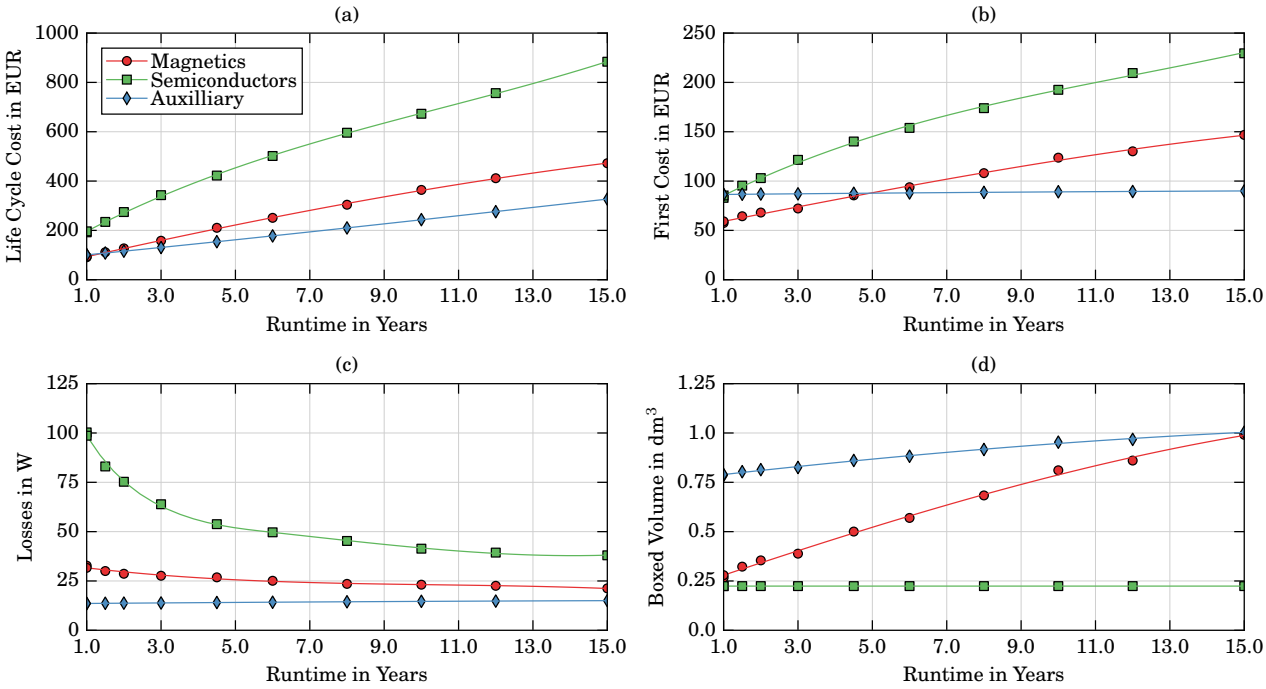

Fig. 12. Spline interpolated results of the numerical optimization (markers) for the semiconductors (incl. heatsinks), magnetics and remaining components (e.g. fans, gate drivers, PCBs, DSP/FPGA, capacitors, EMI filter) of the circuit shown in **Fig. 4**. Nanocrystalline cores with helical windings are used for all magnetic components as they offer the best performance in this case, cf. **Fig. 9**. Plot **a)** shows the optimal life cycle cost $\Lambda(t_\mathrm{r})$, **b)** shows the corresponding optimal first cost $\Sigma(t_\mathrm{r})$, **c)** the losses occurring in the components and **d)** their boxed volume. It can be seen that the semiconductors contribute about half of the first cost and losses and hence the life cycle cost, but only $\approx 10\,\%$ to $20\,\%$ of the total converter volume.

in the semiconductors of which approximately one third are switching losses. Core and winding losses in the main magnetic components L_o, ICT and L_inj account for $\approx 22\,\%$ of the total losses. The remaining $28\,\%$ occur in the EMI filter, the PCB tracks, and other elements such as fans, gate drivers, FPGA, current sensors etc. Measurement results of the prototype converter are presented in the following.

A. AC Input Currents

In **Fig. 15** measurement results of the prototype rectifier operated at full load and nominal input voltage are shown. Sinusoidal input currents with slight distortions at the mains voltage sector boundaries result as expected from simulation.

B. Efficiency

A comparison of the rectifier's calculated and measured efficiency as a function of dc output power is shown in **Fig. 16**. The solid lines show the calculated efficiency for $400\,\mathrm{V}$ and $380\,\mathrm{V}$ output voltage, while the round and triangular markers show measurements taken with a *Yokogawa WT 3000* power analyzer. Additionally three efficiency measurements were taken based on a direct measurement of the converter's losses using a calorimeter which closely match the values obtained by the electrical measurement.

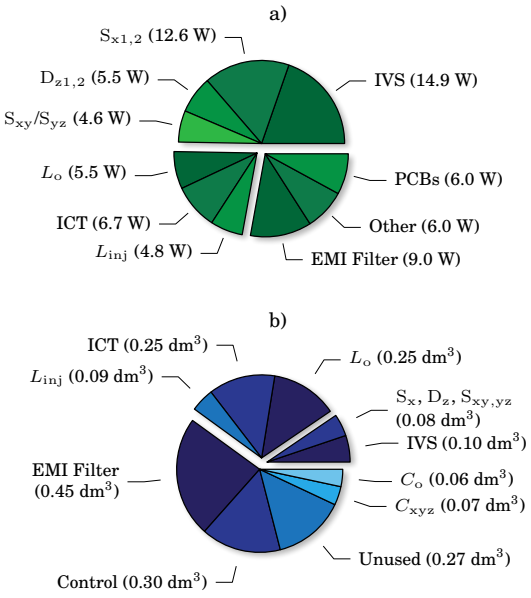

Fig. 14. The calculated distribution of losses for the selected design point at nominal operation is shown in **a)**, the corresponding component volumes are shown in **b)**. Category *other* includes fans, gate drivers, FPGA, ADCs, current sensors, auxiliary supply, etc.

V. Conclusion

This paper describes a life cycle cost driven optimization process were not only the first cost of a converter, but also the capital equivalent worth of the energy dissipated during the system's service life is considered. This allows the selection of optimal components, such as switches, inductors, transformers, etc. which achieve minimal cost for a given application, run time and switching frequency. By sweeping over a range of suitable switching frequencies a cost optimal converter system can then be found.

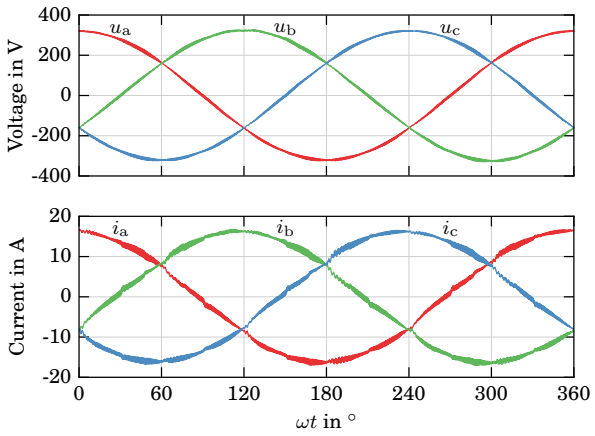

Fig. 15. Measurement results with the converter operating at nominal conditions and full output power, i.e. $P = 8\,\mathrm{kW}$, $U_1 = 230\,\mathrm{V_{rms}}$ and $U_{\mathrm{pn}} = 400\,\mathrm{V}$. Note that phase quantities a and c were measured directly, phase b was recreated numerically as $u_\mathrm{b} = -u_\mathrm{a} - u_\mathrm{c}$ and $i_\mathrm{b} = -i_\mathrm{a} - i_\mathrm{c}$.

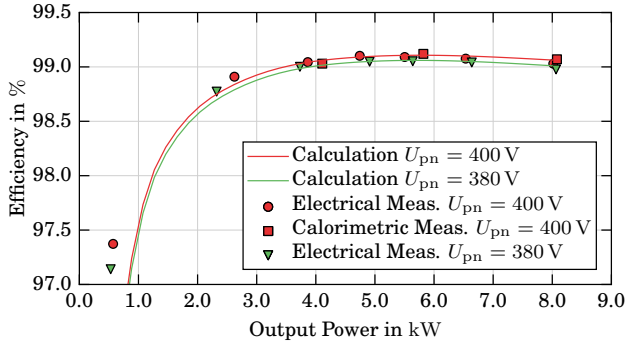

Fig. 16. Comparison of measured and calculated converter efficiencies for two different dc output voltages U_{pn}. The electrical efficiency measurements were performed with a *Yokogawa WT 3000* power analyzer. For $U_{\mathrm{pn}} = 400\,\mathrm{V}$ additional measurements were done using a calorimeter. All measurements were taken at nominal ac input voltage $U_1 = 230\,\mathrm{V_{rms}}$ and an ambient temperature of 30 degrees C.

As an example an 8 kW buck-type three-phase interleaved Integrated Active Filter rectifier for 380 V dc distribution systems in data center and telecommunication applications is designed. Using state-of-the-art SiC MOSFETs and nanocrystalline cores a design with a power density of $4\,\mathrm{kW\,dm^{-3}}$ and an efficiency of 99 % results. Measurement results taken on a hardware prototype verify the validity of the employed models.

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