NEW LOSSLESS TURN-ON AND TURN-OFF (SNUBBER) NETWORKS FOR INVERTERS, INCLUDING CIRCUITS FOR BLOCKING VOLTAGE LIMITATION

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ABSTRACT

Transistorized pulse width modulated (PWM) inverters require careful dimensioning of turn-on and turn-off circuits in order to minimize the switching loss in the power transistors. The paper describes new lossless circuits. Especially the turn-off circuits show a highly reduced part count as compared to circuits known from the literature. Also the turn-on circuits apply energy recovery. Furthermore, due to a special circuit, the voltage across the power transistor is strictly limited. This is very important especially due to the usually low voltage blocking capability of high current power transistors.

1. INTRODUCTION

In general, turn-on and turn-off networks (snubbers) are circuits used for reduction of the switching losses of the power devices in power electronic circuits. These networks are situated in series or in parallel to the power devices, respectively. The power devices taken into account in this paper are mainly power transistors (and GTOs). One major purpose of using such snubbers is also to keep the power device operating within its SOAR (safe operating area).

Two different types of snubbers can be defined: dissipative and nondissipative (lossless) types. While the term nondissipative is based on an idealization, the underlying basic difference can be defined as follows:

(1) In dissipative snubbers the whole energy stored in this network is converted into heat (1, 2, 10). This type obviously is not qualified for high switching frequencies and/or high switched power levels.

(2) Nondissipative snubber networks really should be called snubbers with low losses or, better, snubbers without fundamental losses. Losses are only caused by the nonideal device properties, such as conduction and switching losses of the switching devices contained in the snubber networks (2). It is certainly possible, as frequently realized, to combine dissipative turn-on networks with nondissipative turn-off networks and vice versa (1, 3).

Since the losses of dissipative snubbers reduce the efficiency of power electronic circuits to a great extent especially for higher switching frequencies, nondissipative turn-on and turn-off snubbers are used here.

One other important point is the part count of the additional power devices required by the snubbers. The circuits for inverters applied so far use snubbers developed for one switching device (as applied in a chopper). This means multiple application of the same snubber circuits, four times for one phase bridge inverters and six times for three phase inverters. This relatively high part count in many cases is detrimental to practical application due to the additional cost involved. Therefore, a circuit with a reduced part count for inverter application has been developed here.

A final major point to be observed is the maximum voltage across the switching device. Due to the rather limited voltage blocking capability especially of high current power transistors, this parameter is of paramount practical and economic importance. A circuit has been developed here which allows to strictly limit this voltage to a given amount.

2. REQUIREMENTS FOR IDEAL TURN-ON AND TURN-OFF SNUBBERS

The basic requirements stated in the introduction lead to the following points which should be fulfilled by ideal snubber circuits:
(1) No fundamental losses.
(2) Part count as low as possible.

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(3) No additional discharging (and charging) currents caused by the snubbers should flow through the power devices. This is especially important for high operating frequencies, because there high current peaks have to be admitted for fast charging and discharging of the snubber capacitors. This would mean that the power devices would have to be oversized.
(4) No additional switching devices.
(5) No additional voltage and/or current sources for the snubbers should be required. This is especially important for high switching power levels.
(6) It is advantageous to limit the switching strain (voltage and current levels) on snubber circuit devices to the order of magnitude of the (main) switching devices.
(7) High reliability and safety of operation.
(8) The functioning shall be independent of the various operating conditions (such as load current, switching frequency etc.).

It is obvious that not all of the points mentioned can be realized in a practical and economical way. Especially simultaneous fulfilment of (3) and (4) seems to be impossible as will be explained later. If (4) cannot be fulfilled, (7) has to be observed very carefully, e.g., due to the additional control circuits necessary in this case.

3. REALIZATION

3.1. Inverter Structure

In the following the approach used here to come very close to the requirements stated in section 2 shall be described. The power circuit is shown in Fig.1. The circuit used for measurements is a three phase transistor inverter with DC voltage link (440V $\pm$ 10%). The maximum switching frequency is f_{pmax}=50kHz, the maximum load current is i_{Lmax}=200A. For the power switching devices two Darlington configurations are used in parallel where each Darlington consists of three stages. (First stage: power MOS-FET BUZ 88A, Siemens, second and third stage: high power darlington device with a separate fast recovery flyback diode D67FP7, General Electric.)

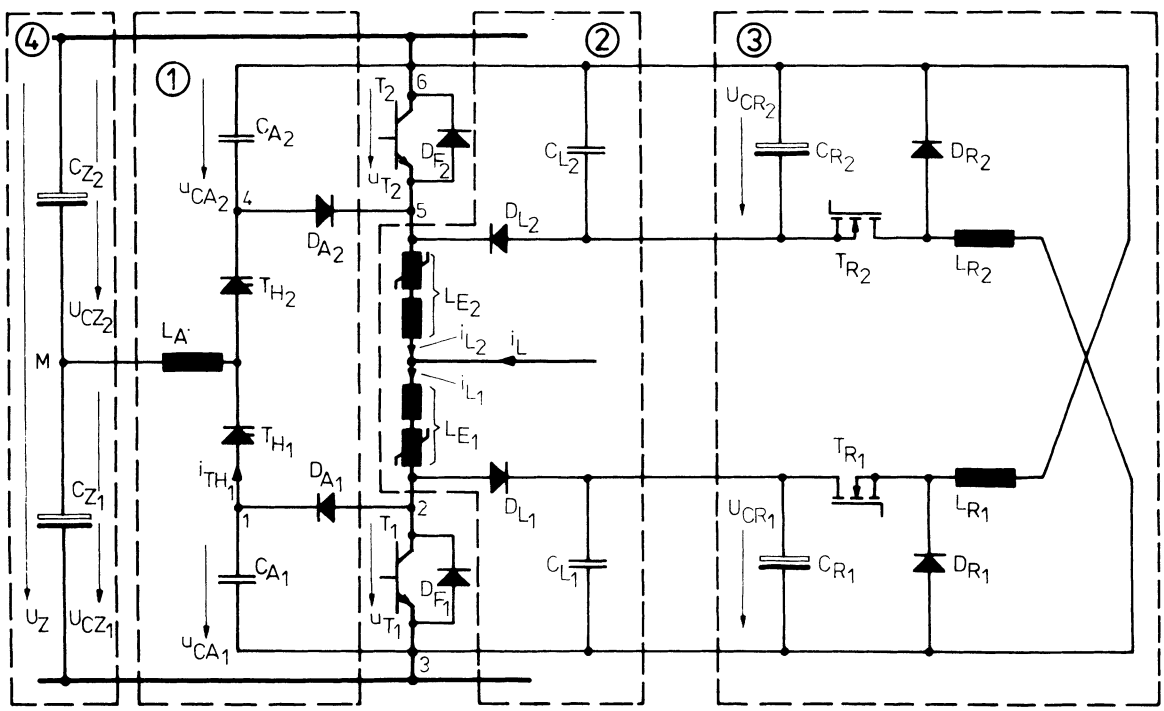

Fig. 1. Pole changer (one phase leg of an inverter)
Block 1: Turn-off snubber (network); 2: Turn-on snubber; 3: Blocking voltage limitation circuit for power switching devices (here: transistors T_1 and T_2) necessary only once also for three phase inverters; 4: Capacitors (for providing a DC voltage link) which form a capacitive center of the inverter supply voltage. This center comes automatically for voltage applications above 450V such as here because this is beyond the usual limit of industrial electrolytical capacitors today. Then capacitors have to be used in series.

3.2. Turn-Off Snubber

Turn-off snubbers are circuits lying in parallel to the power switching device (T,e.g.,T_1,T_2 in Fig.1) whose major element is a capacitor. The load current commutates into the turn-off snubber at turn-off time of T. The dimensioning of the snubber has to be such that the load line always remains within the SOAR (especially within the RBSOAR for negative voltage at the base). Furthermore, the turn-off snubbers are used to reduce the switching loss per switching cycle by shifting the load line towards smaller switching losses in the active region. This makes such snubbers mandatory above a certain operating frequency.

The main problem of the turn-off snubbers lies in proper discharging of the turn-off capacitor. The following possibilities exist:

(a) discharging via a resistance R and the power device T in the conventional RCD-network. The energy stored in the capacitor C_A is dissipated into heat in R and in T, the discharging current is added to the load current;

(b) discharging, e.g., via resonant (ringing) circuits with energy feedback into the DC voltage link. So far this method has employed discharging current also through the power device T (5). In some operating conditions of inverters this method can lead to an even unwanted discharge of the capacitor C_A via the load (when the diode D_F, lying antiparallel to T, is conducting). This effect has in applications been avoided by inserting a diode D_S in series to T. However, on one hand D_S has to carry the load current (which leads to considerable additional losses) and on the other hand this method is only applicable where T and D_F are seperate devices. The latter condition is against today's trend to higher integration. Another method to overcome unwanted discharging is to insert a switching device into the discharging circuit.

Since in all the methods proposed so far the discharging current is added to the load current in T, the new method introduced here applies a discharging method for C_A via an additional switching device. The discharging current does not flow through T.

The function of circuit block 1 in Fig.1 is as follows: when T_1 is turned off (assuming $i_L>0$), C_{A1} is charged via D_{A1}; $i_L$commutates to D_{F2} starting when $u_{CA1}>U_Z$. Always the voltage across T_1 is limited to U_{CR1} (see Fig.2) by a circuit to be described later.

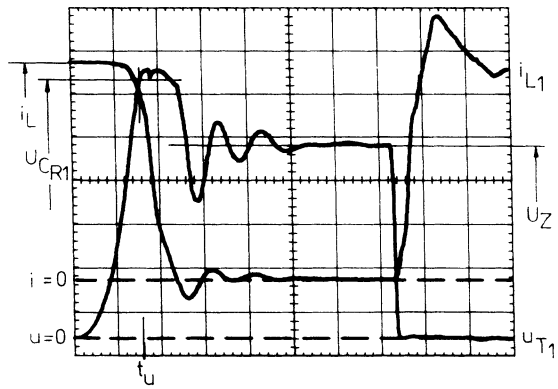

Fig. 2 Turn-on and turn off behavior of T_1 using snubbers; i_L=100A. Scale: i_L, i_{L1}..20A/div (i.e., between full lines); u_{T1}...100V/div; time (horizontal axis)... 2μs/div; for meaning of electrical variables see Fig.1

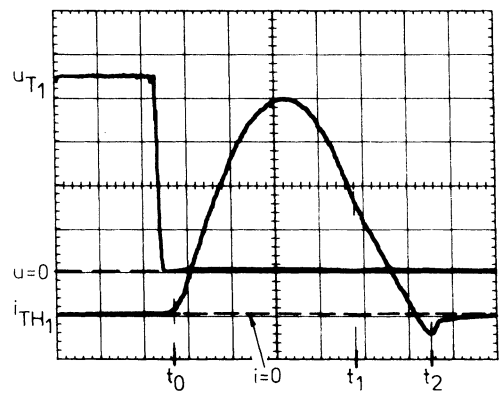

Fig.3 Voltage across power transistor T_1 and current through T_{H1} for illustrating the discharge of the turn-off snubber capacitor C_{A1}. Scale as in Fig.2, only for time.. ..1μs/div.
Here, $u_{CA1}(t=t_o)=U_{CR1}>2U_{CZ1}$.

From Fig.3 it can be seen that at turn-on of T_1 C_{A1} is discharged via L_A into M by turning on thyristor T_{H1}. Thereby the snubber is brought back into its initial status. For M the center of the capacitive voltage divider, built up by the electrolytic capacitors used for providing the inverter DC voltage link, can be applied. Fig.3 shows that for $u_{CA1}=U_{CR1}>2U_{CZ1}$ the current i_{TH1} consists of two different parts. One part (between t_o and t_1) is determined by the circuit C_{A1}-T_{H1}-L_A-C_{Z1}, therefore resulting in a sinusoidal current, U_{CZ1}≈constant. The second part (for t_1, t_2) is linear because there i_{TH1} is determined by the circuit L_A-C_{Z1}-T_1/D_{F1}-D_{A1}-T_{H1} where u_{CA1}=0V for this period (t_1,t_2), U_{CZ1}≈constant. (Whether and where T_1 or D_{F1}conducts depends on the size of i_L.)

Also C_{A2} is discharged into M. For unsymmetries caused by device tolerances, not equal voltages $U_{CR1,2}$ and not equal discharging rates of C_{A1} and C_{A2} the voltage level of M is being shifted. However its final level is stable because the current amplitudes of $i_{TH1,2}$ behave contrary to U_{CZ1}. (E.g., for n times discharging of C_{A1} for once discharging C_{A2} the stable voltage level is $U_{CZ1}=n/(n+1).U_Z$, which relationship can easily be derived by viewing the equilibrium of charges. For given switching frequency the dynamics of the voltage level change of M is dependent on the ratio of the capacitance values of $C_{Z1,2}$ and $C_{A1,2}$.) For always completely discharging of C_{A1}, $u_{CA1}=U_{CR1} > 2U_{CZ1}$ has to be guaranteed. In the limit, i.e. for $U_{CR1}=2U_{CZ1}$ i_{TH1} is quite sinusoidal (Fig.4).

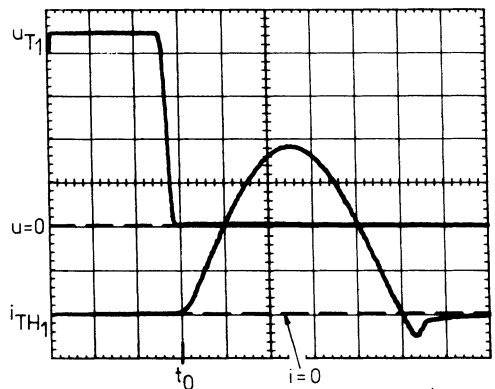

Fig. 4 As Fig. 3, but for $u_{CA1}(t=t_o)=2U_{ZC1}$

A further problem with all low-loss turn-off snubbers lies in the fact that during transistor (in general: the power switching device) turn-off the capacitor has to be charged to a minimum voltage level. This is necessary in order to make possible its complete discharging in one cycle. For given maximum pulse frequency and given snubber capacitor value this load current value $i_{L\varepsilon}$ can be obtained which makes possible the charging of the capacitor up to the minimum voltage required, within the minimum turn-off time. For $i_L < i_{L\varepsilon}$, e.g. after turn-off of T_1 the opposite device T_2 must be turned on (after a time delay to avoid shorting the DC voltage link). It is necessary to turn on T_2 for continuation of charging of C_{A1} via T_2, L_{E1} and L_{E2}. Turning on of T_2 requires (previous) discharging of C_{A2}, here via T_{H2} (in order to provide the turn-off snubber action, as required in most cases, i.e. where $i_{L2} > 0$, for the following turn-off of T_2). When after turn-off of T_2 subsequently T_1 is turned on again, T_1 conducts the sum of load current and charging current for C_{A2} (Fig.5). As mentioned, this is only the case for very small load currents, $i_L < i_{L\varepsilon}$.

The deviation of the current wave from a sine wave is caused by saturating

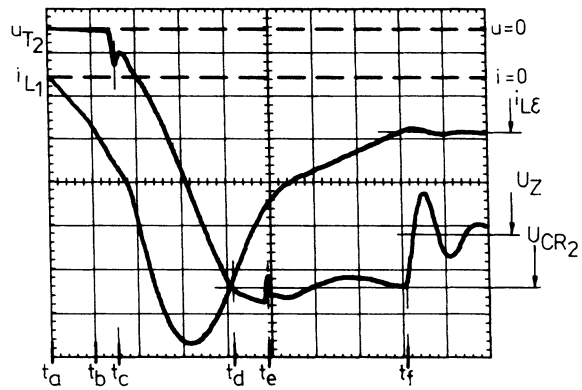

Fig. 5 Recharging of C_{A2} via $L_{E1,2}$ after turning on T_1 and previous conduction of D_{F2} for $0 < i_L < i_{L\varepsilon}$. i_L=25A, U_{CR2}=580V, U_Z=440V. Scale as in Fig.3.

t_a...turn-on of T_1 (L_{E1} not in saturation, L_{E2} in saturation)

t_b...L_{E1} going into saturation

t_c...D_{F2} ceases to conduct, the current commutates into C_{A2}, D_{A2}. The voltage spike is caused by the lead inductances in the circuit 4, 5, 6.

t_d...u_{CA2} reaches U_{CR2}, which means that the condition for the subsequent complete discharging of C_{A2} (in the next cycle) is fulfilled, see text

t_e...D_{A2} ceases to conduct; the voltage spike is caused by the sudden end of the reverse current in D_{A2}

t_e - t_f...demagnetization of L_{E1} and L_{E2} by U_{CR2} - U_Z (lying directly across L_{E1} and L_{E2} in series)

t_f...L_{E1} and L_{E2} are demagnetized; u_{T2} approaches U_Z via a damped oscillation which is caused by an R-C-snubber attached to D_{F2}; additional snubbers (not shown in Fig.1) are necessary to sufficiently reduce the rate of voltage rises across T_2 at turn-off of D_{F2}.

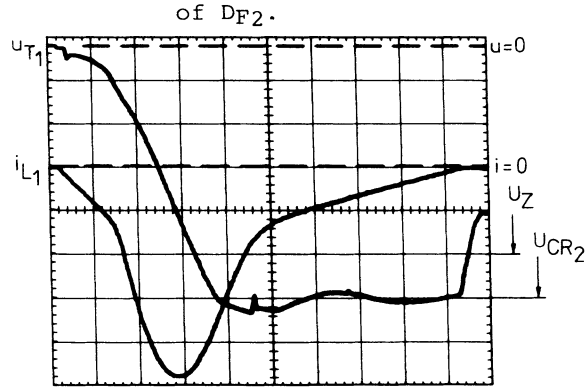

Fig. 6 As Fig.5, but $i_L \approx 0$ (no load condition).

reactors in the inverter leg whose purpose is described later. The voltage form of u_{T2} from t_d on essentially corresponds to the voltage form occurring at turn-off of $T_{1,2}$ (see Fig.2). Figure 6 shows the conditions for load current ≈0. As can be seen from Fig.5, the recharging current of C_{A2} is added to the load current (which is commutated from D_{F2} to T_1). Then T_1 has to carry both, the load and the recharging current. As indicated, for $i_L > i_{L\varepsilon}$ no additional charging is necessary. Therefore, for such i_L the opposite transistor is not turned on and its associate turn-off snubber is not being discharged. Then by proper dimensioning of $L_{E1,2}$ it also becomes possible to keep the sum of $i_{L\varepsilon}$ and the peak of the charging current below $i_{Lmax}+i_{DFLmax}$. There, i_{Lmax}...maximum load current, i_{DFLmax}...peak reverse current through D_F for i_{Lmax} (see Fig.2). A further aspect for dimensioning of $L_{E1,2}$ is the recharging time period t_{ch} given by $C_{A1,2}$ and $L_{E1,2}$. This time period has to be coordinated with the maximum pulse frequency. t_{ch} extends at least from t_a to t_d. With these facts the dimensioning of the transistors with respect to the current is practically given by the load current.

Guidelines for dimensioning of $L_{A1,2}$ and of the thyristors $T_{H1,2}$ are given in the following: For given turn-off capacitances $C_{A1,2}$ and minimum pulse duration the value of L_A is fixed; there, the linear part of the discharging current $i_{TH1,2}$ and the quenching time of the thyristors $T_{H1,2}$ have to be taken into account. The discharge current peaks (Figs. 4,5) may reach high levels where high maximum pulse frequencies are to be handled.

3.3. Turn-On Snubber

3.3.1. General Concepts. In general, turn-on snubbers are based on an inductance connected in series with the transistor T (power switching device). Thereby at turn-on of T a load line shall be maintained within the FBSOAR (forward bias SOAR). In particular, the snubbers reduce the turn-on switching loss in T.(If one considers circuits with no snubbers at all, but certainly load lines within the SOAR, in general the turn-off switching losses will dominate.) The second task of the turn-on snubber is to reduce the reverse current peak through D_F. The D_F to be considered here is the one lying in antiparallel to the opposite T. This D_F has been carrying the load current before turning on that T now to be considered for turn-on. The reverse current peak through D_F is being added to the load current in T being turned on. It is evident that diodes with high reverse currents (especially such diodes with high reverse recovery time) make oversizing of the transistors T necessary.

Similarly to the turn-off snubber, also here the problem of handling the energy originating from the snubber action is to be treated. This energy is stored in the snubber. Basically there are two methods for handling this energy, but both methods are associated with a blocking voltage increase across the transistors:

(a) Dissipation of the magnetic energy into heat in resistors, Zener diodes etc.
(b) Basically lossless energy feedback into the DC voltage link (or into another additional DC voltage source (2)).

Only method (b) is of interest here. There again two approaches can be given:
(b1) Energy feedback via power converters (working in turn as flyback and forward converters) into the DC voltage link (4). The problems encountered here are high blocking voltages across the transistors, across the diodes (lying on the secondary (4)) or across both, transistors and diodes. In practical applications this problem is increased by the transformer stray inductances which cause further increase of the transistor blocking voltages.

(b2) Limitation of the blocking voltage across the transistor (in general: the power switching device) to a defined value (being larger than the DC link voltage value). The magnetization energy is transferred into the limitation circuit, consisting of an energy storage with a possibility of energy feedback into the DC voltage link.

Method (b2) is realized here. The energy storage mentioned for any n-phase bridge application is required only twice (once for the upper half bridge, once for the lower half). This means a substantial reduction of the part count as compared to already known systems, e.g., for three phase applications. The energy storage is realized as a capacitor whose voltage is kept constant by a step down converter feeding into the DC voltage link (block 3 in Fig. 1). (Basically also other methods for energy feedback are thinkable.)

3.3.2. Energy Relationships of Block 2 (Fig. 1). Block 2 is only operational with block 3. The initial conditions shall be given by $i_L>0$, T_1 turned off; i_L is flowing through D_{F2}. At turn-on of T_1 the sum of the load current i_L and the reverse recovery current of D_{F2} will be taken over by T_1 (Fig. 7). From t_x on D_{F2} ceases to conduct; the energy stored in L_{E2} (due to the reverse recovery current spike) will be completely transferred to C_{R2} and C_{L2}. For the energy stored in L_{E1} this is only true for the part above the energy value associated with the load current (see Fig. 6,

interval t_x, t_y). C_{L2} is a small condenser with low inductance, lying in parallel to C_{R2}. C_{L2} keeps transistor blocking voltage spikes small (see t_x in Fig. 7) which are caused by lead inductances between point 5 in Fig. 1 and C_{R2}.(It should be reminded of the fact that C_{R2} is common to all power switches of the upper half bridge. Other devices, such as C_{L2} (or C_{Li}) and D_{L2} (or D_{Li}) are needed for each power switching device seperately.).

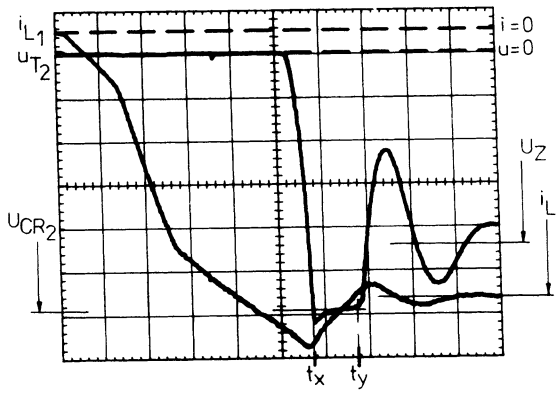

Fig. 7 Current commutation from D_{F2} to T_1. The nonlinear current behavior is caused by the saturating inductances $L_{E1} \approx L_{E2}$ (small differences between L_{E1} and L_{E2} are caused by the production process). U_{CR} = 580V, U_Z=440V, i_L=125A Scale as in Fig.2, only for time ... 500ns/div.

At turn-off of T_1, i_{L1} (starting at t_u in Fig. 2) flows through D_{L1}, C_{L1} and C_{R1} until the current in L_{E1} goes to zero and L_{E2} has taken over the entire load current. Thereby the energy content of C_{L1} and C_{R1} is increased by $(L_{E1} + L_{E2})i_L/2$.

Also during the recharching oscillations (discussed in section 3.2) energy is transferred from L_{E1} and L_{E2} into the voltage limitation circuit in time interval (t_d, t_f). The essential part of the energies mentioned is due to the load current.

3.3.3. Criteria for Dimensioning of $L_{E1,2}$: The requirements are:

(a) Reduction of the reverse recovery current in the D_{Fi}.
(b) Limitation of the amplitude of the recharging oscillation (described in section 3.2.) and thereby determination of the recharging time based upon given $C_{A1,2}$.
(c) Reduction of the turn-on losses of the power switching devices.
(d) Considering (a) and (b), for any given current the inductances should store an energy amount as small as possible, because this energy determines the size of the step down converter (block 3 in Fig. 1).

Basic facts for (a) - (d): (a) requires saturating reactors for $L_{E1,2}$ (2, 6). At turn-off of $D_{F1,2}$ such reactors make possible highly reduced reverse recovery current peaks as compared to application of air coils. For a meaningful comparison in both cases the same reverse recovery times have to be assumed. Furthermore, by this method the maximum current through the T_i is reduced. Consideration of (d) introduces an optimization problem, where the following aspects are essential: The diode turn-off behavior, the maximum (inverter) pulse frequency and the recharging current amplitude (discussed in section 3.2.).

An additional advantage resulting from the application of saturating reactors is that the R-C-snubbers for $D_{F1,2}$ can be kept smaller (6). These relatively small (additional) snubbers (not shown in Fig.1) have been turned out to be necessary in practice for limitation of the blocking voltage rate of rise across T_i. Keeping the snubbers small results in reduced snubber losses.

In practice $L_{E1,2}$ can be realized as series combination of a linear and a saturating inductance. Thereby (for the purpose of reduced material consumption) the linear inductances can most advantageously be realized for the upper and lower leg as one coil with center tap.

Lead inductances between DC voltage link capacitors and inverter can be considered as contribution to the linear part of $L_{E1,2}$ but are only fully equivalent in their function for certain wiring configurations. However, in any case this simplifies the mechanical construction significantly because then no buffer capacitors have to be applied immediately at the bridge. Thereby also the problem of oscillations induced by inverter switching is reduced; such oscillations would take place in the ringing circuit built up by the DC voltage link capacitors, the buffer capacitors and the lead inductances between them (1). These oscillations in general would be damped very little; due to generally high current amplitudes they would cause a substantial additional current stress on the capacitors. In general, the optimization will result in small values for $L_{E1,2}$. Therefore the rate of current rise will be in the order of magnitude of 100 A/µs in the inverter leg in the case of a bridge short circuit. Turning off even upon "immediate" recognition of a failure would certainly not make possible an operation within the RBSOAR. (Keeping the load line in the RBSOAR usually would

require waiting for discharging the turn-off capacitor. Also, this capacitor due to energy reasons usually will not be dimensioned for handling transistor currents of the order of magnitude given by discharging time multiplied by rate of current rise). It is likely that the short circuit current will exceed the transistor surge current before the earliest possible turn-off point of time.

4. DISCUSSION OF THE RESULTS

The results obtained will be discussed here by considering the requirements stated in section 2:

(1): The requirement of being basically lossless is fulfilled. Only a few published turn-on and turn-off snubbers have met this point so far (e.g., (7, 11)).

(2): The part count of the power devices is largely reduced when compared to existing circuits, such as in, e.g., (2, 7).

(3) and (4): For guaranteeing that for high switching frequency the maximum current to be switched by the transistor is not substantially larger than the maximum load current, realization of (4) had to be omitted in favor of (3). In snubber circuits (with active switching devices) described in the literature so far, despite the introduction of such active devices the discharge of the snubber is via the transistor T (power switching device). This leads to considerable (additional) current stress in T for given turn-off snubber capacitor $C_{A1,2}$ and for given maximum pulse frequency.

(5): This requirement has been met only for the turn-off snubber. The additional voltage level introduced in the turn-on snubber, however, makes possible an exact definition (dimensioning) of the blocking voltage stress on the transistors. This allows a better utilization of the transistor voltage limits. Furthermore energy feedback into the DC voltage links poses no problems. A similar approach has been followed in (2), but restricted to step-down converters.

(6): The fulfilment of this requirement readily can be seen from the circuit functional description. This requirement, e.g., would not be met by using the turn-on snubber of, e.g., Ref. (4); there relatively high voltages result across the diode on the secondary of the transformer used for energy feedback of the turn-on inductance.

(7): This problem is common to all snubber circuits whose function is based on switching devices (including their control circuits). However, an inclusion of a function control for the networks into the safety concept of the system is easily possible.

(8): This requirement certainly is fulfilled. The operation of the snubbers is not connected to a certain switching frequency (as would be the case if the methods of, e.g., Refs. (8) or (9) were applied).

5. CONCLUSIONS

This paper shows that under consideration of the special inverter structure low-loss snubbers (stress-relieving networks) can be designed showing low complexity. The comlexity is substantially lower as compared to arrangements where snubbers developed for step-down converters are used for bridge type inverters. The approach followed here also leads to a largely reduced part count especially when the polyphase inverter structure is taken into account. The feedback of the energy stored in the snubbers into the DC voltage link poses no problems.

The discharge of the turn-off snubbers here is controlled by special circuits dependent on the direction and on the amount of the load current. This discharge basically is lossless; it does not operate via the power switching devices (transistors $T_i = T_{1,2}$ in Fig.1) and therefore imposes no additional current stress on the T_i. Inverters built up with such stress-relieved power switching devices make it possible to control the oscillating currents caused by the snubbers in the inverter legs such that the maximum transistor current is only determined by the load. The exact transistor blocking voltage limitation in the system is very important in view of the limited voltage blocking capability of high power transistors. Furthermore, the mechanical construction is simplified.

For GTOs the problem of stress-relief at turn-off is practically the same. One significant limitation for the application range of GTOs, especially for higher switching frequencies, is given by the losses in the conventional RCD-snubbers used today. It seems to be

advisable therefore to investigate the applicability of the snubber circuits proposed here also to GTOs, especially since there are no basic differences (with respect to replacing RCD snubbers by low-loss snubbers).

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